DataPath systems, inc.

DPS9245 High-Speed 5MS/s 16-Bit ADC with PGA Information Sheet

Features

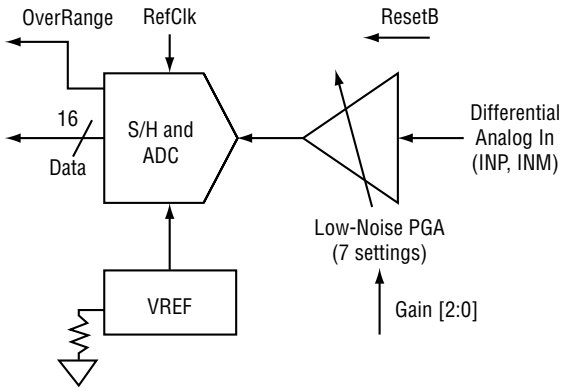
- 16-bit 5 MS/s ADC with on-board voltage reference, programmable gain amplifier and S/H
- Minimal external components: one precision resistor and decoupling capacitors
- 5 V peak-to-peak differential input range
- Resistive inputs > 1 kΩ — easy to drive, without any switched-capacitor kickback transient
- Low-frequency DNL: ±0.5 LSB at 16 bits
- Low-frequency INL: ±1.0 LSB at 16 bits
- Programmable gain amplifier (PGA) preceding ADC with up to 20 dB of gain (7 settings: 0dB, +3dB, +6dB, +12dB, +15dB, +18dB, +20dB)
- Composite input-referred noise floor at peak gain: 8 nV/√Hz
- Higher performance upgrade from AD9260/AD9240/AD9241/AD9243
- 5V ±5% power supply; 3.3V supply for all digital I/O
- User-programmable power dissipation depending on sample rate and linearity required
  - 230 mW at 2.5 MS/s
  - 465 mW at 5 MS/s
- 44-pin LQFP plastic package
- Operating temperature range: –40°C to +85°C

Functional Block Diagram

The DPS 9245 is a versatile analog front end combining a high-resolution 5 MS/s 16-bit ADC, a built-in reference, and a programmable gain amplifier (PGA) with resistive input impedance in a 44-pin package.

The chip includes a digitally calibrated pipeline ADC which is calibrated on assertion of a simple reset signal. The combination of low-noise, high-linearity, high-input impedance buffer (with programmable gain), wideband S/H, on-board voltage references, and simple digital interface (16-bit parallel output word synchronous with the master sampling clock), makes the chip extremely easy to use. The performance of the device with respect to linearity and noise needs to be considered separately, exemplified as follows.

Figure 1
Block diagram of the chip



Linearity: At up to 5 MS/s, and with low input frequencies (~100 kHz) the chip provides outstanding static linearity: DNL is ±0.5 LSB at 16 bits, and SFDR is 100 dB for a near full-scale 60 kHz sinewave. For a 900 kHz sinewave at -10 dBFS (1.5V), SFDR is greater than 90 dB. This linearity is maintained for PGA settings up to 12 dB.

- Dynamic linearity (at 5 MS/s)

Signal Type	Frequencies [kHz)	PGA Setting [dB]	Composite Signal Level at ADC Input [dBFS]	HD3 [dBc]	IM3 [dBc]	SFDR [dB]
Sinusoid	60	0	-0.4	-100		100
Sinusoid	60	20	-0.8	-93		93
Sinusoid	900	12	-11.5	-101		99
2-tone	100, 110	6	-0.7		-98	
2-tone	100, 110	20	-1.0		-98	
2-tone	400, 410	6	-0.6		-97	
2-tone	890, 920	6	-1.6		-87	

Note: in the table, the signal level relative to full-scale (dBFS) is given at the ADC input - i.e., AFTER the PGA, in order to show the dependence on PGA gain; 0 dBFS is 5.0V peak-to-peak differential. The HD3 and IM3 values are given in dBc (dB below carrier) - i.e., dB below the fundamental, or dB below one tone of the two-tone signal, respectively.

Noise: The SNR of the ADC at -1 dBFS is 83 dB, and at -45 dBFS is 39 dB, giving an extrapolated dynamic range of 84 dB. When combined with a programmable gain of up to +20dB gives a composite dynamic range of approximately 100 dB - i.e., for signals 20 dB below full-scale, the chip can provide 80 dB of resolution.

- SNR (at 5 MS/s)

Signal Type	Frequencies [kHz]	PGA Setting [dB]	Composite Signal Level at PGA Input [dBFS]	SNR [dB]
Sinusoid	75	0	-1	83
Sinusoid	75	0	-45	39
Sinusoid	75	20	-21	77
Sinusoid	75	20	-65	33

Note: in the table, the signal level is given at the PGA input - i.e., at chip input, in order to show the dependence on PGA gain and input signal level.

DataPath systems, inc.

(408) 365-6000 Tel • (408) 365-0530 Fax • Email: marketing@datapathsystems.com
www.datapathsystems.com