DataPath systems, inc.

DPS8100 ATU-R
ADSL Analog Front End with Integrated Line Driver Combo IC

Features

- ADSL ATU-R analog front end IC with full receive (RX) and transmit (TX) analog signal path including integrated upstream TX line driver
- Fully monolithic: minimal external components required (2 precision resistors, 2 non-critical resistors, and decoupling capacitors)
- Compatible with both ITU G.992.1 (G.dmt) G.992.2 (G.lite) standard
- Integrated line driver capable of driving +13 dBM onto the line using a 4.25:1 transformer
- Line driver total harmonic distortion for 138 kHz sinewave at 7.4 V peak-to-peak differential with either (a) 11 Ω resistance load or (b) 5.5 Ω resistance and 4.25:1 transformer: -85 dB
- 14-bit linear 4.4 MS/s ADC
- 14-bit linear 4.4 MS/s DAC
- 4th-order continuous time lowpass filters for RX and TX paths, with ±5% cutoff frequency accuracy
- RX (upstream) channel: support for 138 kHz and 276 kHz (for ADSL over ISDN)
- TX (downstream) channel: support for both 552 kHz (G.lite) and 1.104 MHz (G.dmt)
- RX path programmable gain amplifiers (PGA's): -6 dB to +38 dB in 0.25 dB steps
- TX path programmable attenuation amplifiers (PAA's): 0 dB to -24 dB in 1 dB steps
- Maximum signal level at RX inputs: 8 V peak-to-peak differential
- Maximum signal level at TX outputs: 7.4 V peak-to-peak differential
- Entire RX channel (PGA, RX filter, and ADC) linearity: 80 dB MTPR in missing tone test
- Entire TX channel (DAC, TX filter, PAA and driver) linearity: 80 dB MTPR in missing tone test
- RX input-referred noise at peak gain: -160 dBm/Hz at 300 kHz and above (100 Ω system)
- 12-bit DAC to support VCXO
- 4-wire serial port for register control of attenuation/gain settings, filter bandwidths, modes, power down of individual functional blocks etc.
- 5V ±5% power supply; 3.3V supply for all digital I/O
- Power: 1W (driving +13 dBm DMT signal onto the line)
- 128-pin MQFP plastic package
- Operating temperature range: -40°C to +85° C

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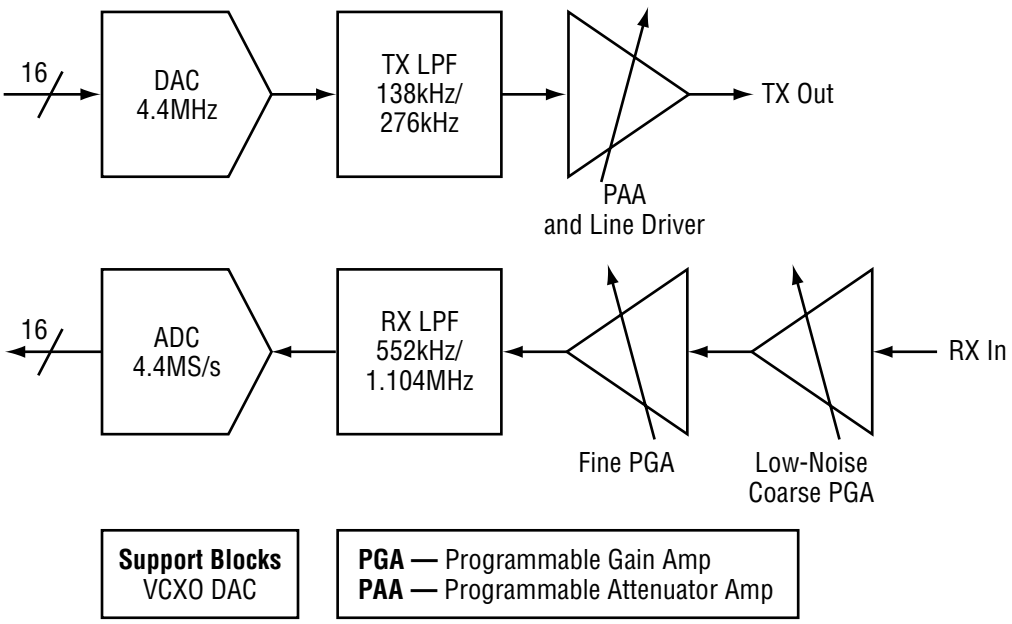
Functional Block Diagram

Fig. 1 Block diagram



General Description

Asymmetric digital subscriber line (ADSL) technology provides a viable solution to meet the emerging need for high-bandwidth communications to the home while utilizing existing twisted-pair copper infrastructure. To simplify the design and reduce deployment costs, DataPath Systems has developed a highly integrated analog front-end IC (DPS8100) designed to perform all of the analog functions of the receive (RX) and transmit (TX) paths for ADSL—full-rate and G.lite—including the line driver, while maintaining the excellent linearity performance of the DPS8001. Integration of the line driver represents a significant cost reduction for the ADSL modem. The chip requires no external circuitry beyond a pair of precision resistors and bypass/coupling capacitors.

The RX portion of the chip comprises a low-noise front end programmable gain amplifier (PGA), an anti-aliasing filter, and a 14-bit A/D converter (ADC). The TX portion consists of a 14-bit D/A converter (DAC), a transmit lowpass filter, and a programmable attenuation amplifier (PAA). To simplify the overall system design, DAC droop compensation is handled internally, removing this burden from the back-end signal processing.

This device includes an integrated TX line driver and, with an appropriate 4.25:1 step up transformer, can drive +13 dBm onto the twisted pair line, as required for the upstream channel in both G.992.1 and G.992.2. Total harmonic distortion of the entire TX channel including line driver is better than 80 dB at full power (+13 dBm on the line).

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Apart from the primary signal paths, the chip also contains support circuitry for other functions required in an ADSL modem. To assist in timing recovery, a 12-bit DAC is present to drive an off-chip voltage controlled crystal oscillator.

The chip's digital input/output interfaces are designed to be as simple as possible, emphasizing ease of design-in and evaluation. The primary digital ADC/DAC interfaces are on separate 16-bit wide busses: 16 for the ADC, and 16 for the DAC. Although the chip itself utilizes a 5V supply voltage, the digital interfaces are fully compliant with either TTL or 3.3V CMOS signal swings. All chip modes are programmable via a single serial port interface.

Information

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