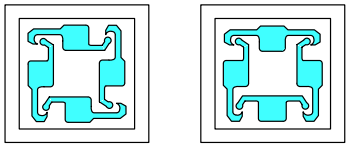
Silicon Beamless Schottky Diodes

Features

- For Microwave MIC Assembly & Automated High Volume Manufacturing Lines
- Mechanically Rugged Design
- Three Barrier Heights for Optimized Mixer Performance
- Wide Product Range: Series Pair, Ring, Bridge, and 8 Diode Ring



Description

The Beamless Diode family is designed for a high degree of device reliability in both commercial and industrial uses. They are designed to offer the utmost in performance as well as achieving price sensitive cost targets for commercial systems.

- Use in ring or crossover designs in double balanced mixer designs
- Virtually any LO requirement can be met with choice of barrier height.
- 100% DC tested on wafer.
- Available in film frame or waffle pack.

Electrical Specifications at 25°C

Part Number	Band	Barrier	V_F I_F = 1.0 mA (mV)		ΔV_F I_F = 1.0 mA (mV)	C_J[1, 2] V_R = 0V, f = 1 MHz (pF)		R_S I_F = 5 mA (Ohms)	V_B (V)@ 10 μA	Outline Drawing Number
			Min.	Max.		Min.	Max.		Min.	
Ring Quad[3]										
DMF3926–000	S	Low	200	260	10	0.3	0.5	5.0	2	551–002
DME3927–000	S	Medium	300	400	10	0.3	0.5	5.0	3	551–002
DMJ3928–000	S	High	500	600	10	0.3	0.5	5.0	4	551–002
DMF3942–000	X	Low	250	310	10	0.15	0.30	8.0	2	551–002
DME3943–000	X	Medium	325	425	10	0.15	0.30	8.0	3	551–002
DMJ3944–000	X	High	550	650	10	0.15	0.30	8.0	4	551–002
Bridge Quad[3]										
DMF3929–000	S	Low	200	260	10	0.3	0.5	5.0	2	551–004
DME3930–000	S	Medium	300	400	10	0.3	0.5	5.0	3	551–004
DMJ3931–000	S	High	500	600	10	0.3	0.5	5.0	4	551–004

1. C_J represents total capacitance.
2. Maximum C_J unbalance @ 0V, 1 MHz = .025 pF.
3. Matching Criteria V_F @ 1 mA $\leq$ 15 mV available for matched sets.

Electrical Specifications (Continued)

Part Number	Band	Drive Level	V_F I_F = 1.0 mA (mV)		ΔV_F I_F = 1.0 mA (mV)	C_J[1, 2] V_R = 0V, f = 1 MHz (pF)		R_S I_F = 5 mA (Ohms)	V_B (V)@ 10 μA	Outline Drawing Number
			Min.	Max.	Max.	Min.	Max.	Max.	Min.	
Series Pair[3]										
DMF3932–000	S	Low	200	260	10	0.3	0.5	5	2	551–012
DME3933–000	S	Medium	300	400	10	0.3	0.5	5	3	551–012
DMJ3934–000	S	High	500	600	10	0.3	0.5	5	4	551–012
Back to Back Ring Series Pair[3]										
DMF3935–000	S	Low	200	260	10	0.3	0.5	5.0	2	551–056
DME3936–000	S	Medium	300	400	10	0.3	0.5	5.0	3	551–056
DMJ3937–000	S	High	500	600	10	0.3	0.5	5.0	4	551–056
OctoQuad Ring[4]										
DMF3938–000	S–X	Low	400	520	15	0.15	0.3	16	4	556–020
DME3939–000	S–X	Medium	600	800	15	0.15	0.3	16	6	556–020
DMJ3940–000	S–X	High	1000	1200	15	0.15	0.3	16	8	556–020

1. C_J represents total capacitance.
2. Maximum C_J unbalance @ 0V, 1 MHz = .025 pF.
3. Matching Criteria V_F @ 1 mA $\leq$ 15 mV available for matched sets.
4. Matching criteria V_F @ 1 mA $\leq$ 20 mV available for matched sets.

Maximum Ratings

T_{STG}:	–65°C to +175°C
T_{OP}:	–65°C to +150°C
P_{diss} CW:	75 mW/junction
I_{MAX}:	50 mA Volts
PIV:	V_B rating

Packing Methods

1. Vacuum release gel–pack.
2. Wafer on film frame (rejects are marked with ink).
   - Diced, ready for pick and place
   - Unsawn whole wafer, 7 mil thick, max.

Assembly and Handling Procedure

The process flow for assembly is:

1. Die attach using nonconductive epoxy
2. Wire bond
3. Encapsulation – nonconductive epoxy

Die Attach Methods

All leadless chips are compatible with both eutectic and conductive epoxy die attach methods. Eutectic processes use Sn–Au or Sn–Pb solder. Non conductive die attach is recommended.

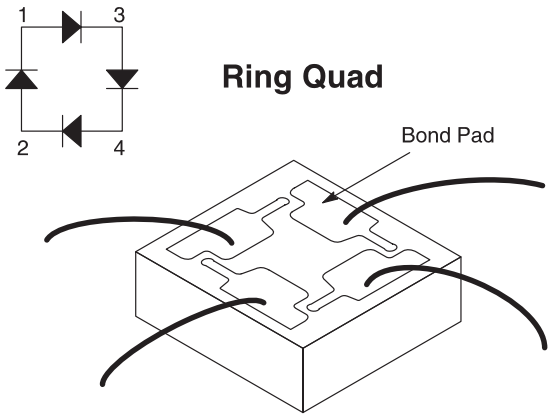
Wire Bonding

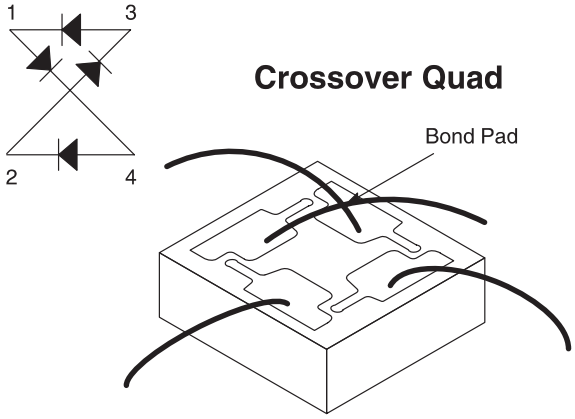
Two methods can be used to connect wire, ribbon, or wire mesh to the chips:

- Thermocompression
- Ballbonding

Alpha recommends use of pure gold wire.

Typical Bonding Configuration



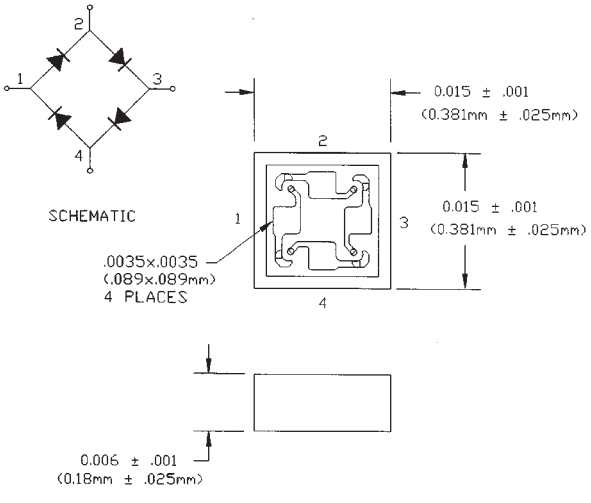


Spice Parameters (Per Junction and Barrier Height)

Part Number Prefix	I_S A	R_S Ohm	N	T_D S	C_J pF	M	E_G eV	V_D eV	X_J1	F_C	B_V	I_{BV} A
DMF	2.5E–7	4	1.04	1.E–11	0.42	0.32	0.69	0.51	2	0.5	2	1E–5
DME	1.3E–9	4	1.04	1.E–11	0.39	0.37	0.69	0.65	2	0.5	3	1E–5
DMJ	9E–13	4	1.04	1.E–11	0.39	0.42	0.69	0.84	2	0.5	3	1E–5

Outline Drawings

551–002



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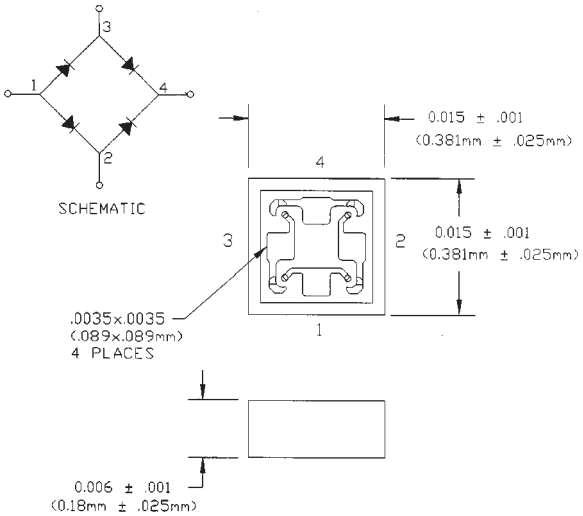

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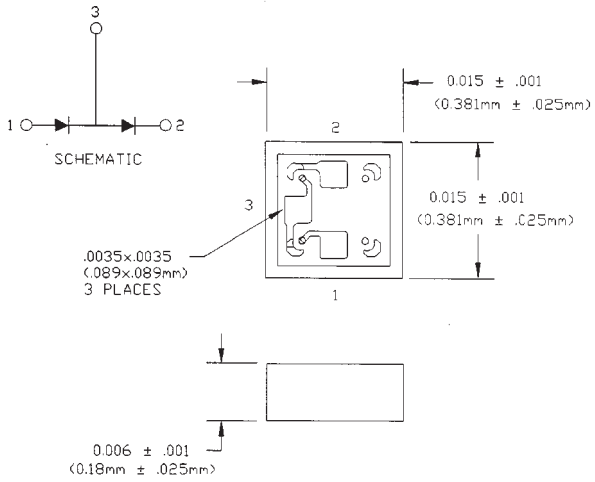

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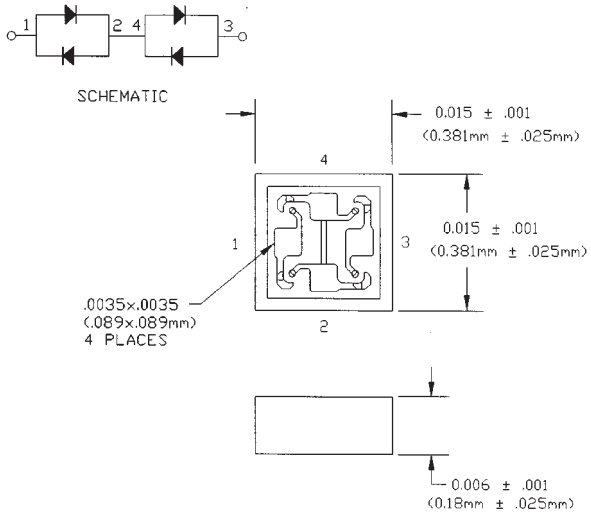

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