ADSL Analog Front End IC
DPS8000 (for ATU-C)
DPS8001 (for ATU-R)

Data Sheet
V1.1.1

DataPath Systems, Inc.

01/20/2000

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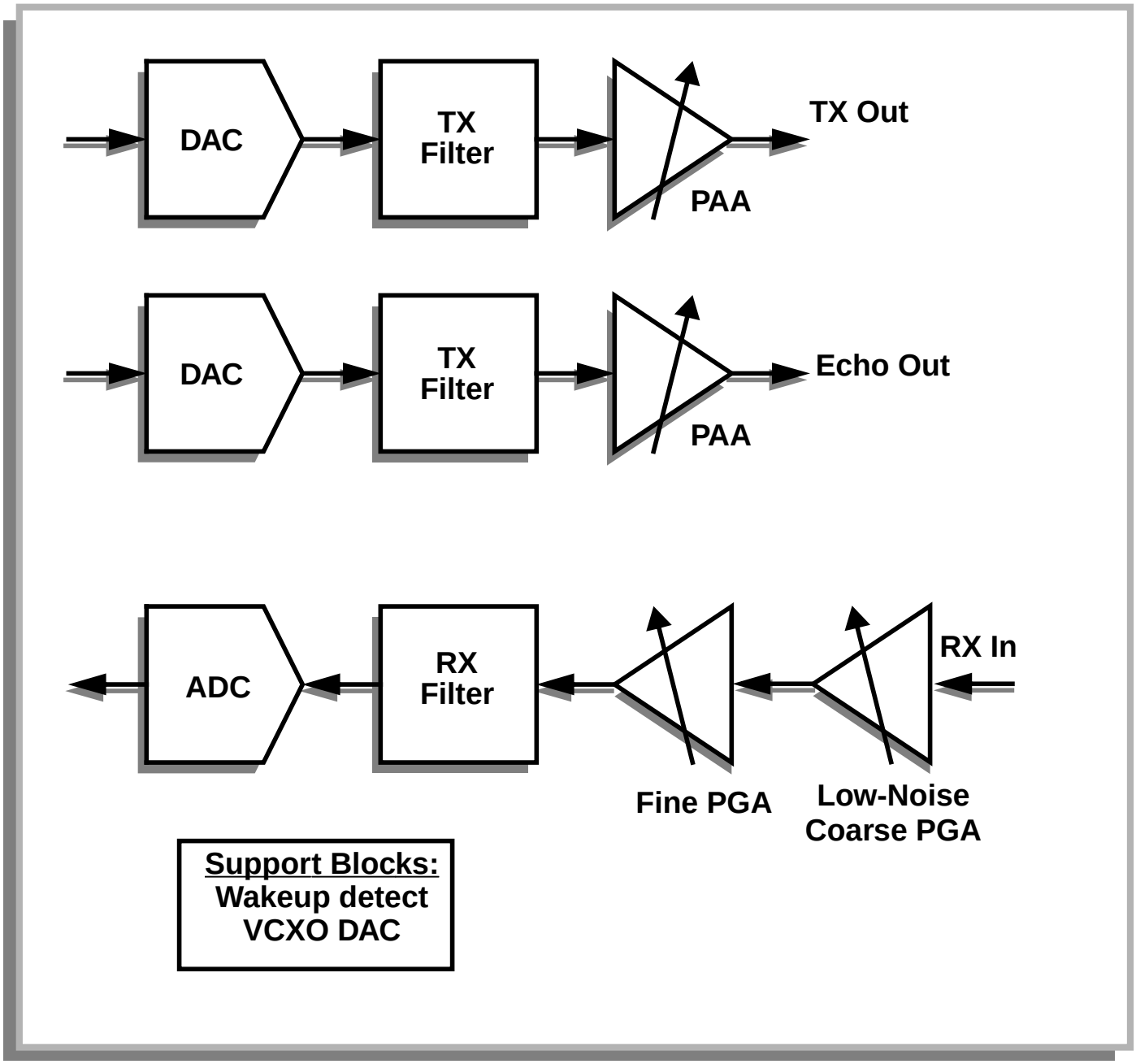
DataPath systems, inc.

1 Features

- ADSL analog front end IC with full RX and TX analog signal path for ATU-R and ATU-C (excluding pots reject filter and high-voltage line drivers/receivers).
- Fully monolithic: minimal external components required (2 precision resistors, 2 non-critical resistors, and decoupling capacitors)
- Support for both echo-cancelled and frequency-division based systems; full analog echo path support in hardware.
- Compatible with ITU G.992.1 *(G.dmt)* and G.992.2 *(G.lite)* standards
- Upstream channel: support for both 138 kHz and 276 kHz (for ADSL over ISDN)
- Downstream channel: support for both 552 kHz (*G.lite*) and 1.104 MHz (*G.dmt*)
- 14-bit linear 4.416 MS/s ADC
- Dual 14-bit linear 4.416 MHz DAC's
- 4th-order lowpass filters for receive and transmit paths, with ±5% cutoff frequency accuracy
- Programmable gain stages and attenuators in RX and TX paths
- ATU-R receive path noise PSD: –160 dBm/Hz at 300 kHz and above (100 Ω system)
- ATU-C receive path noise PSD: –153 dBm/Hz at 30 kHz and above (100 Ω system)
- Integrated wakeup detector for ATU-C†
- 12-bit DAC to support VCXO
- 4-wire serial port for register control of attenuation/gain settings, filter bandwidths, modes, power down of individual functional blocks etc.
- 5V ± 5% power supply; 3.3V supply for all digital I/O
- Power: 0.825 W (full-rate ADSL, with full echo channel turned on))
  0.675 W (full-rate ADSL, echo channel not used — i.e., for typical FDM system)
- 128-pin MQFP plastic package
- Operating temperature range: –40°C to +85°C

†For more information on the operation of this block, please contact DataPath Systems.

2 Functional Block Diagram



3 General Description

Asymmetric digital subscriber line (ADSL) technology provides a viable solution to meet the emerging need for high-bandwidth communications to the home while utilizing existing twisted-pair copper infrastructure. To simplify the design and reduce deployment costs, DataPath Systems has developed an analog front-end IC designed to perform all of the analog functions of the receive (RX) and transmit (TX) paths for ADSL, excluding POTS reject filtering and high-voltage line drivers/receivers. The chip requires no external circuitry beyond a pair of precision resistors and bypass/coupling capacitors. Note that (a) for full compliance with the ITU G.992.1 and G.992.2 transmit PSD masks, additional off-chip filtering in the TX path is needed; (b) in FDM systems, additional off-chip bandsplit filtering may be required for system optimization.

Two versions of the chip exist:
one for the customer remote modem (ATU-R, part number DPS8001) and
one for the central office modem (ATU-C, part number DPS8000).

The chip will allow maximum data throughput greater than 8 Mb/s downstream and 800 kb/s upstream on short lines. At the other extreme, the linearity and noise performance of the analog signal paths enable the chip to successfully transmit and receive data at 1.5 Mb/s on the longest lines — above 18 kfeet of AWG24 wire. The chip can be utilized in systems employing either echo cancellation (EC) or frequency division multiplexing (FDM), and is also fully compatible with the emerging *G.lite* standard. Support for simultaneous operation of ADSL over ISDN is also present. Thus, an ADSL modem equipped with this chip will operate on the vast majority of phone lines worldwide, enabling maximum data rate with maximum reach between the central office (CO) and the remote site.

The RX portion of the chip comprises a low-noise front end programmable gain amplifier (PGA), an anti-aliasing filter, and a 14-bit A/D converter (ADC). The TX portion consists of two independent signal paths, one for the primary transmit signal and one to support echo. One key feature is excellent matching between the echo path and the primary TX path, minimizing difficulties in echo cancellation arising from mismatch between the two. Each path consists of a 14-bit D/A converter (DAC), a transmit lowpass filter, and a programmable attenuation amplifier (PAA). To simplify the overall system design, DAC droop compensation is handled internally, removing this burden from the back-end signal processing.

Apart from the primary signal paths, the chip also contains support circuitry for other functions required in an ADSL modem. To assist in timing recovery, a 12-bit DAC is present to drive an off-chip voltage controlled crystal oscillator. An all-analog “wakeup” detector is present to minimize power consumption in the CO. When the ADSL line is unused, all of the back-end digital and analog circuitry in the modem can thus be powered down, facilitating significant power savings.

The chip’s digital input/output interfaces are designed to be as simple as possible, emphasizing ease of design-in and evaluation. The primary digital ADC/DAC interfaces are on separate 16-bit wide busses. Although the chip itself utilizes a 5V supply voltage, the digital interfaces are fully compliant with either TTL or 3.3V CMOS signal swings. All chip modes are programmable via a single serial port interface.

4 Electrical Specifications

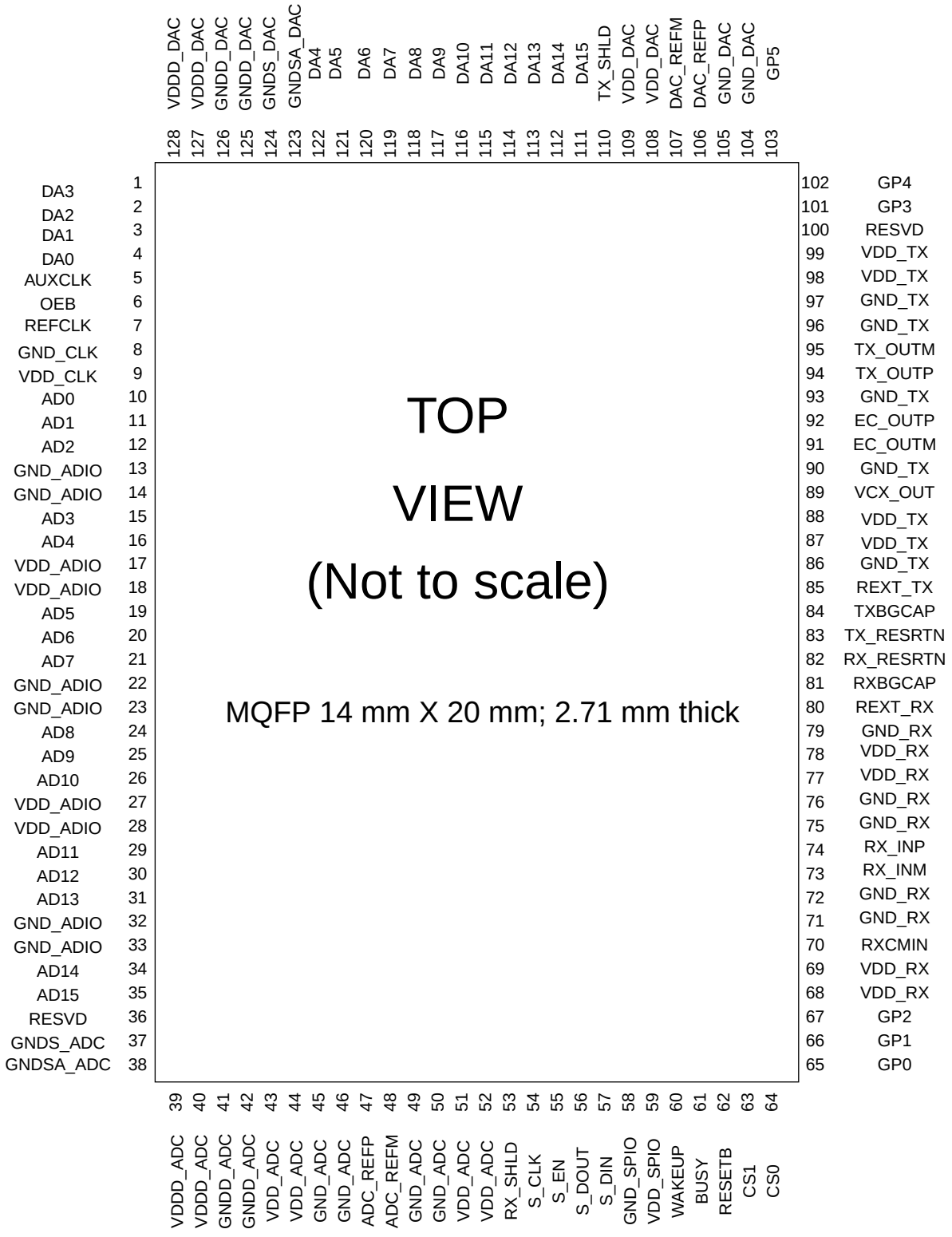
Notes: (a) † indicates not tested in production — guaranteed by design or characterization
(b) dBFS: dB below full scale signal level

Parameter	Min	Typ	Max	Units	Notes/Conditions
General					
†Operating temperature	–40		+85	°C	
Chip power supplies	4.75	5.0	5.25	V	
VDD_ADIO power supply	3.0	3.3	5.25	V	For this supply only
Power supply current		165		mA	Echo path on
		135		mA	Echo path off
RX Path					
ATU-R input-referred noise floor	–156	–160		dBm/Hz (100 Ω)	At frequencies >300 kHz. Assumes maximum-sensitivity condition: PGA's are at maximum gain.
ATU-C input-referred noise floor	–150	–153		dBm/Hz (100 Ω)	At frequencies >30 kHz. Assumes maximum sensitivity condition: PGA's are at maximum gain.
PGA range		–6 to +38		dB	
PGA gain accuracy	–0.2	0	+0.2	dB	
PGA step size		0.25		dB	
ATU-R low-pass filter cutoff frequency		1.104		MHz	Full-rate mode
		552		kHz	Halfband (G.lite) mode
ATU-C low-pass filter cutoff frequency		138		kHz	Non-ISDN mode
		276		kHz	ISDN mode
Filter bandedge tolerance	–5%		+5%		
Entire RX channel (PGA, filter, and ADC) linearity: Multitone Power Ratio (MTPR)		80		dB	The test pattern is a 248-tone multitone over the 1.104 MHz band with 8 missing tones and aggregate level –3 dBFS. PAR is 7.7 dB
†Input resistance	100			kΩ	On pins RX_INP, RX_INM
†Input capacitance			120	pF	On pins RX_INP, RX_INM

Parameter	Min	Typ	Max	Units	Notes/Conditions
TX Path					
PAA range		0 to –24		dB	
PAA gain accuracy	–0.2	0	+0.2	dB	
PAA step size		1.0		dB	
ATU-C low-pass filter cutoff frequency		1.104		MHz	Full-rate mode
		552		kHz	Halfband (G.lite) mode
ATU-R low-pass filter cutoff frequency		138		kHz	Non-ISDN mode
		276		kHz	ISDN mode
Filter bandedge tolerance	–5%		+5%		
Entire TX channel (DAC, filter, and PAA) linearity: Multitone Power Ratio (MTPR)		80		dB	The test pattern is a 248-tone multitone over the 1.104 MHz band with 8 missing tones and aggregate level –3 dBFS. PAR is 7.7 dB
Output load	2	5		kΩ	Resistance to ground (ac coupled), on pins TX_OUTP, TX_OUTM, EC_OUTP, EC_OUTM
		10		pF	Capacitance to ground on pins TX_OUTP, TX_OUTM, EC_OUTP, EC_OUTM
ADC					
†Resolution		16		Bits	
Effective number of bits		13.0		Bits	
Linearity		14.0			
Full scale input range		±2.5		V ppd	
Full scale range accuracy	–5%		+5%		
DAC					
†Resolution		16		Bits	
Effective number of bits		13.5		Bits	
Linearity		14.0			
Full scale output range		±2.5		V ppd	
Full scale range accuracy	–5%		+5%		

Parameter	Min	Typ	Max	Units	Notes/Conditions
VCXO DAC					
Resolution		12		Bits	Guaranteed monotonic
Maximum output voltage		4.0		V	Input word = FFFH
Minimum output voltage		0.5		V	Input word = 000H

5 Pinout


1 DA3
2 DA2
3 DA1
4 DA0
5 AUXCLK
6 OEB
7 REFCLK
8 GND_CLK
9 VDD_CLK
10 AD0
11 AD1
12 AD2
13 GND_ADIO
14 GND_ADIO
15 AD3
16 AD4
17 VDD_ADIO
18 VDD_ADIO
19 AD5
20 AD6
21 AD7
22 GND_ADIO
23 GND_ADIO
24 AD8
25 AD9
26 AD10
27 VDD_ADIO
28 VDD_ADIO
29 AD11
30 AD12
31 AD13
32 GND_ADIO
33 GND_ADIO
34 AD14
35 AD15
36 RESVD
37 GNDS_ADC
38 GNDSA_ADC
39 VDDD_ADC
40 VDDD_ADC
41 GNDD_ADC
42 GNDD_ADC
43 VDD_ADC
44 VDD_ADC
45 GND_ADC
46 GND_ADC
47 ADC_REFP
48 ADC_REFM
49 GND_ADC
50 GND_ADC
51 VDD_ADC
52 VDD_ADC
53 RX_SHLD
54 S_CLK
55 S_EN
56 S_DOUT
57 S_DIN
58 GND_SPIO
59 VDD_SPIO
60 WAKEUP
61 BUSY
62 RESETB
63 CS1
64 CS0
65 GP0
66 GP1
67 GP2
68 VDD_RX
69 VDD_RX
70 RXCMIN
71 GND_RX
72 GND_RX
73 RX_INM
74 RX_INP
75 GND_RX
76 GND_RX
77 VDD_RX
78 VDD_RX
79 GND_RX
80 REXT_RX
81 RXBGCAP
82 RX_RESRTN
83 TX_RESRTN
84 TXBGCAP
85 REXT_TX
86 GND_TX
87 VDD_TX
88 VDD_TX
89 VCX_OUT
90 GND_TX
91 EC_OUTM
92 EC_OUTP
93 GND_TX
94 TX_OUTP
95 TX_OUTM
96 GND_TX
97 GND_TX
98 VDD_TX
99 VDD_TX
100 RESVD
101 GP3
102 GP4
103 GP5
104 GND_DAC
105 GND_DAC
106 DAC_REFP
107 DAC_REFM
108 VDD_DAC
109 VDD_DAC
110 TX_SHLD
111 DA15
112 DA14
113 DA13
114 DA12
115 DA11
116 DA10
117 DA9
118 DA8
119 DA7
120 DA6
121 DA5
122 DA4
123 GNDSA_DAC
124 GNDS_DAC
125 GNDD_DAC
126 GNDD_DAC
127 VDDD_DAC
128 VDDD_DAC
TOP
VIEW
(Not to scale)
MQFP 14 mm X 20 mm; 2.71 mm thick

6 Pin Function Description

Pin Number	Pin Name	Pin Function Description
111,112,113,114, 115,116,117,118, 119,120,121,122, 1,2,3,4	DA15,...,DA0	DAC inputs: MSB is DA15; LSB is DA0
5	AUXCLK	In echo mode, auxiliary clock (=REFCLK/2). Serves as a data tag identifying DAC data as either transmit or echo. In non-echo mode, connect to ground.
6	OEB	Output enable for ADC digital outputs (active low)
7	REFCLK	Master reference clock input — either 8.832 MHz or 4.416 MHz
8	GND_CLK	Ground
9	VDD_CLK	+5.0V
10,11,12,15,16,17, 19,20,21,24,25,26, 29,30,31,34,35	AD0,...,AD15	ADC digital outputs: MSB is AD15; LSB is AD0
13,14,22,23,32,33	GND_ADIO	Ground
17,18,27,28	VDD_ADIO	Power supply for ADC outputs (+3.3V or +5V)
36	RESVD	Reserved — no connect
37	GNDS_ADC	Ground
38	GNDSA_ADC	Ground
39,40	VDDD_ADC	+5.0V
41,42	GNDD_ADC	Ground
43,44,51,52	VDD_ADC	+5.0V
45,46,49,50	GND_ADC	Ground
47,48	ADC_REFP, ADC_REFM	ADC reference voltage outputs
53	RX_SHLD	Ground
54	S_CLK	Serial port clock input to IC
55	S_EN	Serial port enable input to IC
56	S_DOUT	Serial port data output from IC
57	S_DIN	Serial port data input to IC

Pin Number	Pin Name	Pin Function Description
58	GND_SPIO	Ground
59	VDD_SPIO	+5.0V
60	RESVD	Reserved — no connect
61	BUSY	Active high output indicating chip is in self-calibration or reset mode
62	RESETB	Resets internal state of chip (active low)
63,64	CS1,CS0	Chip select address inputs
65,66,67	GP0, GP1, GP2	General purpose I/O (default: no connect)
68,69,77,78	VDD_RX	+5.0V
70	RXCMIN	Common-mode reference voltage output
71,72,75,76,79	GND_RX	Ground
73,74	RX_INP, RX_INM	Analog inputs to IC
80	REXT_RX	External resistor connection on RX side
81	RXBGCAP	External capacitor connection on RX side
82	RX_RESRTN	Resistor return on RX side
83	TX_RESRTN	Resistor return on TX side
84	TXBGCAP	External capacitor connection on RX side
85	TEXT_RX	External resistor connection on TX side
86,90,93,96,97	GND_TX	Ground
87,88,98,99	VDD_TX	+5.0V
89	VCX_OUT	VCXO DAC output voltage
91,92	EC_OUTP, EC_OUTM	Analog outputs of echo path
94,95	TX_OUTP, TX_OUTM	Analog outputs of TX path
100	RESVD	Reserved — no connect
101,102,103	GP3, GP4, GP5	General purpose I/O (default: no connect)
104,105	GND_DAC	Ground
106,107	DAC_REFP, DAC_REFM	DAC reference voltage outputs
108,109	VDD_DAC	+5.0V
110	TX_SHLD	Ground

Pin Number	Pin Name	Pin Function Description
123	GNDSA_DAC	Ground
124	GNDS_DAC	Ground
125,126	GNDD_DAC	Ground
127,128	VDDD_DAC	+5.0V

7 IC Operation and Functionality

7.1 Overview

The following sections describe in greater detail individual blocks and functions on the chip with particular focus on the register bits associated with various modes. First, in Section 7.2, some global modes are described. Then, in Sections 7.3–7.6, the RX path, TX path, ADC, and DAC respectively are discussed. Section 7.7 describes the serial port interface and Sections 7.8 and 7.9 cover some of the ADSL modem support functions included in the chip and some miscellaneous interface issues, respectively.

In the RX portion of the chip, the incoming analog differential signal (maximum level ±4 V peak-to-peak differential, i.e., +22 dBm relative to 100 Ω) enters the chip at the RX_INP, RX_INM pins. The analog signal path is partitioned into a continuous-time (CT) section and an ADC. The CT section consists of a number of stages of programmable gain followed by a 4th order lowpass filter. The gain is set by the user by programming the RXGAIN register. The output of the filter is fed directly to the ADC, which samples at either 4.416 MS/s or 2.208 MS/s and outputs a 16-bit wide parallel word.

In the TX portion of the chip, when the echo path is *not* used, the incoming 16-bit digital word is fed to the DAC at a 4.416 MHz update rate. The DAC output is re-sampled (de-glitched) and is passed to the continuous-time section comprising a 4th order lowpass filter followed by a programmable attenuation amplifier (PAA). The amount of attenuation is set by the user by programming the TXGAIN register. The output of the PAA appears at the TX_OUTP, TX_OUTM pins and can drive an ac-coupled load of 2 kΩ in parallel 10 pF with maximum level of ±2.5 V.

When the echo path *is* used, the chip accepts digital data at an 8.832 MHz rate and alternate digital words are passed in a ping-pong fashion to the main TX path and the echo path, which each operate at 4.416 MHz. To identify which sample goes to the TX path and which goes to the echo path, a “label” or “tag” input, AUXCLK, is used, which is described in more detail later.

The chip requires a single low-jitter clock to be applied at the REFCLK pin. All clock generation is performed internally and all converter and S/H clocks in both RX and TX paths are directly derived from REFCLK. REFCLK must *always* be either 4.416 MHz or 8.832 MHz; frequency tolerance is ±100ppm. When the echo path is not used, REFCLK should be 4.416 MHz. When the echo path is used, REFCLK should be 8.832 MHz and the AUXCLK pin should be used to identify TX or echo data. Since AUXCLK alternates between 1 and 0 on each period of REFCLK, it could be viewed as a 4.416 MHz clock signal. The MODE register sets the appropriate sample rates and enables or disables the echo path, as discussed in Section 7.2.2.

Two versions of the chip exist — one customized for ATU-R and one customized for ATU-C. The ATU-R version contains a high-bandwidth RX path lowpass filter and low-bandwidth TX/echo path lowpass filters. The ATU-C version contains high-bandwidth TX/echo path lowpass filters and a low-bandwidth RX path lowpass filter. All remaining blocks behave identically in the two versions.

7.2 Global Modes and Power Control

7.2.0 Introduction

The chip can be configured in a number of ways depending on the particular system requirements. These configurations include various sample rates and individual functional block power control modes enabling power to be saved when a block is not used. The chip registers are 16-bit wide; the detailed read/write protocol is discussed in Section 7.8. In the following sections the registers are tabulated as two 8-bit bytes, a low byte and a high byte, that form the 16-bit word. Each register has an address in hex and an associated name. If a register bit is shaded, this indicates that it is reserved for internal or test use only and should be set to the value indicated. In later versions of this document, DataPath may supply alternative settings for these registers. Unless otherwise stated, all register descriptions hold for *both* ATU-R and ATU-C versions of the chip.

On power-up, the chip expects an active low reset pulse to be applied to the RESETB pin. This resets all the gain and mode registers to particular values, which is detailed below. [A useful debugging check is to read back the state of these registers after reset and check that the values are as expected.]

7.2.1 Global Power Control Register 01H (PWR)

The global power on/off control of individual blocks on the chip is set by the PWR register, (01H), as tabulated below.

Register 01H (PWR)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name		P6	P5	P4	P3		P1	
Reset Value	0	0	0	0	0	1 (ATU-C) 0 (ATU-R	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name			P13	P12	P11	P10	P9	P8
Reset Value	1	1	1	1	1	1	0 (ATU-C) 1 (ATU-R)	0 (ATU-C) 1 (ATU-R)

The convention for power on/off is as follows.

0: block power on
1: block power off

The assignment of the individual bits in the PWR register is as follows.:

P13	Chip initialization support circuits
P12	Chip initialization support circuits
P11	Chip initialization support circuits
P10	Chip initialization support circuits
P9	VCXO DAC
P6	DAC
P5	ADC
P4	CT blocks in echo path
P3	CT blocks in primary TX path
P1	CT blocks in RX path block — i.e., filter/PGA/PAA etc.

Note that whenever an analog block is powered on, appropriate time must be allowed for settling of internal bias circuits.

7.2.2 Global Mode Control Register 02H (MODE)

The chip is configurable to support various converter rates and filter modes in the signal paths. These global modes are primarily set using the MODE register, as tabulated below.

Register 02H (MODE)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	RXFLTLOW	TXFLTLOW	CLK1	CLK0	AUXCLKINV			
Reset Value	0	0	0 (ATU-C) 1 (ATU-R)	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name								
Reset Value	0	0	0	0	0	0	0	0

ISDN Mode / Halfband Mode Control

The fast-channel (downstream) filters (ATU-R RX and ATU-C TX) default to 1.104 MHz on reset. (Note, however, that a 552 kHz halfband mode exists for the ATU-R receive filter, as detailed below.) The register bits RXFLTLOW and TXFLTLOW control the bandwidth settings on the upstream filters and the halfband mode, as follows.

TXFLTLOW: low-bandwidth mode on for the transmit-path filters.

In the case of the ATU-R:

0: enable ISDN mode (all transmit/echo filters set to 276 kHz).
1: non-ISDN mode (all transmit/echo filters set to 138 kHz).

In the case of the ATU-C:

0: normal mode (all transmit/echo filters set to 1.104 MHz).
1: reserved

RXFLTLOW: low-bandwidth mode on for the receive-path filters.

In the case of the ATU-R:

0: normal mode (receive filter set to 1.104 MHz).
1: halfband mode (receive filter set to 552 kHz).

In the case of the ATU-C:

0: enable ISDN mode (receive filter set to 276 kHz).
1: non-ISDN mode (receive filter set to 138 kHz).

Clock Mode Control

The CLK[1:0] bits control the clocking modes depending on whether the echo path is used or not. Their functionality is as follows.

CLK[0]: ADC clock rate.

0: ADC samples at 4.416 MHz
1: ADC samples at 2.208 MHz

CLK[1]: Echo path clocks enable.

0: echo clocks disabled and chip expects single 4.416 MHz reference clock at the REFCLK pin.
1: echo path and associated DAC functions enabled and chip expects 8.832 MHz clock at the REFCLK pin and a 4.416 MHz clock at the AUXCLK pin to select TX or ECHO data.

AUXCLK = 1 identifies transmit data

AUXCLK = 0 identifies echo data

A summary of the four possible clocking configurations based on CLK[1:0] is given below.

CLK[1:0]	Echo Path	REFCLK	AUXCLK	ADC
00	OFF	4.416 MHz	0	4.416 MHz
01	OFF	4.416 MHz	0	2.208 MHz
10	ON	8.832 MHz	4.416 MHz	4.416 MHz
11	ON	8.832 MHz	4.416 MHz	2.208 MHz

☛WARNING

- The voltages on REFCLK and AUXCLK pins and the CLK[1:0] register bits *must correspond according to the above table.* For example, setting CLK[1:0]=10 with AUXCLK grounded will result in unpredictable behavior.
- The MODE register does not control any analog power on/off. Therefore, if the echo path is used, the relevant bits in both PWR and MODE registers need to be set accordingly.

Note that (a) it is only possible to run ADC at either 4.416 MS/s or 2.208 MS/s; and (b) the DAC always samples incoming digital data at 4.416 MHz.

DAC TX/Echo Timing Protocol

AUXCLKINV: Inverts the interpretation of TX/Echo data with respect to AUXCLK when the echo path is used; see Section 7.6.1.

7.2.3 Chip Startup/Initialization Sequence

The information below is given as a reference guideline only. DataPath will supply this entire initialization sequence described below as a list of register writes, via e-mail or on floppy disk. The user simply has to download the appropriate register values, and wait for the initialization to complete.

☛WARNING

- **This initialization sequence, including the register download supplied by DataPath is required to operate the chip. Without this, the chip will not work.**

- On power-up, the chip expects RESETB (pin 62) to be held low for at least 1 ms. The power supply voltages applied to the chip must be stable during this time. This reset causes all registers on the chip (excluding certain registers associated with ADC and DAC) to be reset to known states. Those reset values are documented in the register definitions for each register. ATU-R and ATU-C have different reset values for some registers.

- Note that the analog blocks on the chip require significant time to power on and come up to their quiescent dc states. Allowance may be needed also for thermal time constants associated with the package/board.

- Following this hard reset on the RESETB pin, but *before* entering the chip initialization phase, the user should program any registers that are required to be different from their default values — especially the PWR and MODE registers.

- Next, the following writes must occur:

  a “0” must be written to bits P10, P11, P12 and P13 in the PWR register, and

  a “1” must be written to bit 0 in the MODE register

  0080H must be written to register 03H (CALC)

The user must then download a set of DataPath-supplied values to registers 04H and 05H on the chip. These values, along with the register writes already described in this section, will be supplied by DataPath via floppy disk or e-mail.

- Next, the chip is initialized by triggering the internal initialization functions. The user must write a “1” to BIT4 of register 03H (CALC) to start the internal initialization sequence. Since bit 7 must be maintained set, this means that **the user should write 0090H to register 03H.**

- Once the chip enters initialization, it asserts an active high signal on BUSY (pin 61). When the initialization is complete, BUSY is de-asserted and the chip is ready for normal operation. During initialization, (BUSY asserted), the user should not write to any registers on chip. The maximum duration of this initialization phase is 2 s. Note that BUSY cannot be tristated: it is always driven either high or low. Upon completion of the internal initialization operations, the initialization control bit (BIT4) in register CALC is reset. As a debugging check, the user can further check that the initialization completed correctly by reading back the contents of the CALC register: it should be 0080H.

- After initialization, the following writes should occur:

  a “1” should be written to bits P10, P11, P12 and P13 in the PWR register, and

  a “0” must be written to bit 0 in the MODE register.

  The write to the PWR register is optional — it powers down some initialization support circuits. The write to bit 0 of the MODE register is mandatory.

7.2.4 Initialization Control Register 03H (CALC)

As mentioned above, chip initialization is performed by writing “1” to the appropriate bits in the CALC register, as tabulated below.

Register 03H (CALC)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Reset Value	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name						TWOS		
Reset Value	0	0	0	0	0	0	0	0

BIT[7:0] trigger internal initialization operations. When the particular bit is SET, the operation is started. When the operation is completed, the bit is RESET.

BIT7: Enable complete initialization

BIT4: Start complete initialization

TWOS: Two’s complement control for ADC outputs (described later in Section 7.3.5).

As mentioned in Section 7.2.3 above, to trigger initialization, the user should write a “1” to BIT7 and BIT4 of register CALC.

7.3 Continuous-Time Blocks in RX Path

7.3.0 Introduction

The continuous-time (CT) blocks comprise a major portion of the receive analog signal paths, providing programmable gain and filtering. A high-level block diagram of the RX signal path is shown below in Fig. 1.

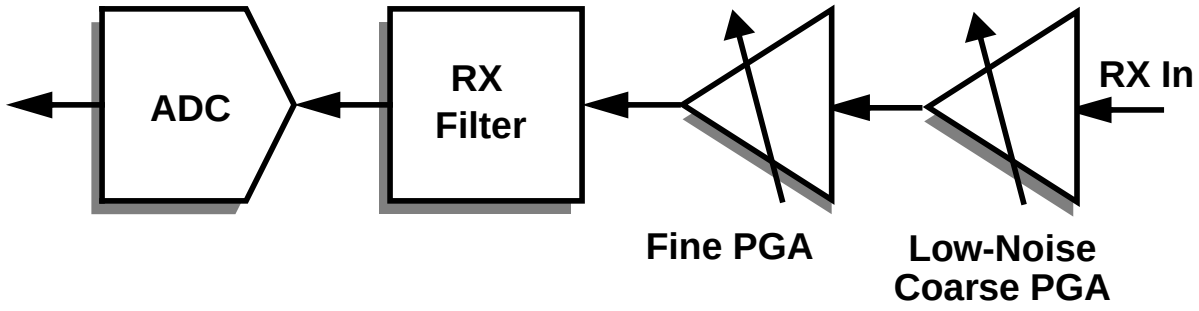


Fig. 1 Diagram showing major portions of the receive signal path

The primary receive inputs are differential, and should be capacitively coupled into the chip. To avoid clipping, signal swing at the inputs should not exceed 8 V peak-to-peak differential (4 V peak-to-peak single ended). The chip provides its own common-mode voltage (on the pin marked RXCMIN), and the input common mode is established by a pair of resistors on the board, as shown in Fig. 2. Output drive capability of RXCMIN is a maximum of 47 µA (50 kΩ to ground).

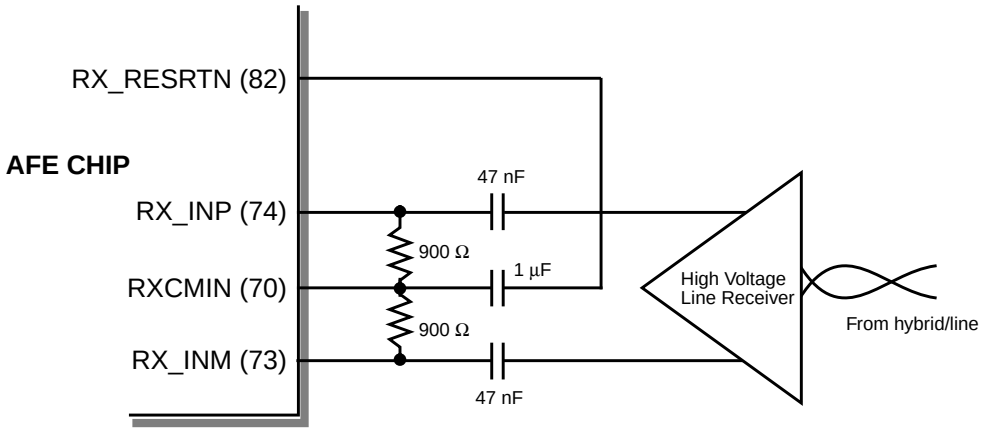


Fig. 2 Recommended receive-side chip interface. Note that other connections to the RX_RESRTN pin are illustrated in Fig. 13.

From the block diagram, there are two programmable gain amplifiers (PGA), one providing coarse-resolution gain control (6 dB steps) and one providing fine-resolution gain control (0.25 dB steps). The coarse PGA (register bits RXGAIN[4:0]) has lower noise, whereas the fine PGA (register bits RXGAIN[11:5]) has higher linearity. Thus, as a general guideline, to maximize noise performance in the receive path, gain should preferentially be placed in the coarse PGA as opposed to the fine PGA — i.e., for long lines where the input signal level is at a minimum. For moderate to large input signals where only up to +14 dB of gain is needed and linearity is more important, it is recommended to employ the fine PGA first. Furthermore, to achieve maximum overall system noise performance, the high-voltage line receiver driving these inputs needs to be as low-noise as possible, while maintaining the required distortion performance.

The internal 0dB analog signal level and ADC full-scale reference level is 5 V peak-to-peak differential (2.5 V peak-to-peak single ended). Thus, if the chip RX input level exceeds 5 V peak-to-peak differential, the PGA must be programmed to provide attenuation.

The fourth order receive filter is implemented as a simple cascade of two second-order lowpass structures. The aggregate filter cutoff frequency is set as a function of ATU-R (1.1 MHz) or ATU-C (138 kHz or 276 kHz, depending on ISDN mode); these values are held to within ±5%. A halfband mode (552 kHz) exists in the ATU-R case to support lower-bandwidth ADSL variants (such as the emerging *G.lite* standard).

The response type of the filter also varies from ATU-R to ATU-C. In the ATU-R case, each of the two second-order stages has a true Butterworth lowpass response. In the ATU-C case, a fifth off-chip pole is desirable to increase rejection of out-of-band signals, and thus the on-chip filter has some peaking to compensate for any in-band loss. Specifically, the off-chip pole frequency should be 160 kHz (in non-ISDN mode), or 320 kHz (in ISDN mode). The resultant fifth-order structure (the off-chip pole plus the fourth-order on-chip filter) has an aggregate response that has a flat magnitude response, with a –3 dB frequency of 138 kHz (non-ISDN mode) or 276 kHz (ISDN mode). The actual implementation of the fifth pole is customer-dependent; it can be embedded within the hybrid, or placed within the high-voltage line receiver itself. The s-domain equations for the nominal RX filter transfer functions are as follows.

ATU-R RX: cascade of two 2nd-order Butterworth sections; aggregate cascade has –3 dB bandwidth at 1.104 MHz. In half-band mode, this response scales to 552 kHz.

$$H(s) = \frac{1}{(1 + 1.631 \times 10^{-7} s + 1.330 \times 10^{-14} s^2)^2}$$

ATU-C RX: cascade of two 2nd-order sections; yields a flat magnitude response having –3 dB bandwidth at 138 kHz when cascaded with an off-chip 160 kHz pole. One section has Q=1.1 to compensate for the off-chip pole.

$$H(s) = \frac{1}{(1 + 9.2579 \times 10^{-7} s + 1.0 \times 10^{-12} s^2) \times (1 + 1.4140 \times 10^{-6} s + 1.0 \times 10^{-12} s^2)}$$

In ISDN mode, this response scales in frequency by 2X and a 320-kHz off chip pole is required.

$$ISDN\ H(s) = \frac{1}{(1 + 4.6290 \times 10^{-7} s + 2.5 \times 10^{-13} s^2) \times (1 + 7.0711 \times 10^{-7} s + 2.5 \times 10^{-13} s^2)}$$

7.3.1 Receive Path Control Register 06H (RXGAIN)

The primary functionality is controlled by the RXGAIN register, as described below:

Register 06H (RXGAIN)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	PAA2	PAA1	PAA0	PGA4	PGA3	PGA2	PGA1	PGA0
Reset Value	0	0	0	0	0	1	1	1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name					PAA6	PAA5	PAA4	PAA3
Reset Value	0	0	0	0	0	0	0	0

☛WARNING NOTE ABOUT THE RXGAIN REGISTER:

After re-programming the gain registers, a minimum of one symbol time (250 μs) needs to be allowed for the ensuing transient to die away. During this 250 μs, the output of the ADC is invalid.

PGA[4:0]: Coarse PGA gain setting. –6 to +24 dB gain. 00000 = –6 dB, and 11111 = +24 dB (00111 is the default, at +12 dB). To achieve precise 6 dB steps, the 5-bit control word is thermometer encoded:

PGA[4:0]	Gain (dB)	Gain (Linear)
00000	–6 dB	0.5
00001	0 dB	1.0
00011	+6 dB	2.0
00111	+12 dB	4.0
01111	+18 dB	8.0
11111	+24 dB	16.0

Any other control values interpolate the gain between these values, in *linear* steps of 0.5. For example, a control word of 00100 (equal to 00011 + 1) yields a gain (linear scale) of 2.0 + 0.5, i.e., 2.5 (+7.96 dB). This can be represented by the equation given below.

$$\text{Gain (dB)} = 20 \log_{10} [\ 0.5 \text{ X } (\text{gain\_word} + 1)\ ]$$

PAA[6:0]: PAA (fine PGA) gain setting. 0 to +14 dB gain in 0.25 dB steps. 0000000= 0 dB (default is 0 dB). To achieve precision control of 0.25 dB steps in the gain, a very fine-grain control is provided, and the exact specification for the gain values is given below. It should be noted that the table lists only PAA[5:0], instead of PAA[6:0]. The MSB, PAA[6], yields an additional +6 dB of gain in the RXPAA if it is set to 1; this additional 6 dB is on top of the gain set by PAA[5:0]. As mentioned earlier, to maximize noise performance, it is far more preferable to place gain in the coarse PGA as opposed to the fine PGA. In particular, the final +6 dB (as set by PAA[6]) should only be utilized under the longest line conditions.

The fine PGA gain can be represented by the equation given below.

$$\text{Gain (dB)} = 20 \log_{10} [\ 0.0246825 \text{ X gain\_word} + 1\ ]$$

Programmable Gains for bits PAA[5:0]. Note: PAA[6]=1 gives an additional +6 dB.

PAA[5:0]	Gain	dB
000000	1	0
000001	1.0246	0.211
000010	1.0493	0.418
000011	1.0740	0.620
000100	1.0987	0.818
000101	1.1234	1.011
000110	1.1481	1.199
000111	1.1728	1.384
001000	1.1975	1.565
001001	1.2222	1.743
001010	1.2469	1.916
001011	1.2716	2.087
001100	1.2962	2.254
001101	1.3209	2.417
001110	1.3456	2.578
001111	1.3703	2.736
010000	1.3950	2.891
010001	1.4197	3.044
010010	1.4444	3.194

010011	1.4691	3.341
010100	1.4938	3.486
010101	1.5185	3.628
010110	1.5432	3.768
010111	1.5679	3.906
011000	1.5925	4.042
011001	1.6172	4.175
011010	1.6419	4.307
011011	1.6666	4.436
011100	1.6913	4.564
011101	1.7160	4.690
011110	1.7407	4.814
011111	1.7654	4.937
100000	1.7901	5.057
100001	1.8148	5.176
100010	1.8395	5.294
100011	1.8641	5.409
100100	1.8888	5.524
100101	1.9135	5.636
100110	1.9382	5.748
100111	1.9629	5.858
101000	1.9876	5.966
101001	2.0123	6.074
101010	2.0370	6.179
101011	2.0617	6.284
101100	2.0864	6.388
101101	2.1111	6.490
101110	2.1358	6.591
101111	2.1604	6.691
110000	2.1851	6.789

110001	2.2098	6.887
110010	2.2345	6.983
110011	2.2592	7.079
110100	2.2839	7.173
110101	2.3086	7.267
110110	2.3333	7.359
110111	2.3580	7.450
111000	2.3827	7.541
111001	2.4074	7.630
111010	2.4320	7.719
111011	2.4567	7.807
111100	2.4814	7.894
111101	2.5061	7.980
111110	2.5308	8.065
111111	2.5555	8.149

The gain versus code relationship for the RX PGA is shown graphically below.

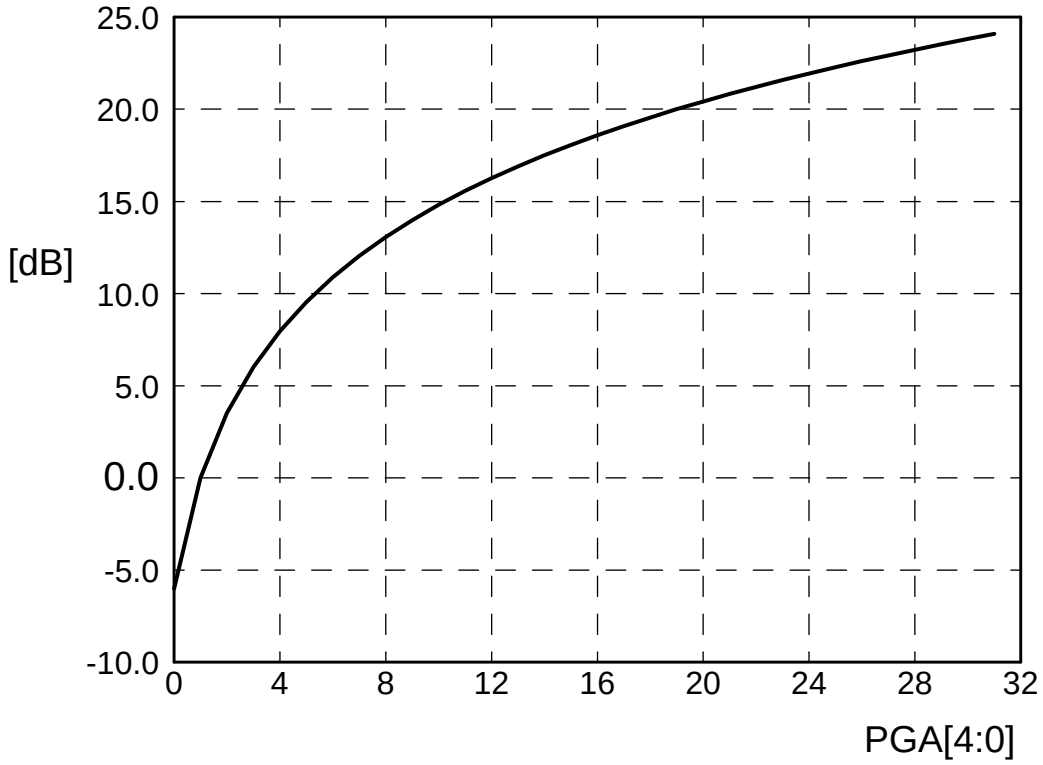


Fig. 3 Functional relationship between the first (coarse) PGA gain and register code.

The gain versus code relationship for the RX PAA is shown graphically below.

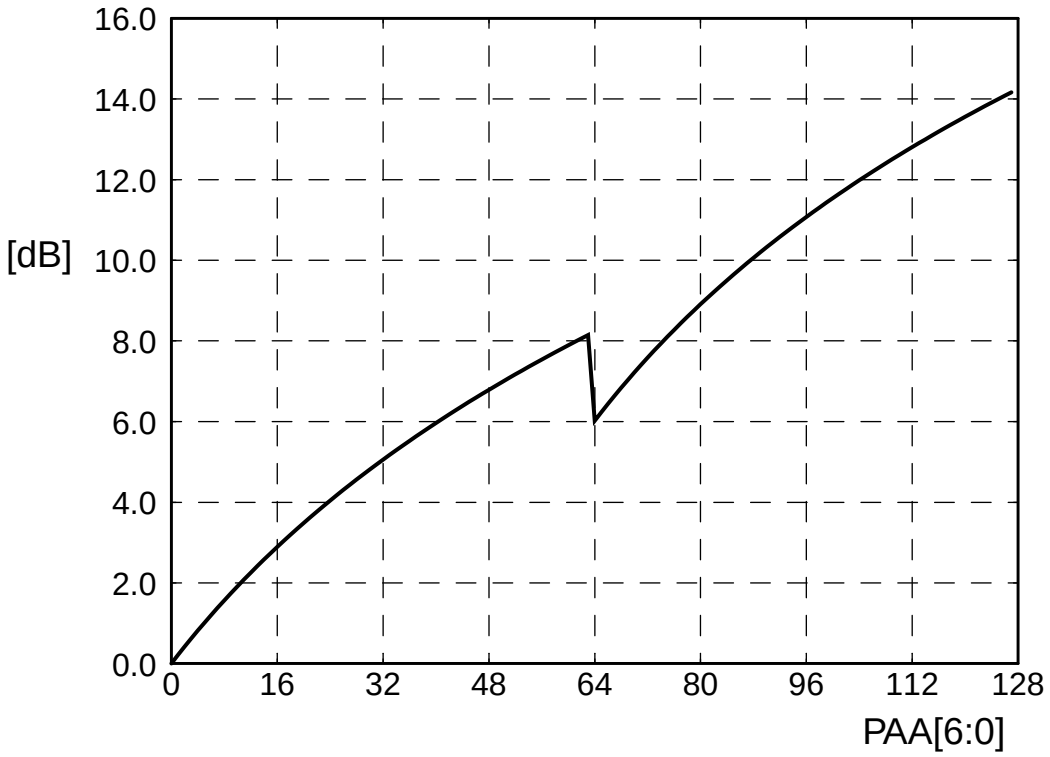


Fig. 4 Functional relationship between the second (fine) PGA gain and register code.

7.3.2 Receive Path Coarse High-Pass Filter

As well as the accurate low-pass filter described above in Section 7.3.0, the receive path has available an un-tuned high-pass filter consisting of two cascaded real high-pass poles, each at approximately 70 kHz. The composite 2nd-order high-pass corner is approximately 108 kHz. This filter can be engaged by setting bit 14 of register 0AH to 1. (Note that register 0AH is normally set to 0012H after initialization.) The tolerance on this high-pass cutoff frequency is approximately ±50%. Therefore, the pole should not be relied on for accurate band-edge control but is best used for purposes of additional out-of-band energy suppression.

7.4 Continuous-Time Blocks in TX Path

7.4.0 Introduction

The TX section continuous-time signal processing includes analog reconstruction filtering for the DAC, droop compensation, and fine control on the system transmit power. The TX section consists of two identical blocks, one for the primary transmit output and the other to provide echo functionality.

In a typical FDM ADSL system using non-overlapped upstream and downstream bands, the echo path is not used, and can be powered down.

The existence of the echo path affords the system designer several new degrees of freedom — modeling of the echo cancellation signal can be done adaptively on the transmit side, in the digital domain. Other approaches, such as a fixed analog compromise hybrid, are limited in their adaptability, and digital echo cancellation on the receive side incurs a large dynamic range penalty in the ADC. Of course, the system designer can revert to one of these more traditional methods of echo cancellation, with a concomitant reduction in power consumption in the chip. A high-level block diagram of the entire TX section is shown below:

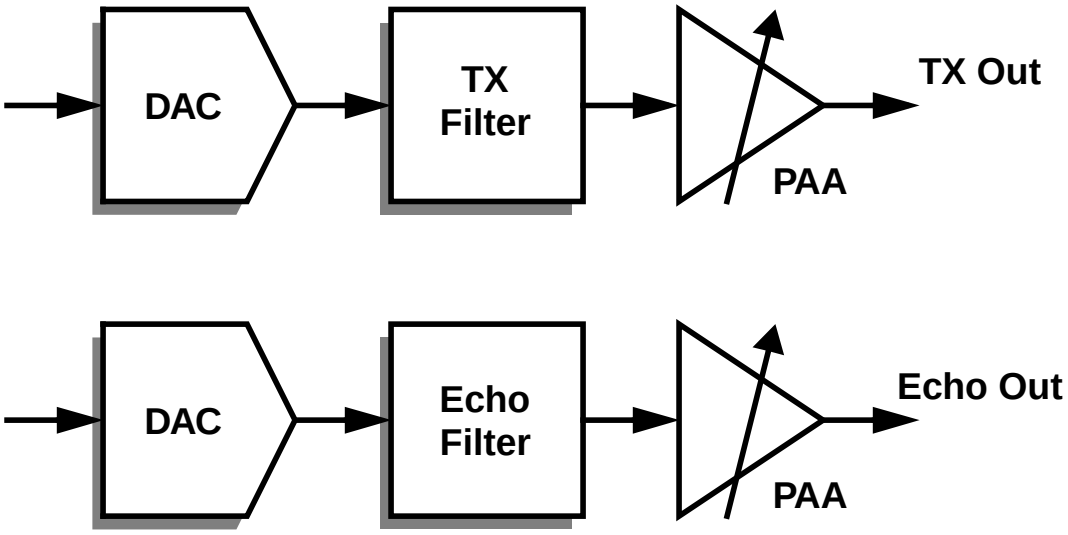


Fig. 5 Diagram showing major portions of the transmit and echo paths.

Like the receive filter, transmit filter's cutoff frequency is set as a function of ATU-C (1.104 MHz) or ATU-R (138 kHz or 276 kHz, depending on ISDN mode); these values are held to within ±5%. The response is a simple fourth-order lowpass, implemented as a pair of two second-order Butterworth structures. The s-domain equations for the nominal filter transfer functions are as follows.

ATU-C TX: cascade of two 2nd-order Butterworth sections; aggregate cascade has –3 dB bandwidth at 1.104 MHz.

$$H(s) = \frac{1}{(1 + 1.631 \times 10^{-7} s + 1.330 \times 10^{-14} s^2)^2}$$

ATU-R TX: cascade of two 2nd-order Butterworth sections; aggregate cascade has –3 dB bandwidth at 138 kHz. In ISDN mode, this response scales to 276 kHz.

$$H(s) = \frac{1}{(1 + 1.3046 \times 10^{-6} s + 8.5104 \times 10^{-13} s^2)^2}$$

Note that (a) for full compliance with the ITU G.992.1 and G.992.2 transmit PSD masks, additional off-chip filtering in the TX path is needed.

The outputs of both the transmit and echo signal paths are differential, with a peak signal swing of 5V peak-to-peak differential (2.5V peak-to-peak single-ended). It is recommended that the outputs be capacitively coupled into the subsequent high voltage line driver. For load-driving capability at maximum linearity, each output is designed to individually drive a resistance no smaller than 2 kΩ, and a capacitive load no greater than 10 pF.

Given the tight gain-control specification in the ADSL standard, gain accuracy in the entire transmit path is designed to be better than ± 0.5 dB about its nominal value. To improve absolute gain accuracy, as large of a load resistance (in excess of 5 kΩ) should be used. The nominal gain settings are described below.

7.4.1 Transmit Path Control Register 07H (TXGAIN)

The main functions of the TX path are controlled by the TXGAIN register.

Register 07H (TXGAIN)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ECPA7	ECPA6	ECPA5	ECPA4	ECPA3	ECPA2	ECPA1	ECPA0
Reset Value	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name	TXPA7	TXPA6	TXPA5	TXPA4	TXPA3	TXPA2	TXPA1	TXPA0
Reset Value	0	0	0	0	0	0	0	0

☞WARNING NOTE ABOUT THE TXGAIN REGISTER:

After re-programming the gain/attenuation registers in either the TX or ECHO paths, a minimum of one symbol period (250 μs) should be allowed for the ensuing transient to die away. During this time, both the TX path and ECHO path outputs are invalid, so that full-power transients cannot be emitted onto the twisted-pair line.

ECPA[7:0]: Echo path output attenuator gain setting. 0 to -24 dB attenuation in 1 dB steps. (default is 0 dB). Note that 00000000 corresponds to 0 dB attenuation, and 11111111 corresponds to –24 dB.

TXPA[7:0]: Transmit path output attenuator gain setting. 0 to -24 dB attenuation in 1 dB steps. (default is 0 dB). Note that 00000000 corresponds to 0 dB attenuation, and 11111111 corresponds to –24 dB.

The encoding for both TXPA[7:0] and ECPA[7:0] is as follows:

The upper 3 bits (TXPA[7:5] and ECPA[7:5]) encode the attenuation factor coarsely(0 to –18 dB in 6 dB steps), with the lower 5 bits (TXPA[4:0] and ECPA[4:0]) encoding the attenuation on a fine scale (0 to –6 dB in 1 dB steps).

In the upper 3 bits, the coarse attenuation control is quasi-thermometer encoded, as follows.

000 = 0 dB
100 = –6 dB
110 = –12 dB
111 = –18 dB

In the lower 5 bits, the fine attenuation control is quasi-binary encoded, as follows.

00000 = 0 dB
00100 = –1 dB
01000 = –2 dB
01101 = –3 dB
10011 = –4 dB
11001 = –5 dB
11111 = –6 dB

NOTE: this last case of -6 dB overlaps the coarse and fine control bits, but is required to achieve the complete -24 dB attenuation).

EXAMPLES OF USE OF THE TXGAIN REGISTER:

000 00000 ⟹ 0 dB coarse, 0 dB fine ⟹ 0 dB.
000 00100 ⟹ 0 dB coarse, –1 dB fine ⟹ –1 dB.
000 01000 ⟹ 0 dB coarse, –2 dB fine ⟹ –2 dB.
100 01101 ⟹ –6 dB coarse, –3 dB fine ⟹ –9 dB.
100 10011 ⟹ –6 dB coarse, –4 dB fine ⟹ –10 dB.
110 11001 ⟹ –12 dB coarse, –5 dB fine ⟹ –17 dB.
111 11111 ⟹ –18 dB coarse, –6 dB fine ⟹ –24 dB.

The TXPAA gain as a function of the TXPA[7:0] register code (0, 1, ..., 255) is given by the equation below.

$$Gain(dB) = 20\log 10\left[\frac{32 - 4 \times (code/32)}{32 + (code\%32)}\right]$$

where: (code / 32) in the numerator is integer division, and (code % 32) in the denominator is modulo.

The gain versus code relationship for both the TX PAA and EC PAA is shown graphically below.

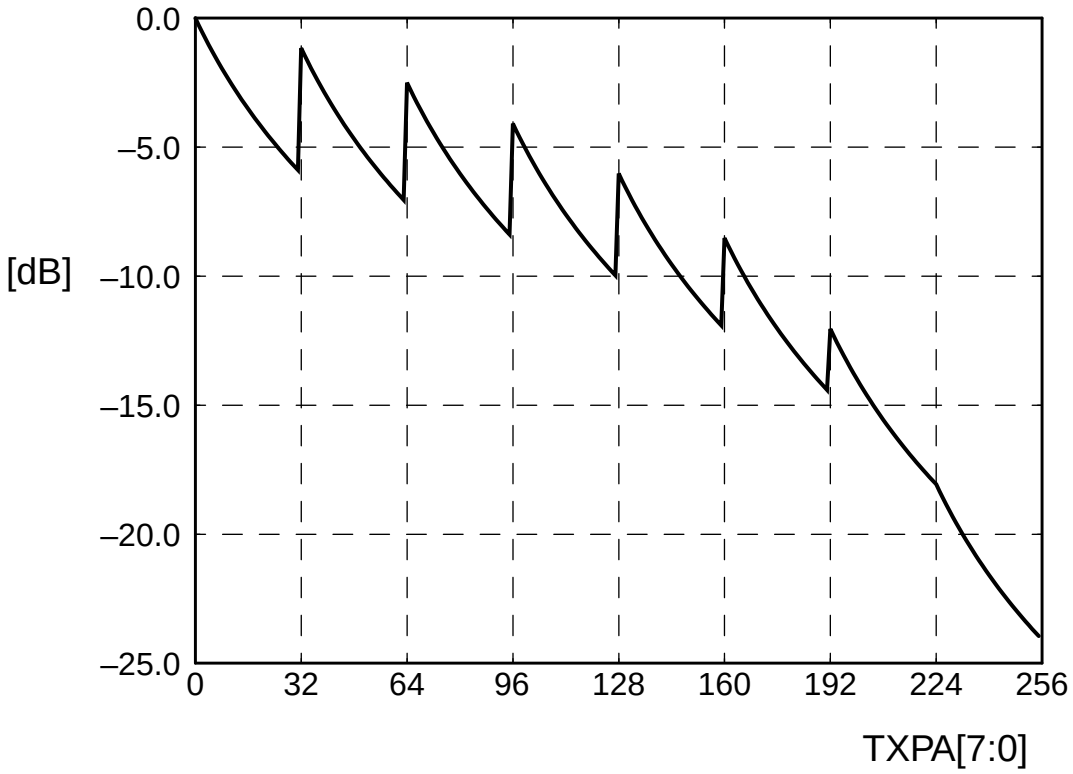


Fig. 6 Functional relationship between the TX and EC attenuation and register code.

7.4.2 Transmit Path Coarse High-Pass Filter

As well as the accurate low-pass filter described above in Section 7.4.0, the transmit path has available an un-tuned high-pass filter consisting of one real high-pass pole at approximately 70 kHz. This filter can be engaged by setting bit 6 of register 0AH to 1. (Note that register 0AH is normally set to 0012H after initialization.) The tolerance on this high-pass cutoff frequency is approximately ±50%. Therefore, the pole should not be relied on for accurate band-edge control but is best used for purposes of additional out-of-band energy suppression.

7.5 ADC

7.5.0 Introduction

The output of the RX filter is fed directly to the ADC. As described earlier, the chip requires a single low-jitter clock to be applied at the REFCLK pin. All clock generation is performed internally and the ADC clock is directly derived from REFCLK. The ADC sampling rate is set by the CLK[1:0] bits in the MODE register to be either 4.416 MS/s or 2.208 MS/s. Note that REFCLK must *always* be either 4.416 MHz or 8.832 MHz; any required divided down clocks are generated internally.

7.5.1 ADC Digital Output Timing

The chip implements a simple interface: the 16 ADC outputs appear on the AD15,...AD0 pins as a parallel word synchronous with the ADC sampling clock. AD0 is the LSB and AD15 is the MSB. The timing diagram for the ADC digital outputs is shown in Fig. 7. The figure shows the case where the ADC sampling clock is at the same frequency as REFCLK.

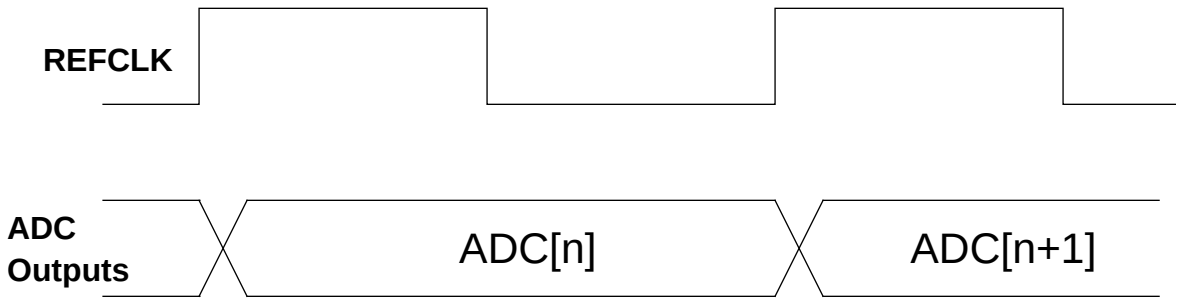


Fig. 7 Timing diagram for ADC outputs.

The data changes on the rising edge of REFCLK and can be latched by a DSP on the falling edge. In the cases where the ADC sampling rate is less than REFCLK, the above timing relationships still hold, with the ADC data changing on every second or every fourth clock edge, as appropriate. The latency through the ADC from the filter output to the digital outputs is 6 clock cycles of the ADC clock. The voltage levels on the AD15,...,AD0 lines are CMOS levels: the HIGH level is determined by the power supply voltage on the VDD_ADIO pins, which can be set independently of the other supply pins on the chip. Typically, VDD_ADIO should be +3.3V: this ensures that the ADC outputs are both TTL-compatible and 3.3V-CMOS compatible.

7.5.2 ADC References

The ADC full scale range is set by reference voltages generated on chip. These two reference voltages appear on pins ADC_REFP and ADC_REFM; nominally their difference is 2.5 V. The ADC_REFP and ADC_REFM pins should be very carefully decoupled on the board using a 10 μF low-ESR capacitor and as short a trace as possible. Some optimization of the decoupling may be required, as shown in Fig. 8.

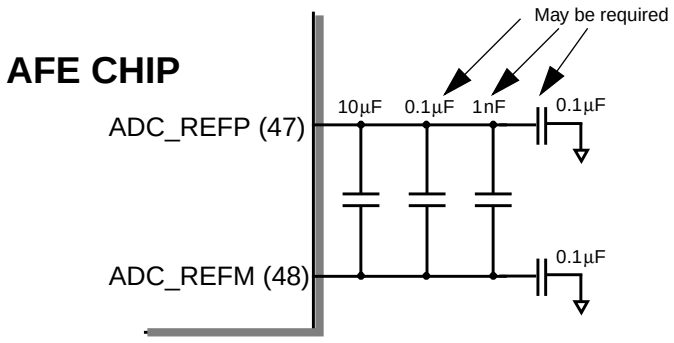


Fig. 8 Recommended connection of pins ADC_REFP and ADC_REFM.

ADC range adjustment:

The default value of the ADC reference is 2.5 V single-ended. However, some adjustment is possible using register bits REFADC[1:0] located in register 0FH (MISC1), bits 5 and 4.

MISC1[5:4] = REFADC[1:0]

- 00: ADC differential-mode reference = 2.5 V (nominal = 100%, default value)
- 01: ADC differential-mode reference = 2.1875 V (87.5%)
- 10: ADC differential-mode reference = 3.0 V (125%)
- 11: ADC differential-mode reference = 2.8125 V (112.5%)

Note that full linearity is not guaranteed outside the nominal reference setting, and the 125% setting especially should be used with caution.

7.5.3 Other ADC Functions

OUTPUT ENABLE:

The ADC digital outputs are enabled by the active low output enable pin (OEB).

- OEB = 0: ADC digital outputs AD15,...,AD0 are enabled
- OEB = 1: ADC digital outputs AD15,...,AD0 are high-impedance (tristated).

FORMAT:

The format of the ADC digital data is controlled by the TWOS bit (bit 10 in the CALC register), which was tabulated in Section 7.2.3.

- 0: AD15,...,AD0 uses unsigned format
- 1: AD15,...,AD0 uses twos' complement format

7.6 DAC

7.6.0 Introduction

The DAC accepts a 16-bit word at the DA15,...,DA0 pins and generates an analog signal for the continuous time blocks in the TX path.

7.6.1 DAC Digital Input Timing

The timing diagram for the DAC input digital data when the echo path is not used is given below in Fig. 9. In this case, AUXCLK (pin 5) is not used and should be tied to GND.

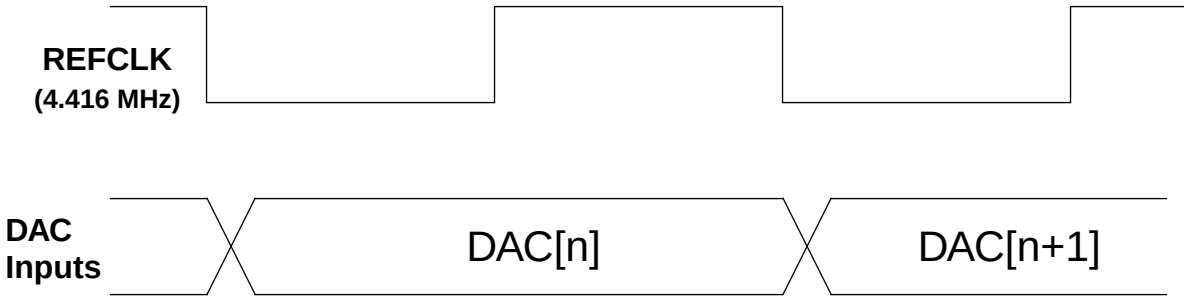


Fig. 9 Timing diagram for DAC digital inputs.

The IC expects the incoming digital data to change at the falling edge of REFCLK and the data is latched internally on the rising edge. Thus, the data should be stable at the rising edge.

The timing diagram for the DAC input for the case when both echo and TX paths are used is given below in Fig. 10.

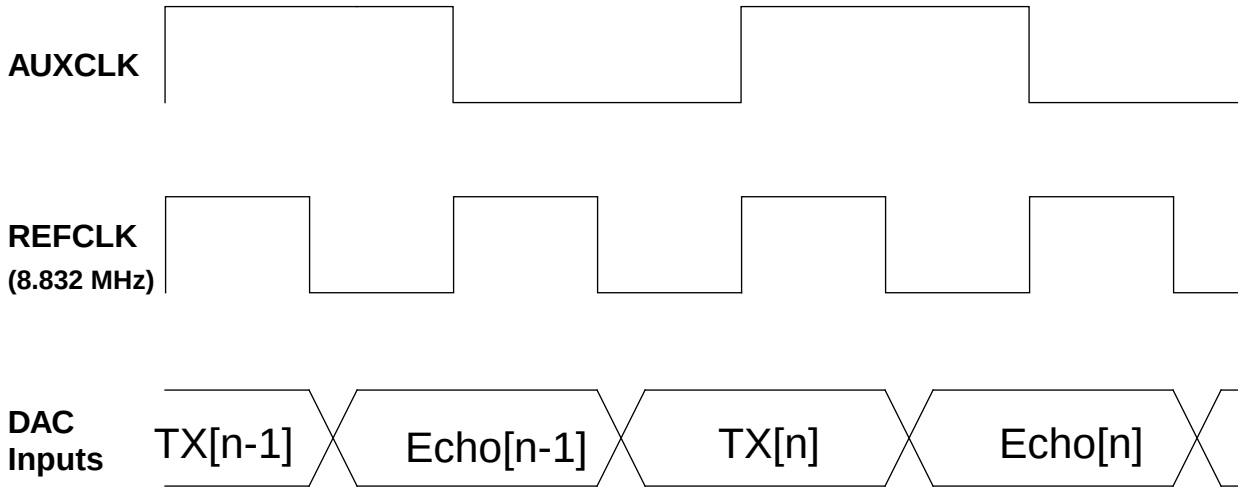


Fig. 10 Timing diagram for DAC digital inputs (DA15,...,DA0) with echo path and TX path both used.

Note that AUXCLK must change on the rising edge of REFCLK. The value of AUXCLK is latched internally on the falling edge of REFCLK. The IC expects the incoming digital data to change at the falling edge of REFCLK and is latched internally on the rising edge. Thus, the data should be stable at the rising edge. The latency through the DAC from the rising edge of REFCLK at which the incoming digital data is latched to the instant when the analog sample is transferred to the filter is 5 periods of the REFCLK clock. Detailed information on setup/hold times is given in Section 8 of this document.

☞WARNING NOTE ABOUT THE TX/ECHO TIMING:

Note: BIT 3 of the MODE register must be set to 1 for the TX/Echo data timing to work as shown above. With BIT 3 set to 0 (default condition), the TX/Echo ordering with respect to AUXCLK is swapped.

7.6.2 DAC References

The DAC full scale range is set by reference voltages generated internally on chip. These two reference voltages appear on pins DAC_REFP and DAC_REFM. As in the case of the ADC references, these two pins should be very carefully decoupled on the board using a 10 µF (or higher) low-ESR capacitor and using traces as short as possible. Some optimization of the decoupling may be required, as shown in Fig. 11.

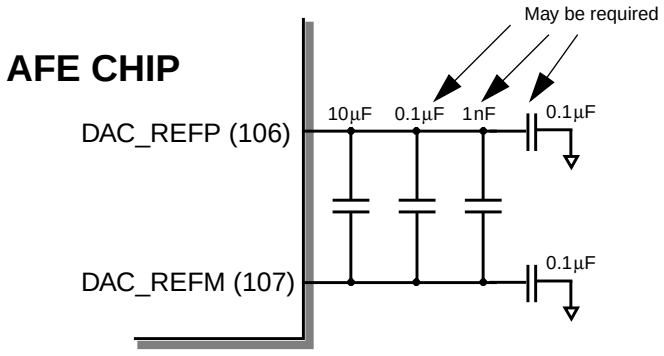


Fig. 11 Recommended decoupling for pins DAC_REFP and DAC_REFM.

DAC range adjustment:

The default value of the DAC reference is 2.5 V single-ended. However, some adjustment is possible using register bits REFDAC[1:0] located in register 0FH (MISC1), bits 7 and 6.

MISC1[7:6] = REFDAC[1:0]

00: DAC differential-mode reference = 2.5 V (nominal = 100%, default value)
01: DAC differential-mode reference = 2.1875 V (87.5%)
10: DAC differential-mode reference = 3.0 V (125%)
11: DAC differential-mode reference = 2.8125 V (112.5%)

Note that full linearity is not guaranteed outside the nominal reference setting, and the 125% setting especially should be used with caution.

7.7 Serial Port Interface

7.7.0 Introduction

The serial port interface controls the read/write to the registers on the chip. The interface consists of an active-low enable input pin (S_EN), a serial clock input pin (S_CLK), a data input pin (S_DIN) and a data output pin (S_DOUT). The timing diagram of the operation of the serial port is shown in Fig. 12. After S_EN is asserted, chip-selects (CS1, CS0), serial port register address (A4-A0) and read/write control bit ($\overline{R}$/W) are serially clocked in at the rising edge of S_CLK. For a write operation ($\overline{R}$/W=1), the addressed register is updated upon receiving the 16-bit write data (D15-D0). For a read operation ($\overline{R}$/W=0), the 16-bit contents of the addressed register is sequentially shifted out at the S_DOUT pin at the falling edge of S_CLK. As shown in Fig. 12, S_DOUT is driven only when data are being read. Otherwise, it is tristated.

7.7.1 Serial Port Timing

The timing diagram for the serial port is shown in Fig. 12.

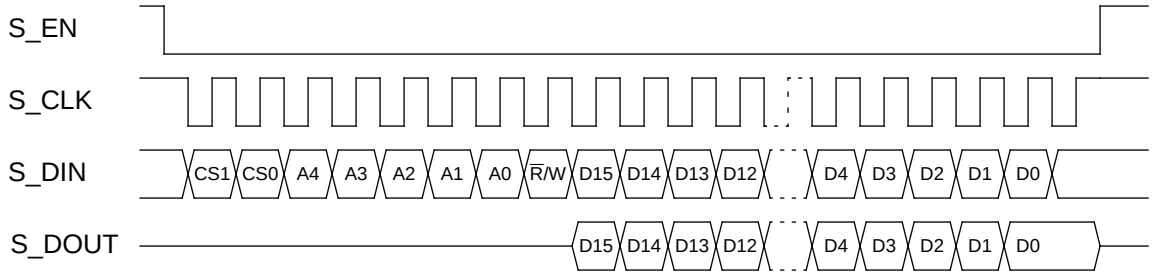


Fig. 12 Timing diagram for the serial port

Detailed information on setup/hold times is given in Section 8 of this document.

7.8 Support Blocks

7.8.0 Introduction

The support blocks on the chip consist of a voltage-mode DAC to drive an external voltage-controlled crystal oscillator (VCXO), and (b) some general purpose digital outputs.

7.8.1 VCXO Control Register 0DH (VCXO)

The VCXO DAC is 12-bit voltage-mode DAC designed to be monotonic and intended to be operated at a 4 kHz update rate. It can source or sink up to 10 μA of dc current. In order to update the DAC, the user must write to the VCXO register through the serial port. The individual bit definitions are given below.

Register 0DH (VCXO)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	VCX7	VCX6	VCX5	VCX4	VCX3	VCX2	VCX1	VCX0
Reset Value	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name					VCX11	VCX10	VCX9	VCX8
Reset Value	0	0	0	0	1	0	0	0

VCX[11:0]: VCXO DAC 12-bit word. The DAC nominal output voltages for extreme and mid-scale codes are as follows.

VCXO[11:0] = 000000000000 = 000H: 0.5 V above GND
VCXO[11:0] = 100000000000 = 800H: 2.25 V above GND (mid-range)
VCXO[11:0] = 111111111111 = FFFH: 4.0 V above GND

A general expression for the DAC output voltage is

0.5 V + (CODE / 4096) X (3.5 V)

where *CODE* is the decimal integer value of the 12-bit word formed by VCXO[11:0].

7.8.2 Miscellaneous Functions Register (MISC1)

The MISC1 register contains the general purpose I/O bit definitions.

Register 0FH (MISC1)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	REFDAC1	REFDAC0	REFADC1	REFADC0				
Reset Value								
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Name			GP5	GP4	GP3	GP2	GP1	GP0
Reset Value								

Register bits GP[5:0]:

The values in GP[5:0] appear directly at the pins GP5,...,GP0 (103-101, and 67-65) as 5-V CMOS digital levels and are available to the user.

Bits REFDAC[1:0] and REFADC[1:0] were described earlier in the DAC and ADC sections.

7.9 Miscellaneous Interface and External Component Connections

EXTERNAL RESISTOR CONNECTIONS:

The connections to the two groups of pins {REXT_TX, TXBGCAP, TX_RESRTN} and {REXT_RX, RXBGCAP, RX_RESRTN} are critical and should be routed very carefully on the board. The connections are as shown in Fig. 13 below. The traces to/from these pins should be as short as possible.

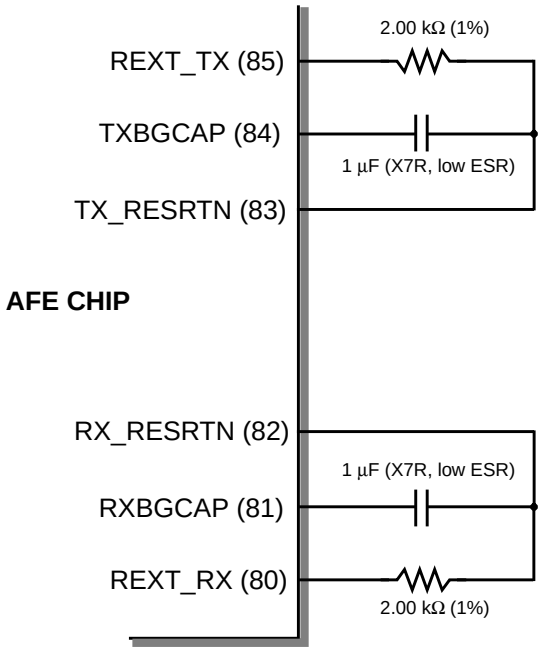


Fig. 13 Recommended connection for pins 80-85. Note that the RX_RESRTN pin is also used for decoupling of the RXCMIN pin, as shown previously in Fig. 2.

GENERAL GUIDELINE FOR CONNECTION OF DIGITAL INPUTS:

In general, all digital inputs on the chip should be connected to a low impedance (either +3.3 V, +5.0 V or GND). Leaving digital inputs floating may result in unreliable behavior — the digital inputs do not have internal pull-up or pull-down resistors. Specifically, this applies to the following pins on the chip:

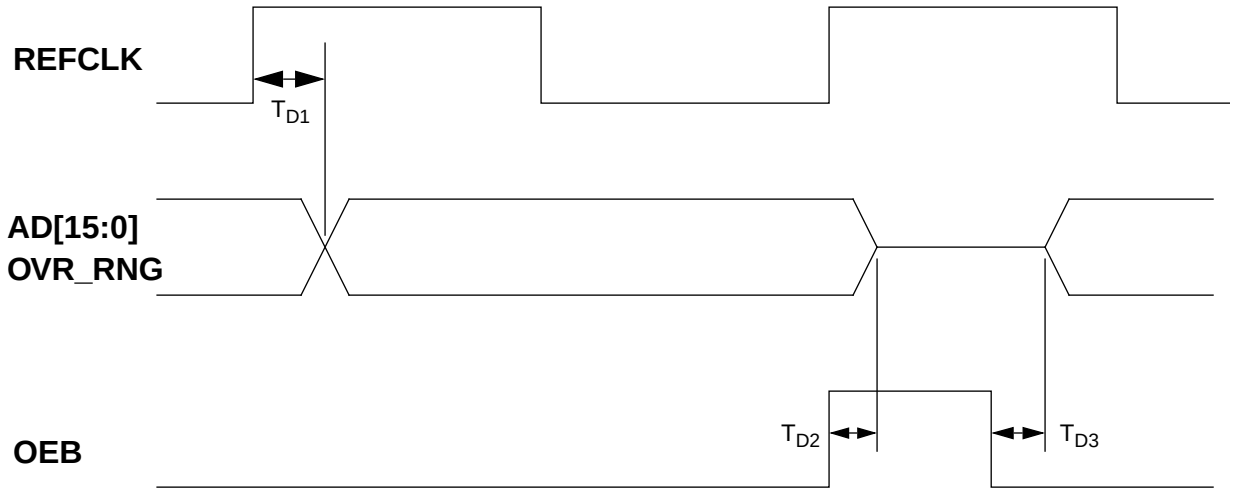
DA15,...,DA0, AUXCLK, OEB, REFCLK, S_CLK, S_EN, S_DIN, RESETB, CS1, CS0.

8 Timing Specifications

8.1 Overview

This section gives detailed timing specifications for the various digital interfaces on the chip.

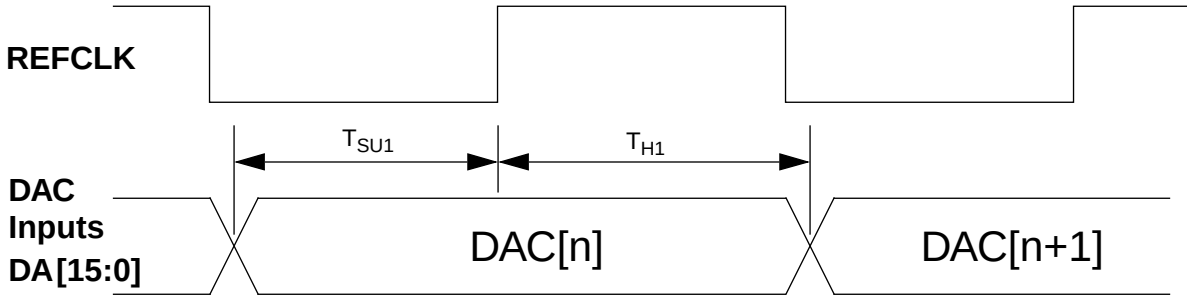
8.2 ADC



Parameter	Symbol	Min	Typ	Max	Units
REFCLK high to Data Valid	T_{D1}			30[a]	ns
OEB inactive to HiZ	T_{D2}			20	ns
OEB active to Data Valid	T_{D3}			20	ns

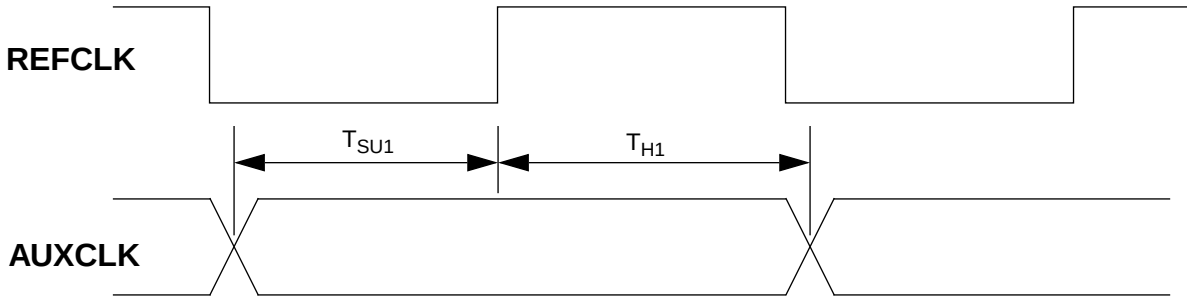
a. Conditions: load capacitance = 20 pF, VOH = 3.3 V

8.3 DAC



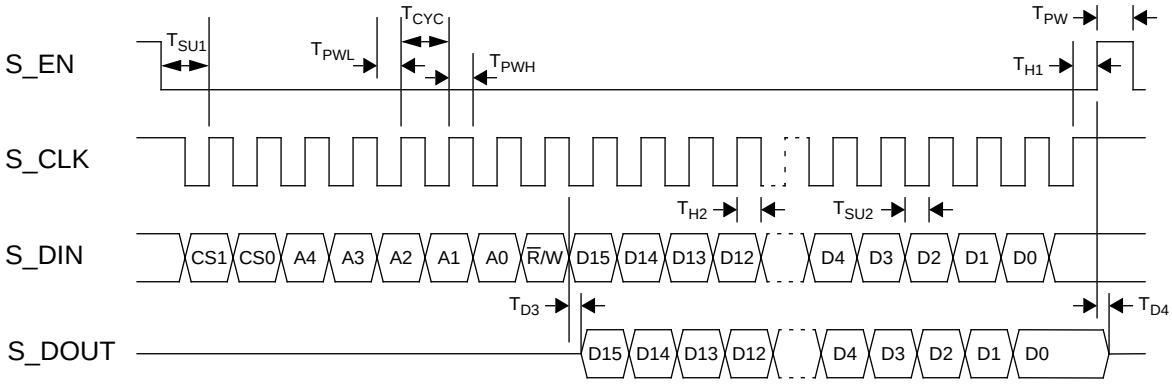
Parameter	Symbol	Min	Typ	Max	Units
DAC inputs setup time	T_{SU1}	15			ns
DAC inputs hold time	T_{H1}	15			ns

AUXCLK Timing in Echo Mode



Parameter	Symbol	Min	Typ	Max	Units
AUXCLK input setup time	T_{SU1}			20	ns
AUXCLK input hold time	T_{H1}			20	ns

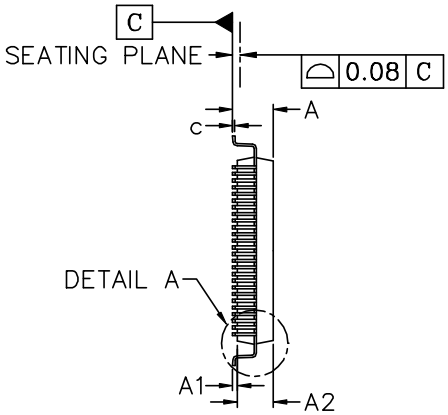
8.4 Serial Port

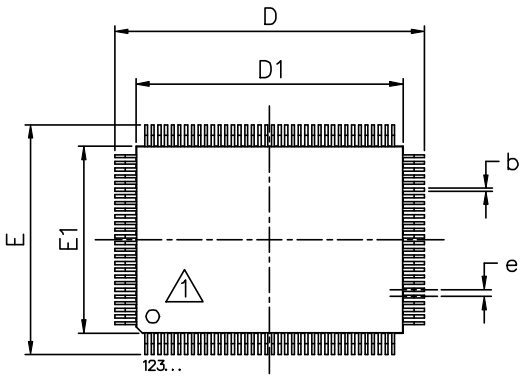


Parameter	Symbol	Min	Typ	Max	Units
S_CLK clock period	T_{CYC}	100	125		ns
S_CLK high time	T_{PWH}	50			ns
S_CLK low time	T_{PWL}	50			ns
S_EN low to S_CLK high	T_{SU1}	30			ns
S_CLK high to S_EN high	T_{H1}	15			ns
S_EN inactive pulse width	T_{PW}	100			ns
S_DIN setup time	T_{SU2}	15			ns
S_DIN hold time	T_{H2}	15			ns
S_CLK low to S_DOUT delay	T_{D3}			30[a]	ns
S_EN inactive to S_DOUT HiZ	T_{D4}			30	ns

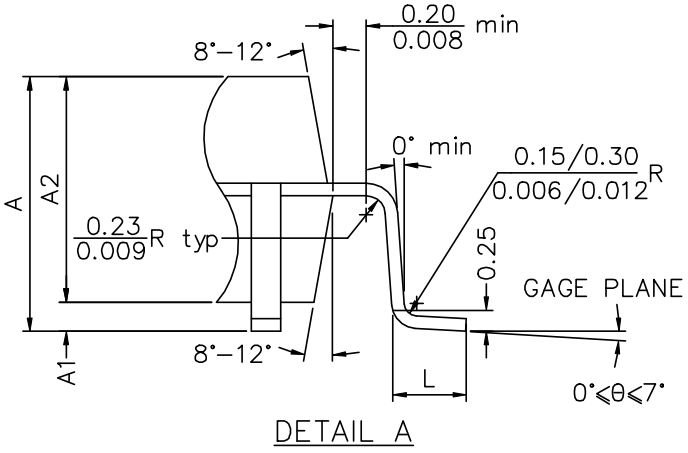
a. Conditions: load capacitance = 30 pF, VOH = 5.0 V

9 Package Drawing





SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.85	3.05	3.25	.112	.120	.128
A1	0.25	0.35	0.45	.010	.014	.018
A2	2.60	2.70	2.80	.102	.106	.110
D	22.95	23.20	23.45	.904	.913	.923
D1	19.90	20.00	20.10	.783	.787	.791
E	16.95	17.20	17.45	.667	.677	.687
E1	13.90	14.00	14.10	.547	.551	.555
L	0.73	0.88	1.03	.029	.035	.041
e	0.50			.0197		
b	0.17	0.22	0.27	.007	.009	.011
c	0.13	0.16	0.20	.005	.006	.008



NOTE: 1. PIN 1 INDICATOR.

2. REFER TO JEDEC OUTLINE MS–029 KA FOR DATUMS, FEATURES AND DIMENSIONS NOT SHOWN. KA VARIATION HAS 38 AND 26 LEADS ON SIDE D AND E RESPECTIVELY.

3. CONTROLLING DIMENSION IN MM.

Appendix A Document Revision History

V1.1.1 (01/20/2000)

- Tolerances of coarse high-pass filters available in RX path and TX path changed in Sections 7.3.2 and 7.4.2, respectively.
- Contact addresses and phone numbers on title page updated.

V1.1.0 (09/15/99)

- Description of coarse high-pass filters available in RX path and TX path added in Sections 7.3.2 and 7.4.2, respectively.
- Description of ADC and DAC range programmability added in Sections 7.5.2 and 7.6.2, respectively.

V1.0.1 (09/03/99)

- Minor typo fixes.
- Resistor values corrected on Fig. 13.

V1.0.0 (08/07/99)

- First version