

DP8482A 100k ECL to TTL Level Translator with Latch

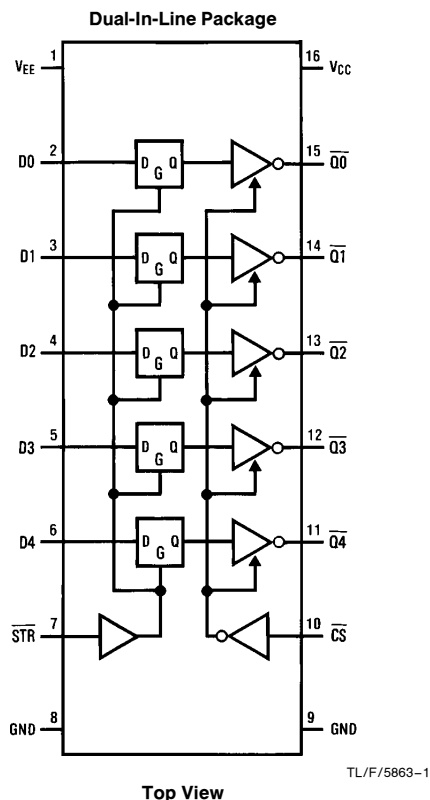
General Description

This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive standard 50 pF loads. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin DIP or S.O.
- TRI-STATE outputs
- ECL control inputs
- 8 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 100k ECL input compatible

Logic and Connection Diagram



Truth Table

D	\bar{Q}	\overline{STR}	\overline{CS}
H	L	L	L
L	H	L	L
X	\bar{Q}	H	L
X	Hi-Z	X	H

H = high level (most positive)

L = low level (most negative)

X = don't care

Order Number DP8482AJ, DP8482AM or DP8482AN
See NS Package Number J16A, N16A or M16B

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V _{EE} Supply Voltage	−8V
V _{CC} Supply Voltage	7V
Input Voltage	GND to V _{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW

Storage Temperature −65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V _{EE} Supply Voltage	−4.5V ± 7%
V _{CC} Supply Voltage	5.0V ± 10%
T _A , Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{OL}	Output Low Voltage	I _{OL} = 12 mA			0.5	V
V _{OH}	Output High Voltage	I _{OH} = −10 mA	V _{CC} − 2V			V
I _{AV}	Output Low Drive Current	Force 2.5V	70	150		mA
I _{OS}	Output High Drive Current	Force 0V	−70	−150	−350	mA
I _{OZ}	TRI-STATE Output Current		−50	1	+ 50	μA
I _{CC}	Supply Current				35	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	T _A	Min	Typ	Max	Units
V _{IL}	Input Low Voltage	V _{EE} = −4.5V		−1810		−1475	mV
V _{IH}	Input High Voltage	V _{EE} = −4.5V		−1165		−880	mV
I _{IL}	Input Low Current	V _{IN} = V _{IL} Max			50	100	μA
I _{IH}	Input High Current	V _{IN} = V _{IH} Max			75	750	μA
I _{EE}	Supply Current					−55	mA

Switching Characteristics (Notes 2 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{PD1}	Strobe to Output Delay	C _L = 50 pF	4	9	15	ns
t _{PD2}	Data to Output Delay	C _L = 50 pF	3.5	8	15	ns
t _S	Data Set-Up Time	(Note 6)	3.0	1.0		ns
t _H	Data Hold Time	(Note 6)	3.0	1.0		ns
t _{PW}	Strobe Pulse Width	(Note 6)	5.0	3.0		ns
t _{ZE}	Delay from Chip Select to Active State from Hi-Z State	C _L = 50 pF	6	15	25	ns
t _{EZ}	Delay from Chip Select to Hi-Z State from Active State	C _L = 50 pF	4.5	12	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply. Maximum propagation delays are specified with all outputs switching simultaneously.

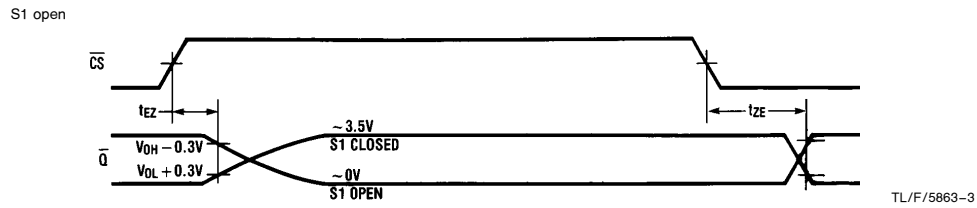
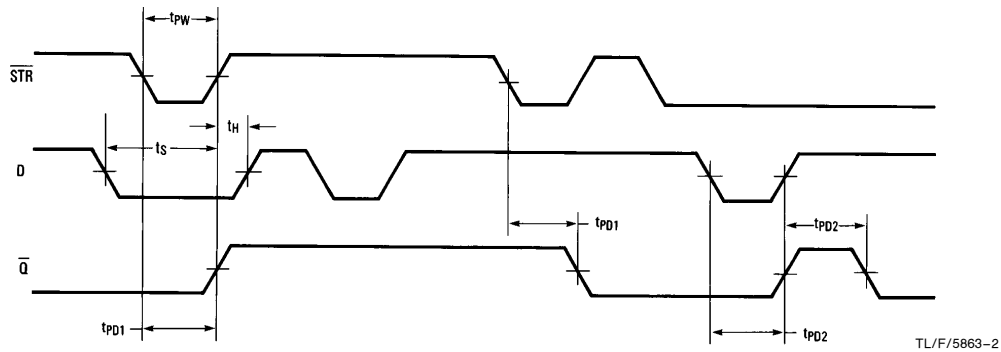
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: When DC testing I_{AV} or I_{OS}, only one output should be tested at a time and the current limited to 120 mA max.

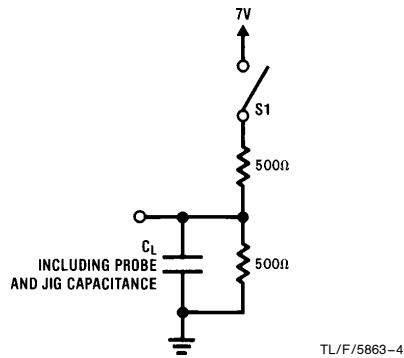
Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 0.7 ns ± 0.1 ns from 20% to 80%.

Note 6: Caution should be used when latching data while the outputs are switching. TTL outputs generate severe ground noise when switching. This noise can be sufficient to cause the ECL latch to lose data. Board mounting and good supply decoupling are desirable. The worst case conditions are with all outputs switching low simultaneously, the maximum capacitive loading on the outputs and the maximum V_{CC} supply voltage applied.

Switching Time Waveforms



Test Load



Typical Performance Versus C_L

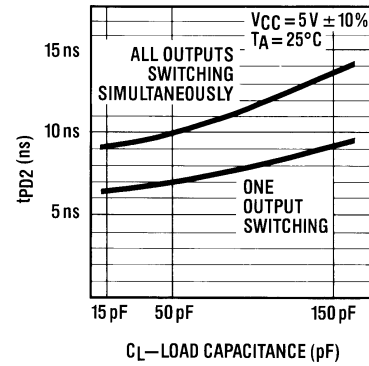
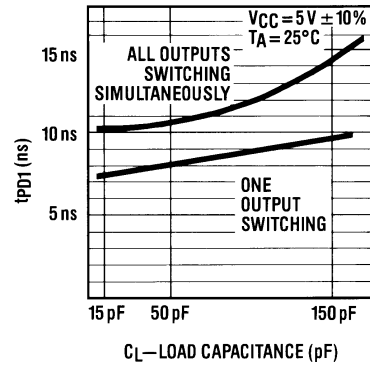
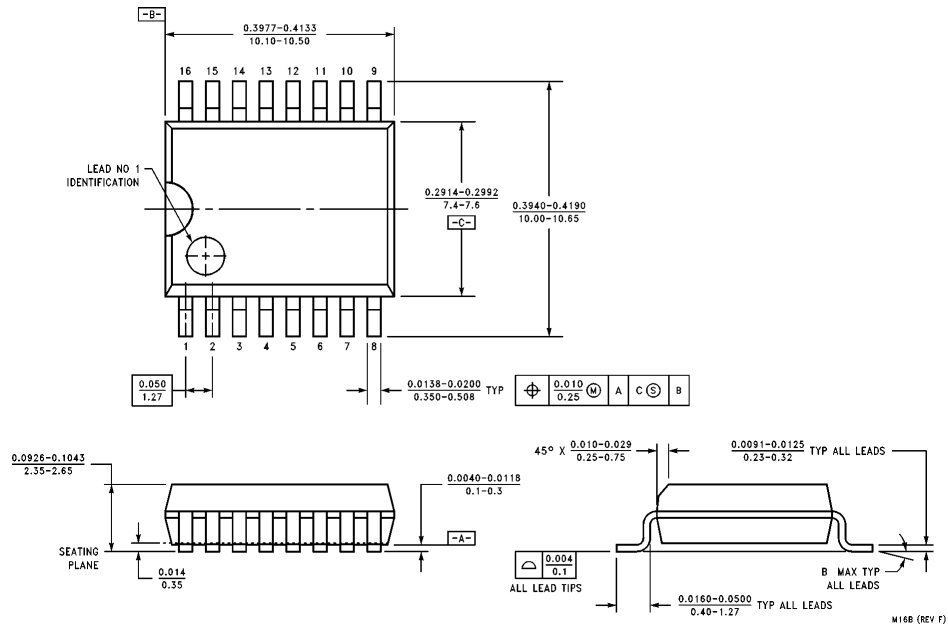


Figure 1: Mechanical drawing of the J16A connector. The drawing includes three views: a top view, a side view, and a cross-sectional view. The top view shows a rectangular connector with 16 pins on one side and 9 pins on the other. Dimensions include a total length of 0.785 [19.94] MAX, a pin pitch of 0.037 ± 0.005 [0.94 ± 0.13] TYP, and a pin diameter of 0.020 [0.51-1.52] TYP. The side view shows a height of 0.220-0.310 [5.59-7.87] and a pin height of 0.005 [0.13] MIN TYP. The cross-sectional view shows a glass sealant and a pin with a diameter of 0.180 [4.57] MAX and a height of 0.310-0.410 [7.87-10.41].

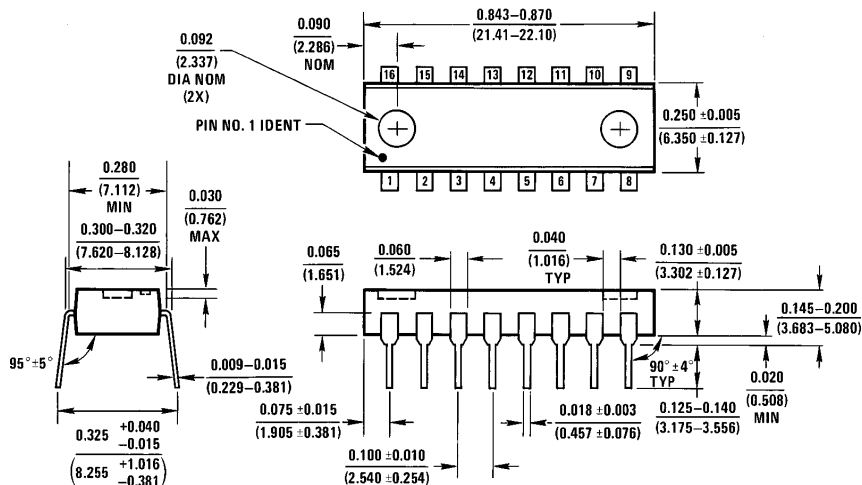
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Physical Dimensions inches (millimeters) (Continued)



Order Number DP8482AM
NS Package Number M16B

W16B (REV F)




Molded Dual-In-Line Package (N)
Order Number DP8482AN
NS Package Number N16A

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