DL6000™ Family

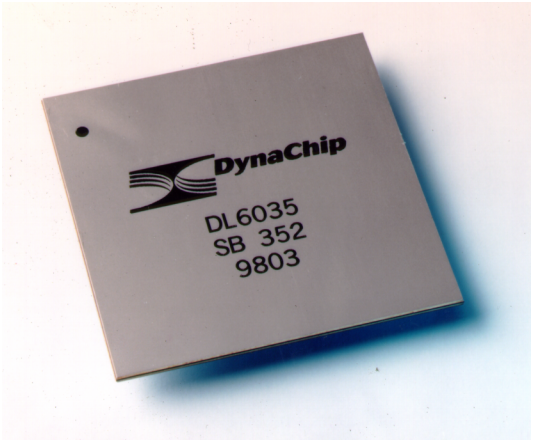
Fast Field Programmable Gate Array™

Features

- System Clock Rates Up To 200 MHz
- 9,000 to 105,000 Usable Gates
- Synchronous Dual-port RAM with 8 ns Access Time
- 2 Analog PLLs For Clock Multiplication, Division and Locking
- LV-TTL and GTL Interface Levels
- Up to 10 LVDS Compatible Inputs
- Up to 10 Differential or Single-Ended LV-PECL Inputs
- 1.3 ns Input Register Setup Time
- 33/66 MHz PCI Compatible
- Partial Reconfiguration
- 10 Clock Trees with 150 ps Skew
- 3.3 Volt Operation
- 5 Volt Tolerant I/O
- Patented Active Repeater Architecture
- In-System Reprogrammability (ISP)
- JTAG Support
- Output Slew Rate Control
- Fully Automatic Implementation With DynaTool™

Applications Examples

- Telecommunication
- Datacommunication
- High Speed Graphics
- DSP
- ASIC Emulation



Introduction

The DL6000 is DynaChip's second generation Fast Field Programmable Gate Array family. Built on a deep sub-micron CMOS process, this family supports applications with system clock rates up to 200 MHz.

The DL6000 family features DynaChip's patented Active Repeater Architecture. This results in extremely short routing delays allowing these devices to run at system frequencies well above conventional FPGAs.

To support the fast data rates of high-speed applications, every I/O pin can be programmed to LV-TTL or GTL interface levels.

DL6000 family devices contain synchronous RAM with 8 ns access time. These flexible RAM structures operate in true dual and single port modes and are ideal for applications that require fast access to memory.

High operating frequencies, on-chip RAM, fast I/O and PCI compatibility make these devices ideal for high-speed telecommunications, datacommunications, graphics and emulation applications.

The DL6000 features SRAM-based programming allowing the devices to be configured in-circuit and reprogrammed on-the-fly. They support dynamic single-block reconfiguration enabling a portion of the device to be reprogrammed without affecting operation of the remaining logic.

Device	Gates	Logic Blocks	Max User RAM Bits	Flip Flops	Clock Trees	I/O Blocks
DL6009	9,000	256	8,192	768	10	128
DL6020	20,000	576	18,432	1,536	10	192
DL6035	35,000	1,024	32,768	2,560	10	254
DL6055	55,000	1,600	51,200	3,840	10	320
DL6080	80,000	2,304	73,728	5,376	10	384
DL6105	105,000	3,136	100,352	7,168	10	448

Table 1: DL6000 Family

Table of Contents

Performance Examples

The DL6000 family with DynaChip's patented Active Repeater Architecture supports high-speed applications with clock rates up to 200 MHz.

The following table shows the performance of various size functions implemented in the DL6035*.

Circuit	DL6035 - G	Logic Block Count
8-bit Fully Synchronous, Loadable Up Counter	145 MHz	9
16-bit Fully Synchronous, Loadable Up Counter	140 MHz	20
32-bit Fully Synchronous, Loadable Up Counter	125 MHz	42
64-bit Fully Synchronous, Loadable Up Counter	100 MHz	86
32x32 RAM-based FIFO	100 MHz	49
128x32 RAM-based FIFO	80 MHz	145
64-bit Shift Register	160 MHz	64
Maximum chip-to-chip performance**	250 MHz	-

Table 2: Performance of Various Applications

* Based on -G speed grade over commercial voltage and temperature range.
** With 10 pF load and fast slew rate.

High Performance Active Repeater Technology

The enabling technology behind DynaChip's Fast Field Programmable Gate Arrays is the Active Repeater. Conventional FPGA devices use pass gates to create programmable interconnections. These pass gates act like a series of resistors with distributed capacitance to ground. Nets formed out of these pass gates slow down dramatically as the number of programmable connections increases.

This results in long, unpredictable delays, especially for nets that have to travel a long distance or drive a large number of loads.

In contrast, DynaChip uses Active Repeaters to create programmable interconnections. As shown in figure 1, these repeaters buffer the signal at every interconnection point and isolate the capacitance of the rest of the net.

The result is fast, predictable performance even for long, high fanout nets.

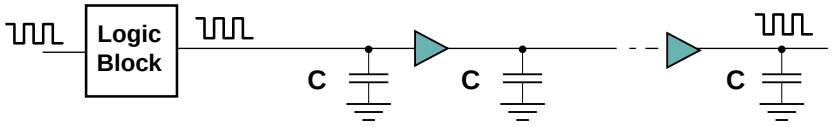


Figure 1: DynaChip's Active Interconnect

In FPGA devices that use pass-gate based interconnect, net delays increase quadratically with the number of programmable interconnect points, as shown in figure 2. This results in a performance bottleneck that is especially troublesome for nets that have to travel a long distance or drive a large number of loads.

In devices that use Active Repeaters for interconnect, net delays are linear and are not affected by fanout. The result is much higher performance and greater predictability.

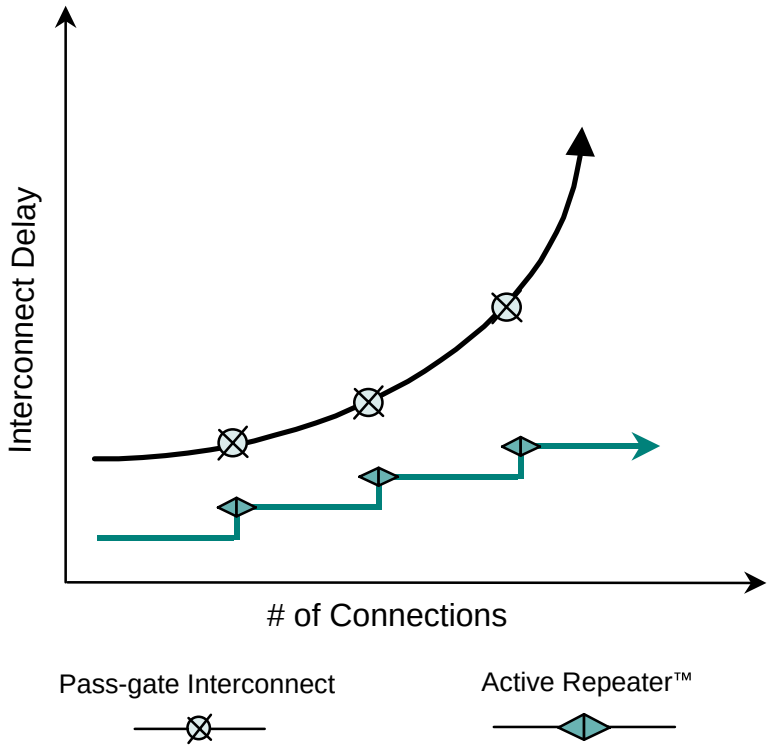


Figure 2: Active Repeater™ vs. Pass Gate Delays

Top-Level Architecture

At the very top level, DynaChip devices look a lot like conventional FPGA devices. As shown in figure 3, input/output blocks surround the edges of the device, an array of logic blocks fill the interior and routing tracks are distributed between the rows and columns of logic blocks.

The difference in DynaChip's architecture lies in the routing resources.

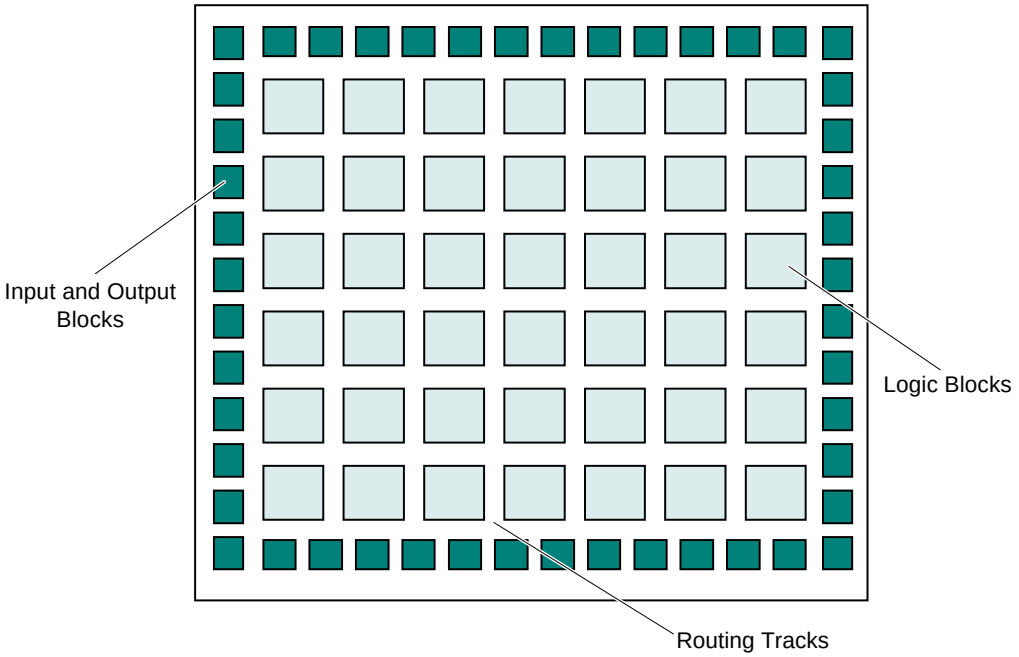


Figure 3: High Level View of Architecture

Routing Architecture

DynaChip's architecture is optimized for Active Repeater technology.

As shown in figure 4, interconnect resources consist of a series of vertical and horizontal wires that make up a routing region. Buffers that drive these wires can be turned on and off to create the required connections. Since every buffer drives a fixed load, it has been carefully optimized to provide maximum performance. The fixed load nature of the interconnect results in completely predictable performance since the delay through the buffer is fixed.

Routing regions are connected with Active Repeaters. After passing through an Active Repeater, signals are available throughout the next routing region.

In the DL6000 family, each routing region is 3 columns wide by 3 rows tall. The location of the Active Repeaters are staggered so that each logic block has its own 3 x 3 region.

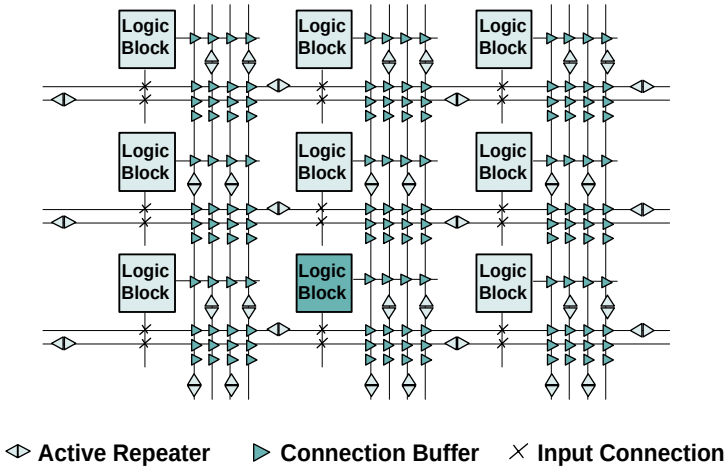


Figure 4: Routing Architecture

This architecture results in completely deterministic performance within a routing region. The logic block delays specified in this datasheet include the delay of the connection buffers and all the routing within a region (refer to table 24 for logic block delays).

As shown in figure 5, this architecture allows a logic block to drive all 9 blocks in the 3 column by 3 row routing region with no additional routing delays. This allows even high fanout nets to have extremely high performance.

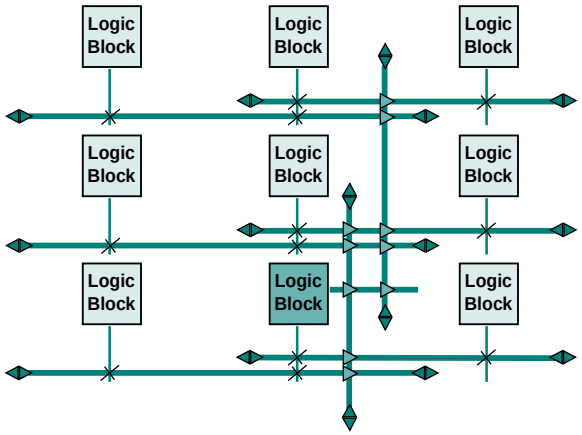


Figure 5: Routing Region With No Interconnect Delay

For signals that drive blocks in the next region, the fixed delay through an Active Repeater is added to the logic block delay. These Active Repeater delays are the only routing delays in the device and their performance is completely specified in this datasheet (refer to table 27 for Active Repeater delays).

As shown in figure 6, a logic block output can drive 33 logic blocks with just 1 Active Repeater delay. This allows structures with up to 660 gates of logic or 1,056 bits of RAM to be implemented with just 800 ps routing delay. With 2 Active Repeater delays, a logic block output can drive 73 logic blocks. This allows up to 1,460 gates of logic or 2,336 bits of RAM with just 1.6 ns routing delay. All routing delays in the device are fixed and are not affected by the fanout on the net.

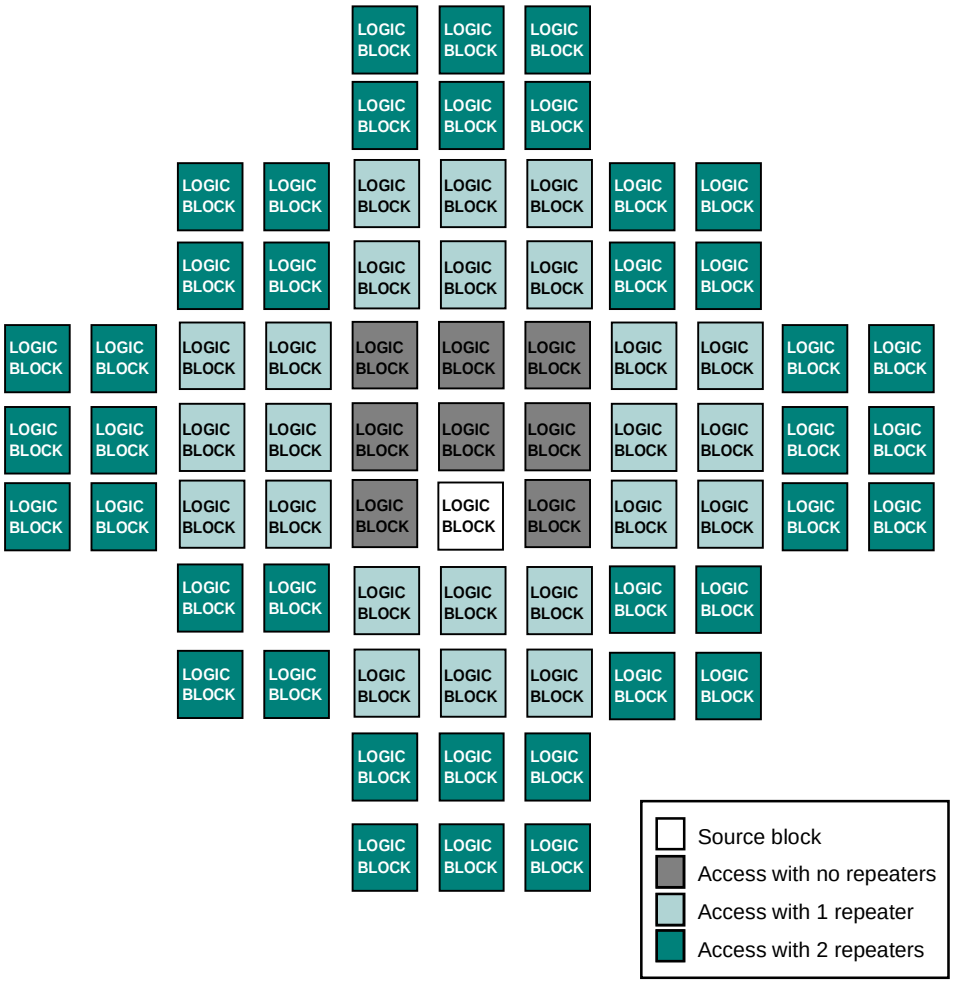


Figure 6: Logic Block Reached With 2 Repeaters

Input/Output Blocks

Every input/output block in the DL6000 can be independently set to TTL and GTL interface levels. The 10 clock inputs can also be set to single-ended or differential LV-PECL levels. When set to differential LV-PECL, the inputs are compatible with LVDS. If any of these 10 inputs are not used for clock signals, they can be used as general purpose inputs.

When set to TTL mode, input/output blocks are 100% compliant with 33Mhz and 66 MHz PCI busses.

Each input/output block can be configured for input, output or bi-directional signals. Each block has 2 flip flops that can be used to register input and output signals. Each flip flop has a clock enable input. Clock signals for flip flops in the input/output blocks are sourced from either of the 2 global clock pins and either of the 2 quadrant clock pins for that region.

Each output has individual slew rate control and 3-state capability. The 3-state enable for each output can be controlled individually.

Each input/output block contains dedicated JTAG Boundary Scan logic compatible with IEEE specifications.

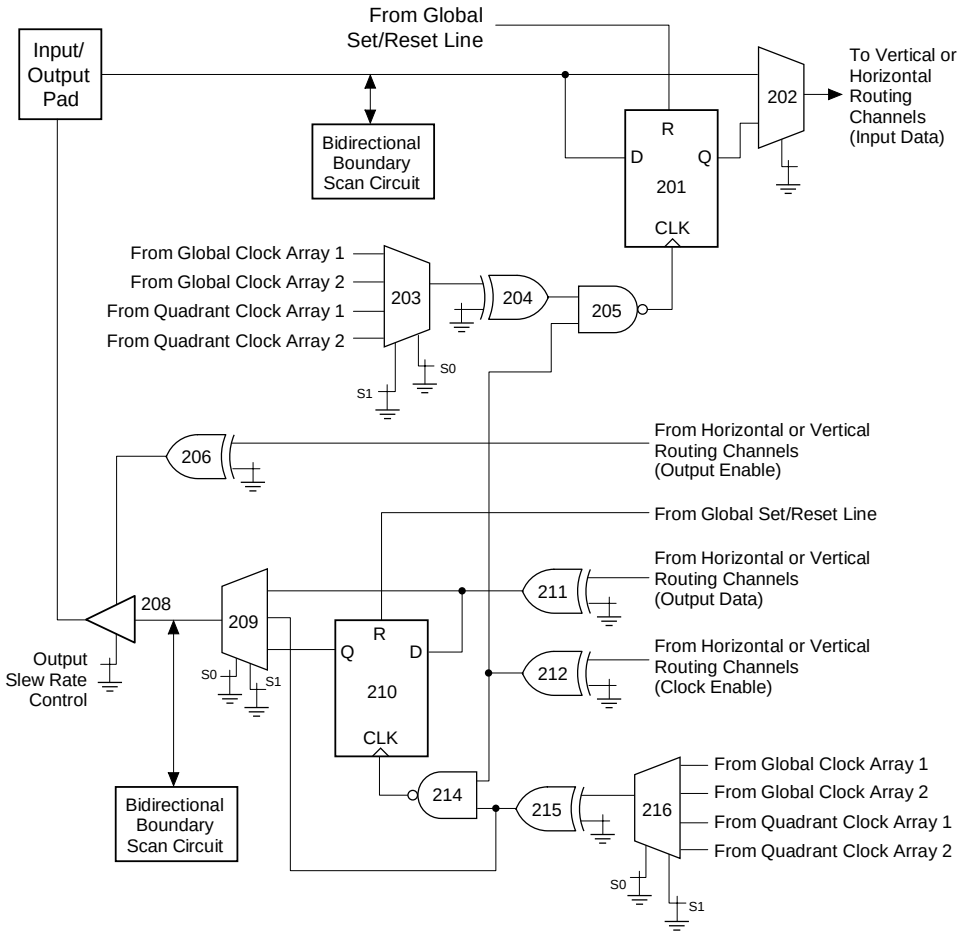


Figure 7: Input/Output Block

LVDS

When set to differential LV-PECL levels, the 10 clock inputs can interface to LVDS levels using a 100 ohm shunt resistor as shown in the following figure. If these inputs are not used for clock signals, they can be used as general purpose inputs.

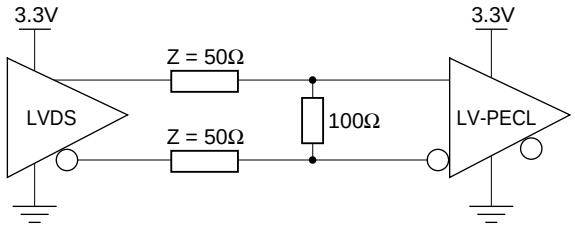


Figure 8: Interfacing LVDS to LV-PECL

Logic Block

The logic block in the DL6000 is extremely flexible and can implement a wide variety of functions. Each block has 18 inputs. One of the inputs is dedicated for clocking and one is for a set or reset signal. The remaining 16 are general purpose inputs to the logic block.

Each logic block contains combinatorial logic, RAM and two flip flops. The combinatorial section contains flexible building blocks optimized for high utilization. Structures like multiplexers, AND/OR gates, comparators and arithmetic functions are automatically mapped to these resources by the DynaChip Development System.

A multiplexer allows the outputs of the combinatorial logic to exit the block directly or to serve as inputs to the two flip flops.

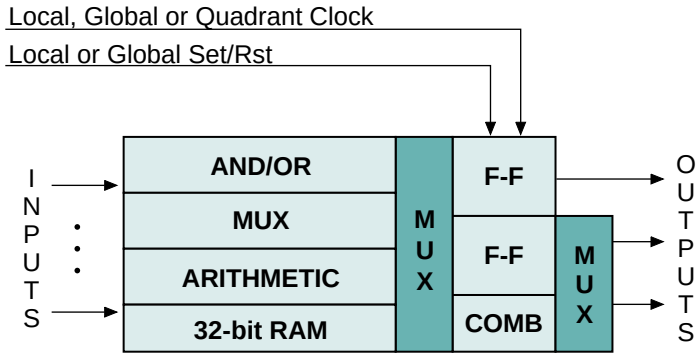


Figure 9: Logic Block

Figure 10 shows a detailed diagram of the logic block in the DL6000.

The logic block contains sections that are optimized for AND/OR logic, multiplexers, arithmetic logic and RAM. All logic block inputs have polarity control allowing signals to be inverted as they enter the block.

Each logic block contains two storage elements that can be configured as D-type or T (toggle) flip flops. The flip flops share a common clock that can be driven by the

device's global or quadrant clocks or by local interconnect. The clock input to each logic block has polarity control allowing the flip flops to be triggered from either clock edge.

The flip flops also share a common set/reset signal that is driven by the device's global set/reset or by local interconnect. Each flip flop can be configured to have either a set or reset capability. The set/reset input to each logic block has polarity control allowing active high or active low operation.

Each logic block has 3 outputs that are driven by the combinatorial logic, RAM or flip flops.

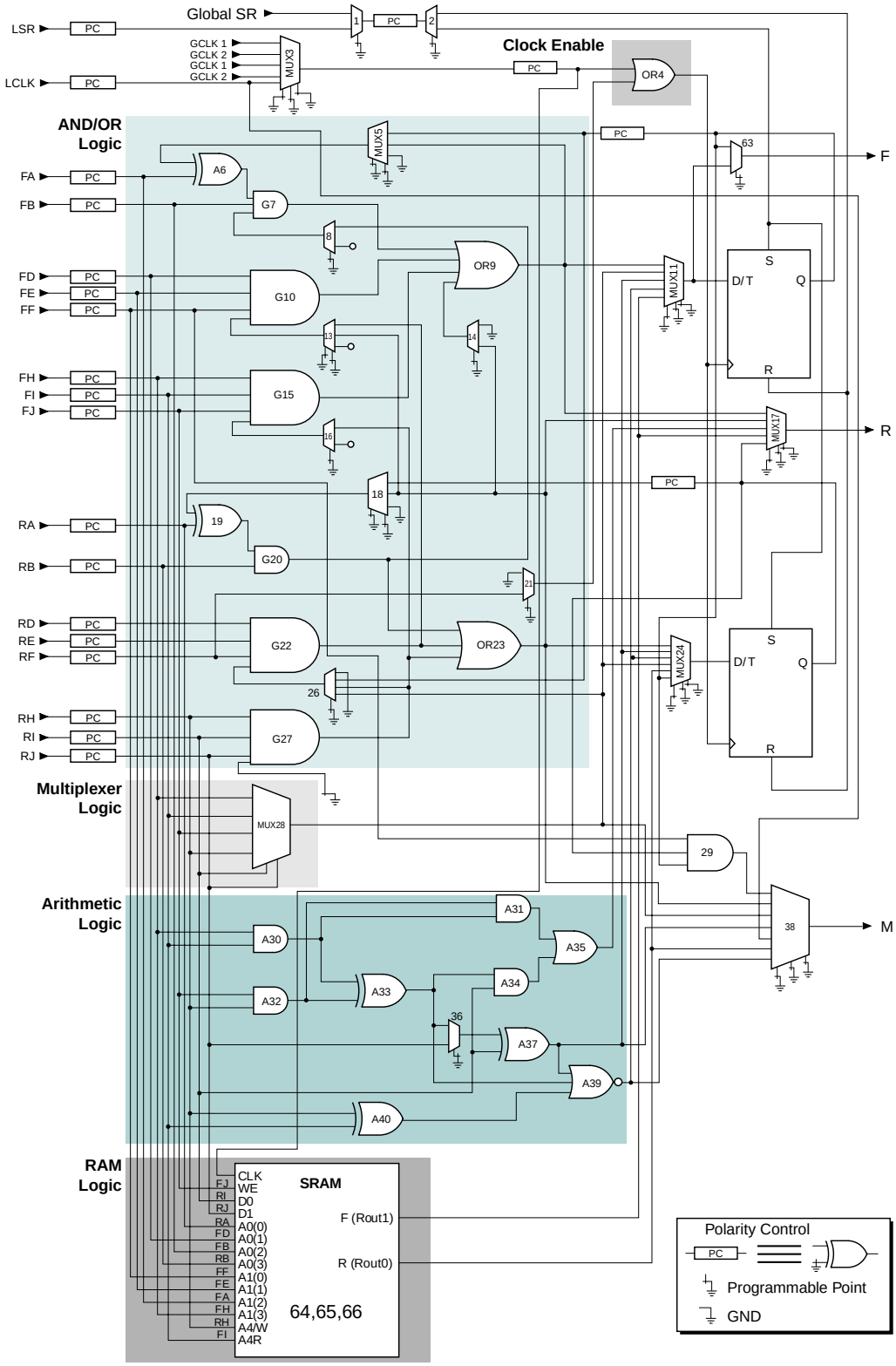


Figure 10: Logic Block Resources

RAM

Each logic block in DL6000 family devices contain a 32-bit fully synchronous configurable RAM. The RAM can be configured as a 32x1 dual port RAM, a 32x1 single port RAM or two 16x1 RAMs with independent data and addresses. The RAM is "self-timed" which makes both read and write operations fully synchronous. The user only needs to be concerned with maintaining setup and hold times for all inputs with respect to the clock. This includes the WE, data and address inputs. There is no need for standard RAM timing parameters such as 'WE pulse width', 'write cycle' or 'read cycle'. From a timing standpoint, the RAM can be treated just like a flip-flop.

The RAM includes a clock generator cell and latches data on its inputs and outputs. Upon receipt of a LOW-to-HIGH transition on the clock input, the clock generator creates a set of internal signals for the RAM. During a write cycle, the clock generator creates a pulse to latch the write enable, data and address inputs. During a read cycle a pulse is generated to latch the addressed data in the output latches. Both read and write operations are completed upon a single low-to-high transition of the clock. This is true for both single and dual port modes. Timing diagrams for the 2 operations are shown in figure 11.

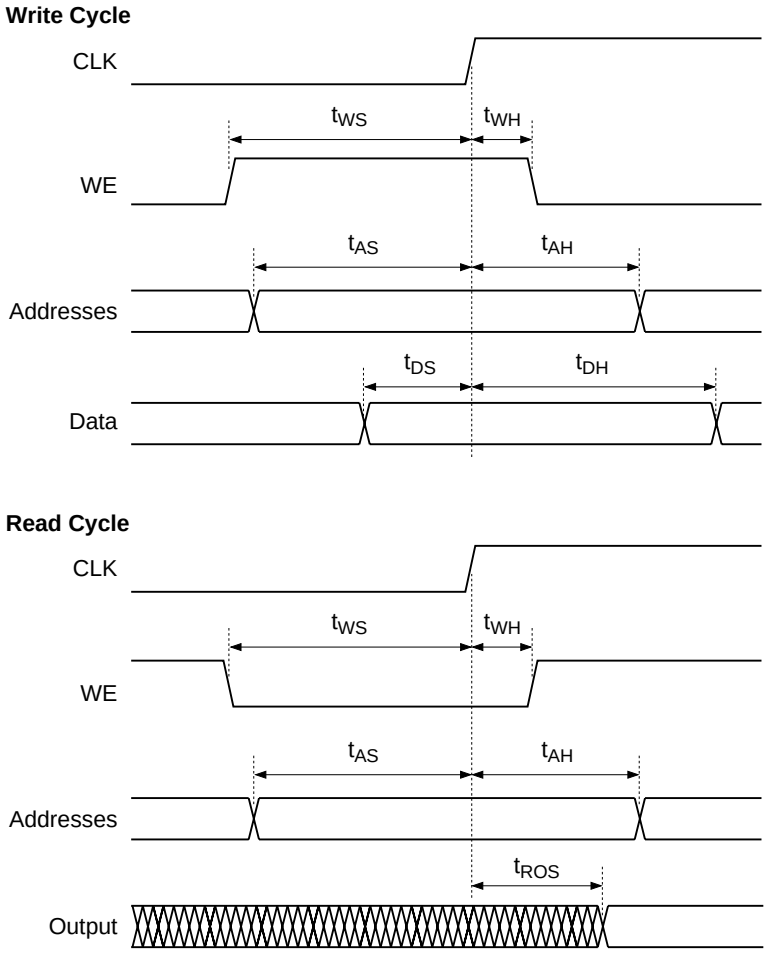


Figure 11: Read/Write Cycle Timing

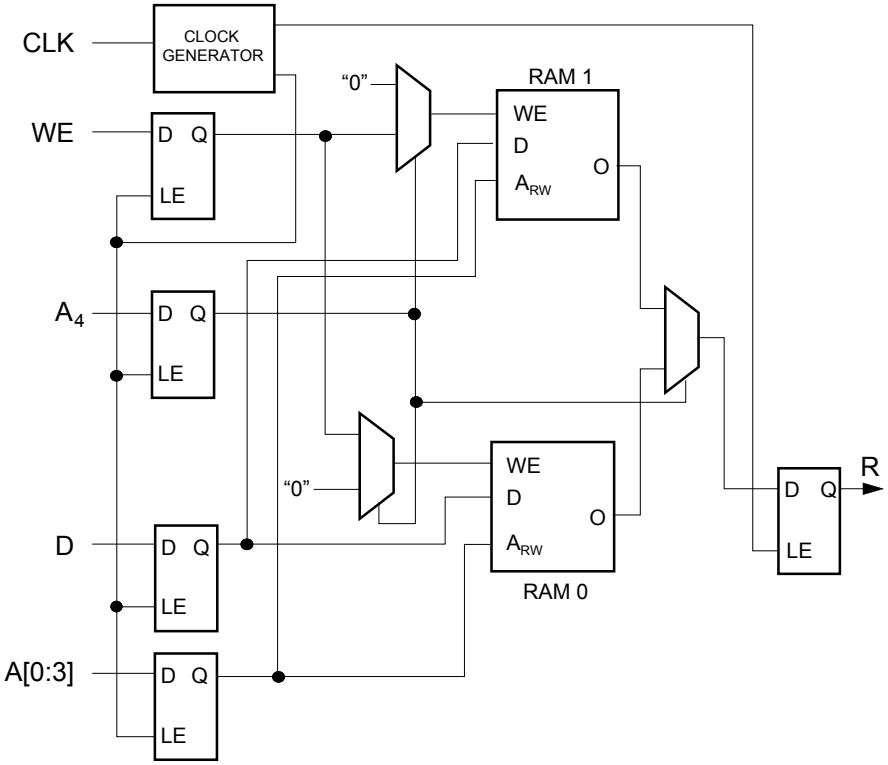


Figure 12: 32x1 Single Port RAM

Figure 12 shows the configuration for the 32x1 Single Port RAM. There are 5 bits for address (A0 - A4), a data input (D), a write enable (WE) and a clock input. All 7 inputs are totally synchronous to the clock. Just like an edge triggered flip flop, the only timing requirement is that all setup and hold times must be obeyed. When WE is HIGH, the RAM is in the write mode. Data presented on the D input will be written to the location specified by addresses A0 - A4. During a write cycle, the output of the RAM is in an unknown state. When WE is LOW, the RAM is in the read mode. The data stored in the location specified by A0 - A4 appears on the output after the rising edge of the clock. This is a single clock operation. The WE and A0 - A4 are setup before the rising edge of the clock and the data stored in the RAM appears after the rising edge of the clock.

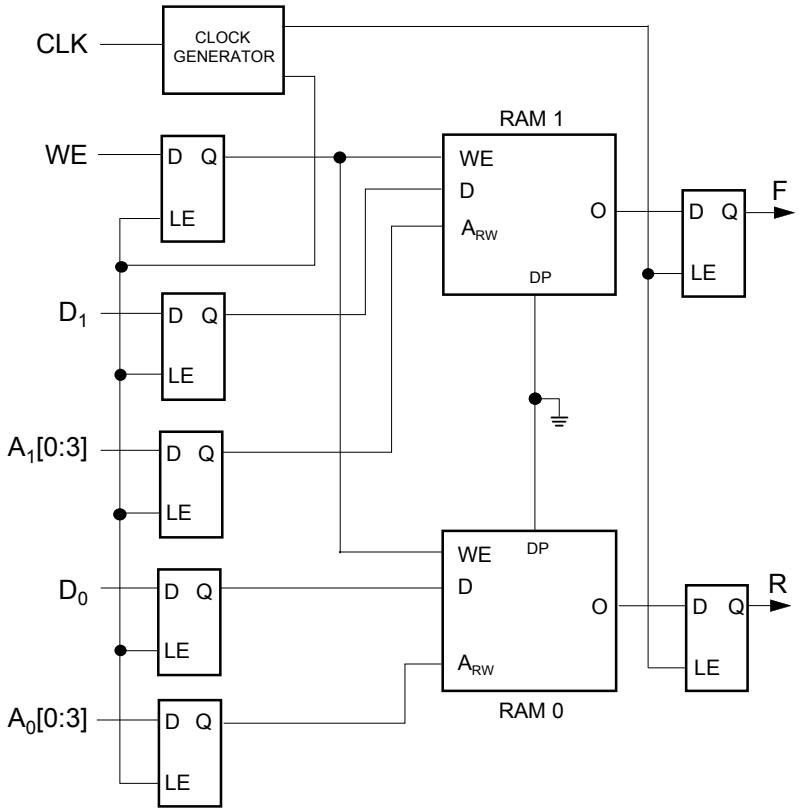


Figure 13: Dual 16X1 Single Port RAM

Figure 13 shows the configuration for the dual 16X1 single port RAM. The cell contains 2 separate 16X1 RAMs where each has their own address and data pins. The dual RAM has 12 inputs. There are 4 bits of address (A00 - A03) and a data input (D0) for RAM 0 and 4 separate bits of address (A10 - A13) and a separate data input (D1) for RAM 1. Both RAMs share the same write enable (WE) and clock input. All 11 inputs are totally synchronous to the clock. Just like an edge triggered flip flop, the only timing requirement is that all setup and hold times are obeyed. Operation of the RAMs is identical to that of the 32X1 single port. When WE is HIGH, the RAMs are in the write mode. Data presented on the D0 input will be written to the location specified by addresses A00 - A03 while data presented on the D1 input will be written to the location specified by addresses A10 - A13. During a write cycle, the outputs of the RAMs are in an unknown state. When WE is LOW, the RAMs are in the read mode. After the rising edge of the clock, the data stored in the location specified by A00 - A03 appears on the output of RAM 0 and the data stored in the location specified by A10 - A13 appears on the output of RAM 1. This is a single clock operation.

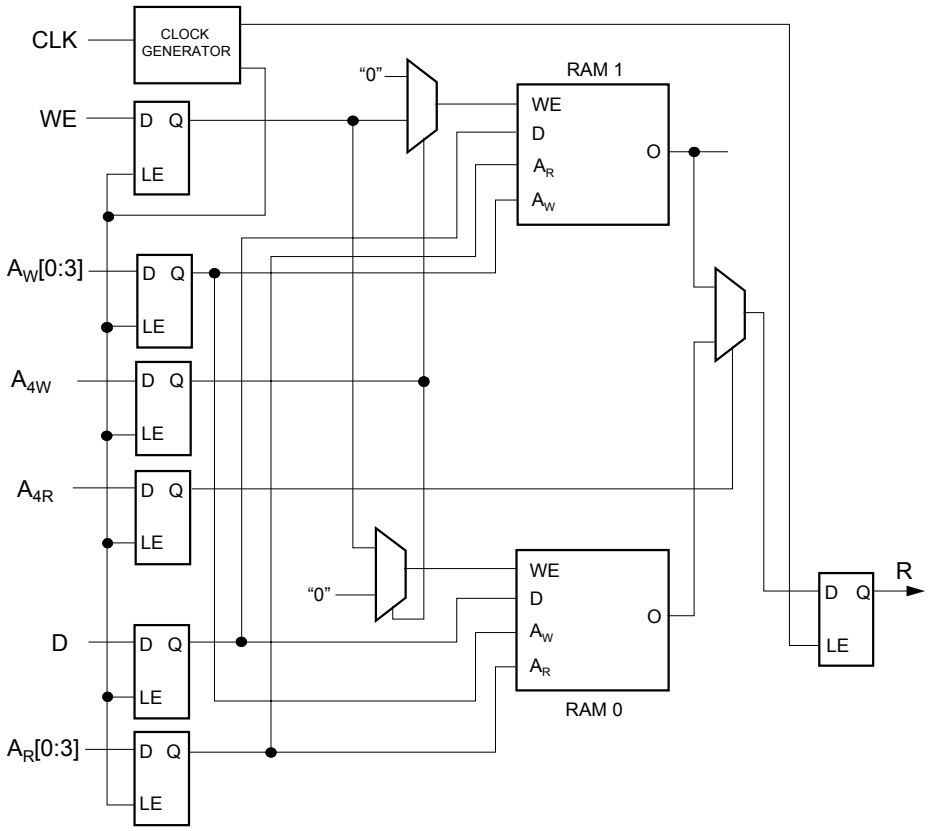


Figure 14: 32x1 Dual Port RAM

Figure 14 shows the configuration for the 32x1 Dual Port RAM. This is a true dual port RAM with separate read and write addresses. The RAM has 5 bits of read address (A0R - A4R), 5 bits of write address (A0W - A4W), a data input (D), a write enable (WE) and a clock input. All 12 inputs are totally synchronous to the clock. Just like an edge triggered flip flop, the only timing requirement is that all setup and hold times are obeyed. The operation of the dual port RAM is slightly different than that of the single port RAMs. When WE is HIGH, the RAM is in the write mode. Data presented on the D input will be written to the location specified by addresses A0W - A4W.

The dual port RAM is always in read mode. The state of WE is unimportant thus WE can either be a "0" or a "1". The data stored in the location specified by A0R - A4R will appear on the output after the rising edge of the clock. This is a single clock operation.

There is one exception to the rule that the RAM is always in read mode. If the read and write addresses are equal and WE is HIGH, the write function takes precedence over the read. As a result, when reading and writing to the same location, only the write function is enabled and the output will be at an unknown state. Note that if WE is LOW, the dual port RAM is in read mode and there will never be a conflict when the read and write addresses are identical.

Clock Distribution

DL6000 family devices have 10 low-skew clock distribution networks. These networks are driven by dedicated pins on the device, internal logic or by the internal PLLs.

Two of the clock networks are global clocks that can drive every flip flop in the device. Eight of the networks are quadrant clocks. The quadrant clocks can drive all the logic block flip flops in one quarter of the device and the I/O flip flops adjacent to these logic blocks.

When driven by input pins, each of the 10 clocks are programmable to LV-TTL, GTL or LV-PECL interface levels. When set to LV-PECL, clock inputs can be single-ended or differential.

Any I/O pin can be used to drive a clock signal out of the device for use elsewhere in the system.

Phase Lock Loops

Devices in the DL6000 family contain 2 analog phase lock loop (PLL) circuits that are used for clock multiplication, division and phase locking.

The output clock from the PLL has a duty cycle of 50% +/- 5% and a lock time of 1 ms.

As shown in figure 15, the output of each PLL can drive 1 global clock and 4 quadrant clock trees. The multipliers and dividers for each quadrant can be set independently. This allows each PLL to generate up to 5 derivative frequencies from the incoming clock.

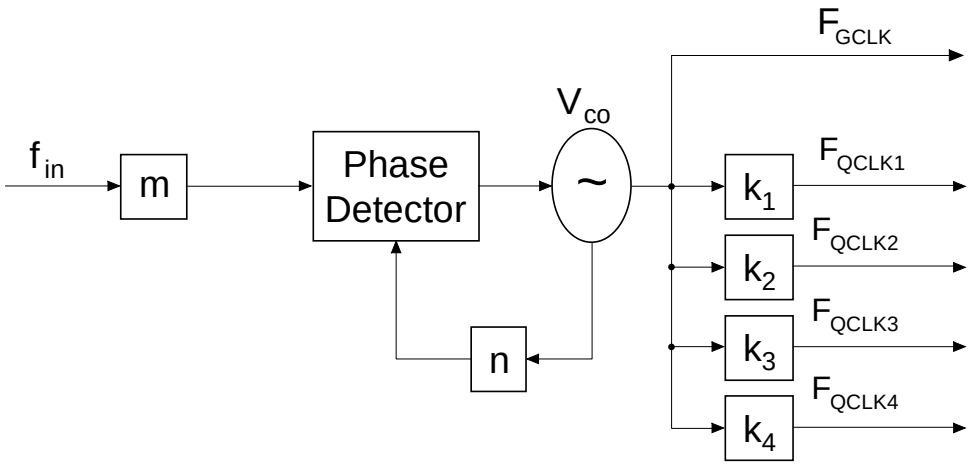


Figure 15: PLL

Frequencies for quadrant clock outputs can be divided or multiplied according to the following formula.

$$f_{QCLKx} = fin*n / k_x*m$$

Frequencies for global clock outputs can be multiplied according to the following formula.

$$f_{GCLK} = fin*n / m$$

Values for k, m, and n can be programmed as shown in table 3.

Variable	Allowable Values
k	2,3,4,6 or 8
m	1 or 2
n	2,3,4,6 or 8

Table 3: PLL Variables

The following tables show the available multipliers and dividers for different frequencies.

Fin Min	Fin Max	GCLK Multiplier	QCLK Multiplier	QCLK Dividers
14.4	20.6	8	4 2 2/3 2 1 1/3 1 (Lock)	
19.2	27.5	6 1 (Lock)	3 2 1 1/2 1 (Lock)	3/4
28.8	41.3	4 1 (Lock)	2 1 1/3 1 (Lock)	2/3 1/2
38.3	55.0	3 1 (Lock)	1 1/2 1 (Lock)	3/4 1/2 3/8
57.5	82.5	2 1 (Lock)	1 (Lock)	2/3 1/2 1/3 1/4
76.7	110.0	1 1/2 1 (Lock)		1/2 3/4 3/8 1/4 3/16
115.0	200.0	1 (Lock)		1/2 1/3 1/4 1/6 1/8

Table 4: Multipliers and Dividers for PLL1

Notes:
(1) PLL1 is located in the top left corner and drives GCLK1, QCLK1TL, QCLK1TR, QCLK1BL, and QCLK1BR.
(3) Some frequencies require an external resistor connected to the PLL1REST pin.

Fin Min	Fin Max	GCLK Multiplier	QCLK Multiplier	QCLK Dividers
10.3	14.4	8	4 2 2/3 2 1 1/3 1 (Lock)	
13.8	19.2	6	3 2 1 1/2 1 (Lock)	3/4
20.6	28.8	4 1 (Lock)	2 1 1/3 1 (Lock)	2/3 1/2
27.5	38.3	3 1 (Lock)	1 1/2 1 (Lock)	3/4 1/2 3/8
41.3	57.5	2 1 (Lock)	1 (Lock)	2/3 1/2 1/3 1/4
55.0	76.7	1.5 1 (Lock)		3/4 1/2 3/8 1/4 3/16
82.5	115.0	1 (Lock)		1/2 1/3 1/4 1/6 1/8

Table 5: Multipliers and Dividers for PLL2

Notes:
(1) PLL2 is located in the top right corner and drives GCLK2, QCLK2TL, QCLK2TR, QCLK2BL, and QCLK2BR.
(3) Some frequencies require an external resistor connected to the PLL2REST pin.

GCLK Frequency	Jitter
14 to 80 MHz	3% of clock period
81 to 165 MHz	350 ps (1)

Table 6: PLL Jitter

Note:
(1) Requires input clock jitter ≤ 100 ps.

Power Consumption

Power consumption for a specific design implemented in a DL6000 family device depends on the following factors.

- Number of logic blocks used
- Operating frequency
- Number of outputs used
- I/O interface level setting (TTL or GTL)
- Output slew rate selection
- Number of global and quadrant clocks used
- Operating supply voltage

The following table shows typical power consumption for various components of a DL6035 operating at 100 MHz.

DL6035 Component	Typical Power Consumption at 100 MHz
Logic Block (including interconnect)	4.6 mW
I/O Block set to TTL mode (excluding off-chip current)	910 µW
I/O Block set to GTL mode (excluding off-chip current)	7.5 mW
Each Global Clock	600 mW
Each Quadrant Clock	150 mW

Table 7: Typical Power Consumption

Configuration

Memory cells in DynaChip FPGAs store configuration bits that control all the programmable elements in the device. These configuration bits are called a bitstream and they are loaded automatically from a PROM at power-up or under user control through a microprocessor.

Systems that contain more than one DynaChip device can be set up in a programming chain to simplify connections.

Configuration Modes

The DL6000 supports 6 configuration modes. Five are for loading a bitstream into the device and one is for reading a bitstream out of a programmed device. The state of three special pins called mode pins sets the configuration mode of the DL6000 device.

Serial Configuration Modes

There are 3 serial configuration modes as described in table 8.

Serial Configuration Mode	Description
Serial Internal Last	This mode is used in 2 situations. 1) To program a single device from a serial PROM. In this mode, the DL6000 generates a clock signal to drive the serial PROM. 2) For the last device in a programming chain that uses a serial PROM. In this mode, the DL6000 generates a clock signal to drive the serial PROM and the other DynaChip devices in the chain.
Serial External Not Last	This mode is used for each device except the last device in a programming chain that uses a serial PROM.
Serial External Last	This mode is used to program a single device using a serial bitstream and a user supplied clock. It is also used for the last device in a programming chain that is programmed using a serial bitstream and a user supplied clock.

Table 8: Serial Configuration Modes

Microprocessor Configuration Modes

There are 2 microprocessor configuration modes as described in table 9.

Microprocessor Configuration Mode	Description
Microprocessor Last	This mode is used in 2 situations. 1) To program a single device from a microprocessor. 2) For the last device in a programming chain that uses a microprocessor.
Microprocessor Not Last	This mode is used for each device except the last device in a programming chain that uses a microprocessor.

Table 9: Microprocessor Configuration Modes

Dynamic Reconfiguration Using Full Chip Reset

Full Chip Reset enables the user to completely reset the device without turning off the power. It is typically used to prepare a device for a complete reconfiguration after initial configuration. When full chip reset is asserted, all the configuration bits and flip flops in the device are reset. This is similar to the internal reset that occurs when the device is first powered-up.

Full chip reset is activated by setting the mode pins to '111' and then asserting the RESET pin (active low) for a minimum of 10 ms. The mode pins must be set before the reset is asserted.

To reprogram the device after a full chip reset, set the mode pins to their appropriate values (refer to table 10, page 22) and apply another RESET pulse of at least 10 ms.

As an alternative to using full chip reset, the device can be reprogrammed using a complete bitstream that programs every element. Contact the factory for availability of a complete bitstream.

Partial Reprogramming

After the device has been powered-up and programmed, the user can reprogram a portion of the device on the fly without affecting the existing application.

To dynamically reprogram a portion of the device, set the mode pins to their appropriate value (refer to table10, page20), and then assert RESET (active low). The mode pins must be set before the RESET is asserted.

The portion of the device that is not affected by the partial reprogramming operates normally during reconfiguration.

Special bitstreams must be used for partial reconfiguration to insure that unused logic and interconnect from the previous function are deleted. Contact the factory for more information on availability of these special bitstreams.

Some of the non-dedicated configuration I/O do not function as user I/O during dynamic reprogramming as indicated below:

In Serial Mode:

- Pins M0, M1, M2 and D0, become dedicated for programming.
- The DONE pin becomes dedicated for programming when the device is used in a programming chain.
- The DOUT pin becomes dedicated for programming if readback is required.
- The rest of the I/O's remain operational.

In Processor Mode:

- Pins M0, M1, M2, D0, D1-D7, WE and RDY become dedicated for programming.
- The DONE pin becomes dedicated for programming when the device is used in a programming chain.
- The DOUT pin becomes dedicated for programming if readback is required.
- The rest of the I/O's remain operational.

Readback

Once the device has been programmed, a configuration mode called readback can be used to read the program bitstream out of the device to determine if it was loaded properly.

Configuration Clock Frequencies

In Serial Internal Last mode, the DL6000 generates a 2.5 MHz clock that is used to drive the serial PROM.

In Serial External Last mode, an external clock up to 25 MHz can be supplied to the DL6000.

Mode Pin Settings

The state of three pins on the DL6000 device named M0, M1 and M2 determine the loading mode. The settings for each mode are shown in table 10.

Configuration Mode	M2	M1	M0
Serial Internal Last	0	0	0
Serial External Not Last	1	0	0
Serial External Last	0	0	1
Microprocessor Last	1	0	1
Microprocessor Not Last	1	1	0
Readback	0	1	1
Full Chip Reset	1	1	1

Table 10: Mode Pin Settings

Note:
If the mode pins are not connected, they are pulled down to a logic '0'.

Flip Flop Initialization

After configuration, flip flops are in an unknown state. All flip flops can be initialized by applying a global reset signal to the device.

Upon assertion of the global reset, I/O and logic block flip flops are either set or reset depending on their definition in the design.

Configuration Schematics

The following schematics show typical connections to the DL6000 for each loading mode.

Serial PROM Configuration Mode

In the serial PROM configuration mode, the device automatically loads itself from a serial PROM when the system is powered up. The PROM provides serial data and responds to a clock signal generated by the DL6000 device.

Systems using this loading mode should be connected as shown in figure 16.

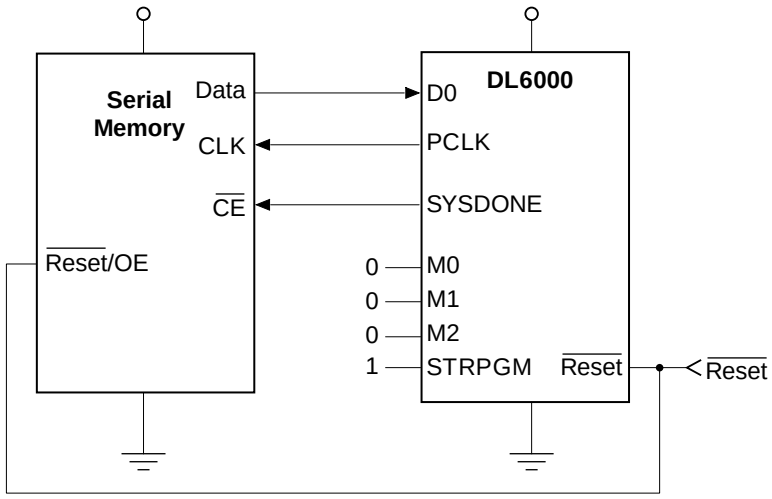


Figure 16: Serial PROM Configuration Schematic

Microprocessor Configuration Mode

In the microprocessor configuration mode, the device is loaded under user control from a microprocessor interface. Data is loaded into the DL6000 device byte-wide in response to the rising edge of a write enable signal. The DL6000 device generates a ready signal that indicates it is ready for the next byte of data.

Systems using the microprocessor configuration mode should be connected as shown in figure 17.

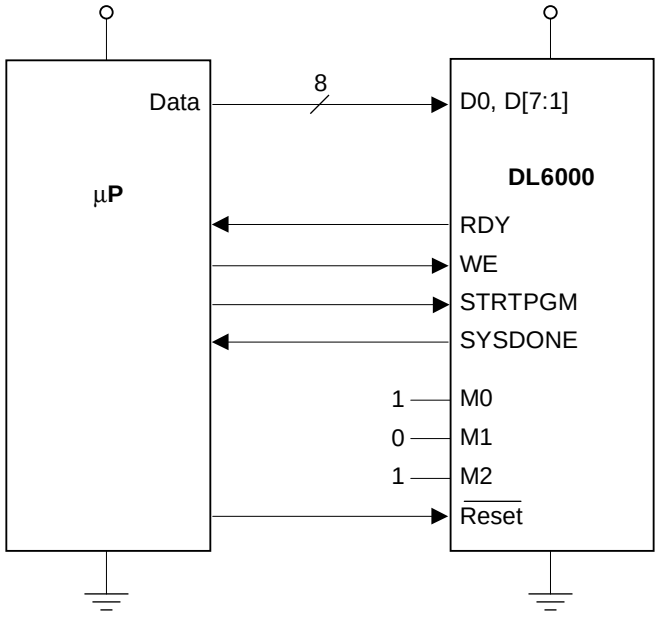


Figure 17: Microprocessor Configuration

A microprocessor can also be used to load the DL6000 family device in serial external mode. In this configuration, the microprocessor supplies a clock and serial data to the DL6000 family device.

Programming Chains

Programming chains simplify connections for systems that use more than one DL6000 family device. Using programming chains, one DL6000, called the last device, connects to the source of the configuration data. The remaining DL6000 devices connect in a chain using their serial configuration pins.

Systems using programming chains with a serial PROM should be connected as shown in figure 18. Systems using programming chains with a microprocessor should be connected as shown in figure 19.

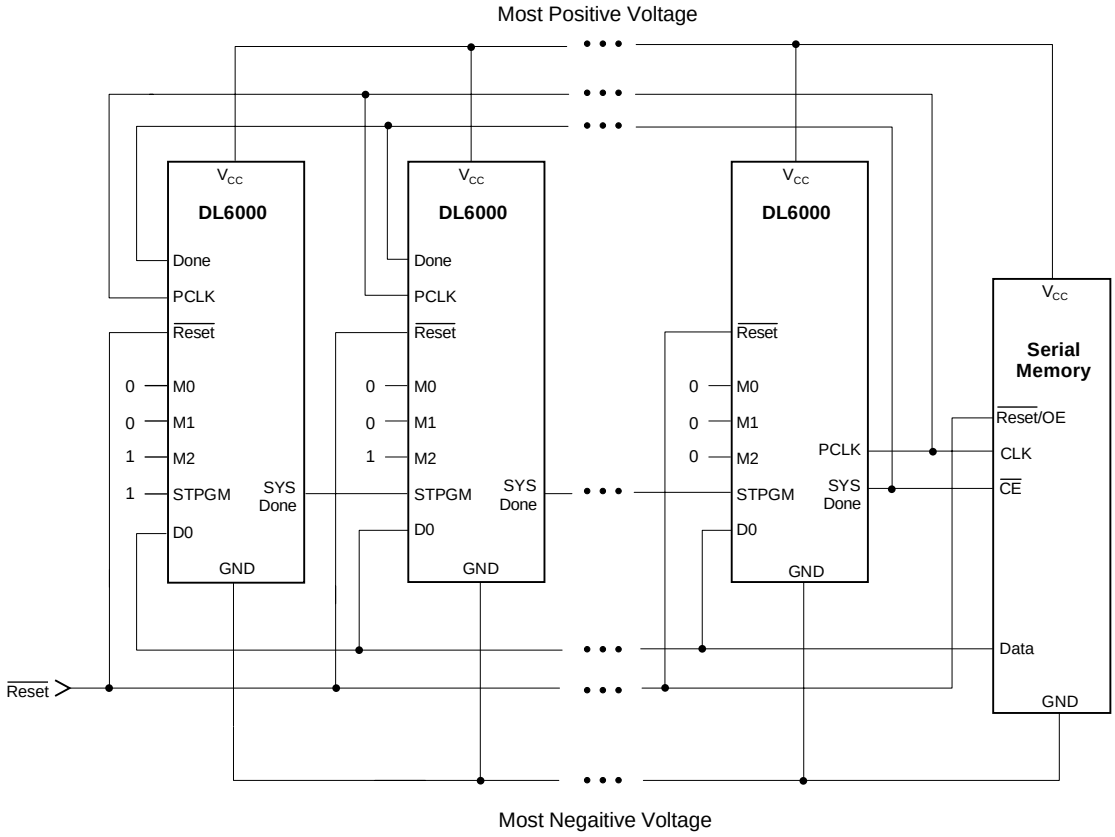


Figure 18: Programming Chain Using Serial Memory

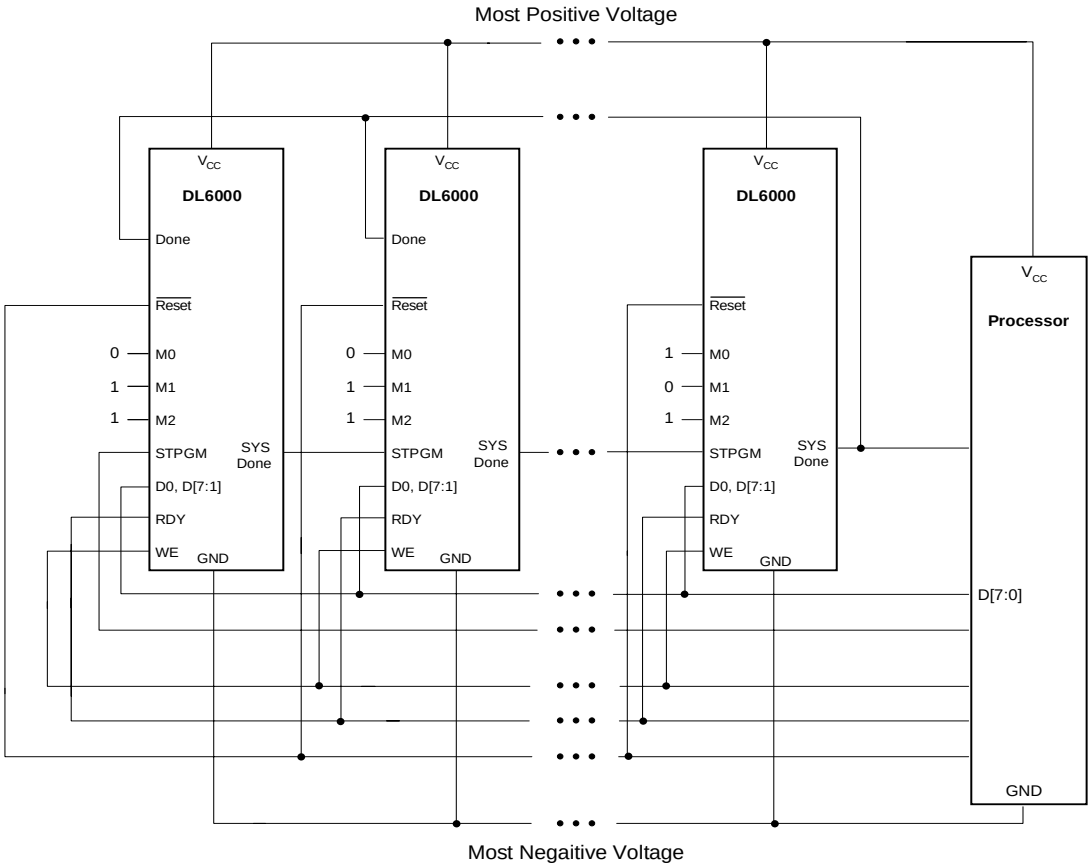


Figure 19: Programming Chain Using Microprocessor

Bitstream Size

The size of the programming bitstream for a DL6000 family device depends on the number of logic blocks that are used in the design. The following table shows the maximum number of programming bits for each device in the DL6000 family.

Device	Maximum Number of Programming Bits
DL6009	140,000
DL6020	270,000
DL6035	450,000
DL6055	670,000
DL6080	940,000
DL6105	1,300,000

Table 11: Maximum Number of Programming Bits

Configuration Pins

Two types of pins are used in the configuration process. Permanently dedicated pins are always dedicated to configuration functions. User pins that can have special functions become user I/O pins after device configuration

Pin	Dedicated	Function
PCKI/ PCKO	Yes	This pin has 3 different functions depending on the programming mode. 1) If the device is the only device to be programmed or is last in a programming chain and an external clock is not being used, this pin is an output that sends the master clock to all other devices and the serial PROM. 2) If the device is in a programming chain and is not the last device, this is an input pin that receives the master clock from the last device. 3) If an external, user supplied clock controls the configuration process, this pin is the input for that clock. When not in programming, this pin defaults to an input.
STRPGM	Yes	This pin should be connected as shown in the configuration schematics.
$\overline{\text{RESET}}$	Yes	This reset is used for dynamic reprogramming. It is asserted by setting the mode pins to any value except '111' and asserting the RESET pin (active low) for a minimum of 10 ms. Note that the mode pins must be set before the RESET is asserted. All non-dedicated configuration I/O's assume states based on the function defined by the programming mode. If dynamic reprogramming is not required, the RESET pin should be connected as shown in the configuration schematics.
SYS DONE	Yes	This output pin is dedicated for programming. Once configuration has been completed, this pin goes from low to high and stays high until either the power is turned off or a reset signal is applied. If the device is the last or only device to be programmed, this pin signals the device that configuration has been completed and to start normal operation. Also, if the device is the last in a programming chain, this pin signals all other devices that programming has been completed and to return to normal operation. This signal also controls the enabling and disabling of a serial PROM(s).
M0 - M2	No	These pins are inputs during programming. They are used to tell the device(s) which mode will be used for configuration. The list of settings for each configuration mode is shown in table 10. These pins become I/O's during normal operation. If the mode pins are not connected, they are pulled down to a logic '0'.

Pin	Dedicated	Function
DONE	No	This is an input pin during programming that is only used in a multiple device configuration mode. If the device is not last, the DONE pin is tied to the SYSDONE pin of the last device. A low to high on this pin signals that programming has been completed and the device begins normal operation. This pin can be used as an I/O during normal operation.
D0	No	This is an input pin during programming. It accepts serial data from a memory source or another device. It can also accept the LSB from a byte wide memory source for microprocessor configuration mode. This pin can be used as an I/O during normal operation.
D1 - D7	No	These are data input pins for the microprocessor configuration mode. They are only activated after the reset signal has been applied. They accepts bits 1 - 7 of data loaded from a parallel source. Can be used as I/Os during normal operation.
WE	No	This is a input pin during microprocessor configuration mode. It is only activated after the reset signal has been applied. This pin is used by the processor to signal the DL6000 that 8-bits have been placed on the D[7:0] pins for loading. This pin becomes an I/O during normal operation.
RDY	No	This is an output pin for microprocessor configuration mode. It signals an external processor that 8 bits have been loaded and the device is ready to receive the next 8 bits. This pin can be used as an I/O during normal operation.
DOUT	No	This outputs pin supplies the bitstream during readback mode. This pin can be used as an I/O during normal operation.

JTAG

All devices in the DL60000 family provide JTAG Boundary Scan. Completely compatible with IEEE specifications, this feature simplifies testing of boards with surface mount packages or closely spaced pins.

Four JTAG instructions are supported as shown in table 12.

JTAG Instructions	Register	Opcode
SAMPL/PRE	BSC	1000
EXTEST	BSC	0000
BYPASS	BYPASS	1111
IDCODE	ID	1101

Table 12: JTAG Instructions

The JTAG ID register is read when the DL6000 is reset and when Opcode 1101 is loaded. On power-up, the opcode defaults to 1101. Internal pull-up resistors are provided on the TDI and TMS pins.

The DL6000 JEDEC ID number is 331-300-6100-0.

Product Specifications

Maximum Ratings

Symbol	Description	Value	Unit
V_{CC}	V_{CC} Pin Potential to GND Pin	-0.5 to +5.0	V
V_{IN}	Input Voltage	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} + 0.5	V
T_{STORE}	Storage temperature	-65 to +150	C
T_J	Junction Temperature	+150	C

Table 13: Absolute Maximum Rating

Note:

Permanent damage to the device may occur if the Absolute Maximum ratings are exceeded. This is a stress rating only. Functional operation of the device at these or any other conditions other than those listed under the Recommended Operating Conditions is not implied.

Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Unit
V_{CC}(1)	Supply voltage relative to GND			
	Commercial 0 C to 85 C junction	3.14	3.47	V
	Industrial –40 C to 100 C junction	3.0	3.6	V
V_{TT}	GTL terminating voltage relative to GND			
	Commercial 0 C to 85 C junction	1.14	1.26	V
	Industrial –40 C to 100 C junction	1.08	1.32	V

Table 14: Recommended Operating Conditions

Notes:

(1) 0.25µ devices require a core supply voltage of 2.5V +/- 5% and an I/O supply voltage of 3.3V +/- 5%.

(2) All junction temperatures above those listed as Operating conditions are illegal.

DC Characteristics Over Operating Conditions

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IMAX} (5)	Max. voltage applied to input	-	5.5	V	
V_{CMAX} (6)	Max. voltage applied to clock inputs	-	3.63	V	
$V_{IH(TTL)}$	High-level Input Voltage	2.0	V_{CC} + 0.3	V	
$V_{IL(TTL)}$	Low-level input voltage	0.0	0.8	V	
$V_{IH(CMOS)}$	High-level Input Voltage	$0.7V_{CC}$	V_{CC}	V	
$V_{IL(CMOS)}$	Low-level input voltage	0.0	$0.3V_{CC}$	V	
$V_{IH(GTL)}$	High-level Input Voltage	V_{REF} + 0.2	V_{TT}	V	
$V_{IL(GTL)}$	Low-level input voltage	0.0	V_{REF} - 0.2	V	
$V_{IH(LVPECL)}$	High-level input voltage	2.135	2.420	V	When V_{CC} = 3.3V
$V_{IL(LVPECL)}$	Low-level input voltage	1.490	1.825	V	When V_{CC} = 3.3V
$V_{OH\ (TTL)}$	High level output voltage	2.4		V	V_{CC} min, See note 2 for I_{OH}
$V_{OL(TTL)}$	Low level output voltage (1,2)	-	0.4	V	V_{CC} min, See note 2 for I_{OL}
$V_{OH(GTL)}$	High level output voltage (3,4)	-	V_{TT}	V	
$V_{OL(GTL)}$	Low level output voltage (3)	-	0.4	V	I_{OL} = 20 mA, V_{TT} max
I_{CC}	Quiescent current	-	10	mA	V_{CC} = MAX; All I/O's open
I_{IL}	Leakage Current	-10	+10	µA	
C_{IN}	Input capacitance	-	8.5	pF	

Table 15: DC Electrical Characteristics

Notes:
(1) With 50% of the outputs simultaneously sinking 16 mA each.
(2) Sink/Source current in TTL mode varies with slew rate setting:
Fast slew rate: sink/source current = 16 mA (at V_{CC} min)
Medium slew rate: sink/source current = 11 mA (at V_{CC} min)
Slow slew rate: sink/source current = 5 mA (at V_{CC} min)
(3) Sink current in GTL mode = 24 mA. Source current is provided by external pull-up resistor.
(4) $V_{REF} = 2/3\ V_{TT}$
(5) All I/O pins except clock inputs are 5 volt tolerant.
(6) The maximum voltage applied to the following clock input pins should not exceed this value, even if they are used as non-clock I/O.
QCLK1TL, QCLK1TLN, QCLK2TL, QCKL2TLN, QCLK1BL, QCKL1BLN, QCLK2BL, QCKL2BLN, QCLK1BR, QCLK1BRN, QCLK2BR, QCKL2BRN, QCLK1TR, QCKL1TRN, QCLK2TR, QCKL2TRN, GCLK1, GCLK1N, GCLK2, GCLK2N, PLLIREST, PLL2REST

Clock and Set/Reset Buffer Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Clock buffer delay with PLL	T_{CPLL}	1.1	1.0	0.9	ns
Global clock delay without PLL (1)	T_{GCKD}	6.7	5.6	5.0	ns
Global clock skew	T_{GCKS}	.15	.15	.15	ns
Quadrant clock delay without PLL(1)	T_{QCKD}	5.5	5.0	4.5	ns
Quadrant clock skew	T_{QCKS}	.15	.15	.15	ns
Clock min pulse width high	T_{MPH}	2.4	2.2	2.0	ns
Clock min pulse width low	T_{MPL}	2.4	2.2	2.0	ns
Global Set/Reset delay	T_{GSR}	33	30	27	ns

Table 16: Clock Buffer AC Characteristics (Input Set to TTL)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip flop clock input.
(2) All delays are specified over commercial voltage and temperature range.
(3) Clock delays are also referred to as latency.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Clock buffer delay with PLL	T_{CPLL}	1.9	1.7	1.6	ns
Global clock delay without PLL (1)	T_{GCKD}	7.6	6.1	5.5	ns
Global clock skew	T_{GCKS}	.15	.15	.15	ns
Quadrant clock delay without PLL(1)	T_{QCKD}	6.4	5.9	5.4	ns
Quadrant clock skew	T_{QCKS}	.15	.15	.15	ns
Clock min pulse width high	T_{MPH}	2.4	2.2	2.0	ns
Clock min pulse width low	T_{MPL}	2.4	2.2	2.0	ns
Global Set/Reset delay	T_{GSR}	34	31	28	ns

Table 17: Clock Buffer AC Characteristics (Input Set to GTL)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip flop clock input.
(2) All delays are specified over commercial voltage and temperature range.
(3) Clock delays are also referred to as latency.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Clock buffer delay with PLL	T_{CPLL}	1.9	1.7	1.6	ns
Global clock delay without PLL (1)	T_{GCKD}	7.6	6.1	5.5	ns
Global clock skew	T_{GCKS}	.15	.15	.15	ns
Quadrant clock delay without PLL(1)	T_{QCKD}	6.4	5.9	5.4	ns
Quadrant clock skew	T_{QCKS}	.15	.15	.15	ns
Clock min pulse width high	T_{MPH}	2.4	2.2	2.0	ns
Clock min pulse width low	T_{MPL}	2.4	2.2	2.0	ns
Global Set/Reset delay	T_{GSR}	34	31	28	ns

Table 18: Clock Buffer AC Characteristics (Input Set to LV-PECL)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip flop clock input.
(2) All delays are specified over commercial voltage and temperature range.
(3) Clock delays are also referred to as latency.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Clock buffer delay with PLL	T_{CPLL}	1.9	1.7	1.6	ns
Global clock delay without PLL (1)	T_{GCKD}	7.6	6.1	5.5	ns
Global clock skew	T_{GCKS}	.15	.15	.15	ns
Quadrant clock delay without PLL(1)	T_{QCKD}	6.4	5.9	5.4	ns
Quadrant clock skew	T_{QCKS}	.15	.15	.15	ns
Clock min pulse width high (4)	T_{MPH}	2.4	2.2	2.0	ns
Clock min pulse width low	T_{MPL}	2.4	2.2	2.0	ns
Global Set/Reset delay	T_{GSR}	34	31	28	ns

Table 19: Clock Buffer AC Characteristics (Input Set to Differential LV-PECL)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip flop clock input.
(2) All delays are specified over commercial voltage and temperature range.
(3) Clock delays are also referred to as latency.
(4) For RAM operation, see clock min pulse width high in table 25.

Input and Output Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input buffer combinatorial delay	T_{INPD}	4.3	3.2	2.6	ns
Input Register Set-up Time (global clock)	T_{INIS1}	2.1	1.6	1.3	ns
Input Register Hold Time (global clock)	T_{INIH1}	0	0	0	ns
Input Register Clock to Output (global clock)	T_{INCO1}	3.5	2.6	2.1	ns
Output buffer combinatorial delay (no load)(2,3)	T_{OUTIS1}	6.0	4.6	3.5	ns
Output Register Set-up Time (global clock)	T_{OUTIS2}	3.5	2.6	1.9	ns
Output Register Hold Time (global clock)	T_{OUTIH1}	0	0	0	ns
Output Register Clock to Output (global clock, no load) (2,3)	T_{OUTCO1}	3.6	2.9	2.3	ns
I/O Register Clock Enable Setup Time	T_{CES1}	2.7	2.0	1.4	ns
I/O Register Clock Enable Hold Time	T_{CEH1}	0	0	0	ns
Input Register GSR set/reset delays	T_{GSRI}	3.4	2.6	2.1	ns
Output Register GSR set/reset delays	T_{GSRO}	3.7	3.0	2.4	ns
Input Register GSR set/reset setup time	T_{GSRIS1}	0.5	0.4	0.3	ns
Output Register GSR set/reset setup time	T_{GSROS1}	0.5	0.4	0.3	ns

Table 20: Input and Output Buffer Parameters (I/O Set to TTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Output delays are specified with no load. Add the following delays to adjust for loading.
Fast Slew Rate: 40 ps/pf
Medium Slew Rate: 60 ps/pf
Slow Slew Rate: 95 ps/pf
(3) The maximum loading for outputs switching at the same time in the same direction is shown below. Significant ground bounce may occur if these guidelines are violated.
Fast Slew Rate: 200 pf between each power/ground pair
Medium Slew Rate: 300 pf between each power/ground pair
Slow Slew Rate: 400 pf between each power/ground pair
(4) Each output pin has individual slew rate control.

Three-state Buffer Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
3-state to Pad Active (no load)(2,3)	T_{3SOE}	4.5	3.7	3.3	ns
3-state to Pad Hi-Z (no load) (2,3)	T_{INIS1}	4.5	3.7	3.3	ns

Table 21: Three-state Buffer Delays

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Output delays are specified with no load. Add the following delays to adjust for loading.
Fast Slew Rate: 40 ps/pf
Medium Slew Rate: 60 ps/pf
Slow Slew Rate: 95 ps/pf
(3) Each output pin has individual slew rate control.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Output buffer combinatorial delay (no load)(2)	T_{OUTIS1}	5.2	3.9	2.9	ns
Output Register Set-up Time (global clock)	T_{OUTIS2}	3.4	2.6	2.0	ns
Output Register Hold Time (global clock)	T_{OUTIH1}	0	0	0	ns
Output Register Clock to Output (global clock, no load) (2)	T_{OUTCO1}	2.8	2.2	1.8	ns
I/O Register Clock Enable Setup Time	T_{CES1}	2.8	2.0	1.6	ns
I/O Register Clock Enable Hold Time	T_{CEH1}	0	0	0	ns
Input Register GSR set/reset delays	T_{GSRI}	3.5	2.6	2.1	ns
Output Register GSR set/reset delays	T_{GSRO}	2.9	2.3	1.9	ns
Input Register GSR set/reset setup time	T_{GSRIS1}	0.5	0.4	0.3	ns
Output Register GSR set/reset setup time	T_{GSROS1}	0.5	0.4	0.3	ns

Table 22: Input and Output Buffer Parameters (I/O Set to GTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Output delays are specified with no load. Add the following delays to adjust for loading.
GTL: 27 ps/pf

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input buffer combinatorial delay	T_{INPD}	5.3	4.0	3.2	ns
Input Register Set-up Time (global clock)	T_{INIS1}	3.2	2.4	1.9	ns
Input Register Hold Time (global clock)	T_{INIH1}	0	0	0	ns
Input Register Clock to Output (global clock)	T_{INCO1}	4.5	3.4	2.7	ns

Table 23: Input and Output Buffer Parameters (I/O Set to LV-PECL/LVDS)

Logic Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
3-input AND/OR to flip-flop delay	T_{ANDR3}	3.6	3.3	3.0	ns
6-input AND/OR to flip-flop delay	T_{ANDR6}	4.2	3.8	3.4	ns
9-input AND/OR to flip-flop delay	T_{ANDR9}	5.1	4.6	4.1	ns
4:1 Multiplexer data to flip-flop	T_{MUXR}	3.5	3.2	2.9	ns
4:1 Multiplexer select to flip-flop	T_{MUXSR}	3.5	3.2	2.9	ns
Adder/multiplier to flip-flop (sum)	T_{ADDCR}	4.6	3.6	3.2	ns
3-input AND/OR combinatorial delay	T_{ANDC3}	4.0	3.8	3.6	ns
6-input AND/OR combinatorial delay	T_{ANDC6}	4.7	4.3	3.9	ns
9-input AND/OR combinatorial delay	T_{ANDC9}	5.6	5.1	4.6	ns
Adder/Multiplier delay (sum)	T_{ADDC}	4.5	4.1	3.7	ns
4:1 Multiplexer data delay	T_{MUXC}	4.1	3.7	3.4	ns
4:1 Multiplexer select delay	T_{MUXS}	4.1	3.7	3.4	ns
D Flip-flop setup time	T_{SU}	0.7	0.6	0.5	ns
T Flip-flop setup time	T_{SUT}	0.9	0.8	0.7	ns
Flip-flop clock to out (GCLK or QCLK)	T_{COG}	2.0	1.8	1.6	ns
Flip-flop clock to out (LCK2)	T_{COL}	5.5	5.0	4.5	ns
GSR set/reset to flip-flop out	T_{GSRFF}	2.2	2.0	1.8	ns
LSR set/reset delay	T_{LSR}	5.9	5.4	4.9	ns
Logic Block Pass Through	T_{LBPT}	4.0	3.6	3.2	ns

Table 24: Logic Block Switching Parameters

(Includes All Routing Delays Within Routing Region(6))

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Industrial speed grade delays are 5% higher.
(3) Refer to figure 10 for a picture of the logic paths described in the above table.
(4) The AND/OR combinatorial delay, adder/multiplier delay and 4:1 multiplexer delay include the complete path through the logic block from inputs through outputs, connection buffers and routing to the next logic block or active repeater.
(5) The AND/OR to flip flop, 4:1 multiplexer data to flip-flop, 4:1 multiplexer select to flip-flop and adder/multiplier to flip flop delay includes all elements from inputs to the D/T input of either flip flop.
(6) Logic block delays shown in table 24 include all connection buffer and routing delays within a 9 block routing region. Additional delays are incurred only when a net must go through an active repeater to reach a block in another routing region. See table 27 for active repeater delays.

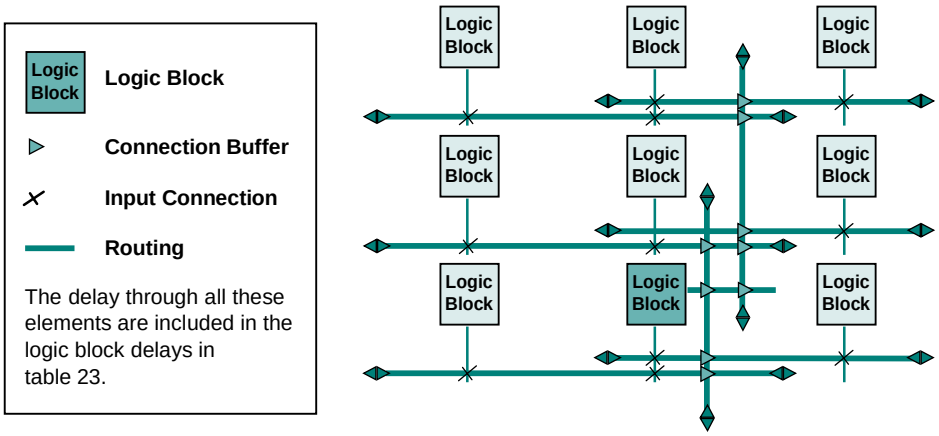


Figure 20: Logic Block Delays Includes Routing Within a Region

RAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Read/Write Operation		Max	Max	Max	
Address setup time before clock	T_{AS}	4.0	3.5	3.0	ns
Address hold time after clock	T_{AH}	0	0	0	ns
WE setup time before clock	T_{WS}	4.0	3.5	3.0	ns
WE hold time after clock	T_{WH}	0	0	0	ns
DIN setup time before clock	T_{DS}	4.0	3.5	3.0	ns
DIN hold time after clock	T_{DH}	0	0	0	ns
Clock min pulse width high (2)	T_{MPH}	5.0	5.0	5.0	ns
Read Cycle		Min	Min	Min	
Output data valid after clock	T_{ROS}	10.0	9.0	8.0	ns

Table 25: RAM Switching Parameters – Dual Port Mode

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Applies to RAM operation only. See table 19 for clock min pulse width high in all other operating modes.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Read/Write Operation		Max	Max	Max	
Address setup time before clock	T_{AS}	4.0	3.5	3.0	ns
Address hold time after clock	T_{AH}	0	0	0	ns
WE setup time before clock	T_{WS}	4.0	3.5	3.0	ns
WE hold time after clock	T_{WH}	0	0	0	ns
DIN setup time before clock	T_{DS}	4.0	3.5	3.0	ns
DIN hold time after clock	T_{DH}	0	0	0	ns
Read Cycle		Min	Min	Min	
Output data valid after clock	T_{ROS}	11.0	10.0	9.0	ns

Table 26: RAM Switching Parameters – Single Port Mode

Note:
All delays are specified over commercial voltage and temperature range.

Programmable Interconnect Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Horizontal Active Repeater Delay	T_{HRPT}	1.2	0.9	0.8	ns
Vertical Active Repeater Delay	T_{VRPT}	0.9	0.7	0.6	ns
Vertical to Horizontal Active Repeater Delay	T_{VHRPT}	1.2	0.9	0.8	ns
Horizontal to Vertical Active Repeater Delay	T_{HVRPT}	1.2	0.9	0.8	ns

Table 27: Active Repeater Switching Parameters

Note:
All delays are specified over commercial voltage and temperature range.

Pin Description

352-pin SBGA - DL6035

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
RESET	AE25	IO_46/QCLK1BLN	V25
STRPGM	AE24	IO_47/QCLK1BL	V23
PCKI/PCKO	AD22	IO_48	W26
SYSDONE	AE3	IO_49/DI(5)	W24
PLL1REST	B25	IO_50/QCLK2BLN	W25
PLL2REST	C3	IO_51/QCLK2BL	Y24
IO_2 (1)	C24	IO_52	Y25
IO_3	C25	IO_53/DI(4)	AA25
IO_4	E24	IO_54	Y23
IO_5	F23	IO_55/DI(3)	AB25
IO_6	D25	IO_56	AA24
IO_7	F24	IO_57/DI(2)	AA23
IO_8	B26	IO_58	AC26
IO_9	D26	IO_59/DI(1)	AB24
IO_10	G24	IO_60	AC25
IO_11	E25	IO_61/DI(0)	AD25
IO_12	H23	IO_62/TDO	AB23
IO_13	H24	IO_63	AD24
IO_14/QCLK1TLN	F25	IO_64	AC24
IO_15/QCLK1TL	J24	IO_65	AD23
IO_16	G25	IO_66	AF25
IO_17	K23	IO_67/M0	AC22
IO_18/QCLK2TLN	G26	IO_68	AE23
IO_19/QCLK2TL	K24	IO_69	AE22
IO_20	H25	IO_70/M1	AC21
IO_21	L23	IO_71	AF22
IO_22	J25	IO_72/M2	AD21
IO_23	L24	IO_73	AC20
IO_24	K25	IO_74/DONE	AE21
IO_25	L25	IO_75	AD20
IO_26	M23	IO_76/DOUT	AE20
IO_27	L26	IO_77	AE19
IO_28	M24	IO_78	AD19
IO_29	N23	IO_79	AE18
IO_30/GCLK1N	M25	IO_80	AC18
IO_31/GCLK1	N24	IO_81	AD18
IO_32	N25	IO_82	AF18
IO_33	P24	IO_83	AC17
IO_34	N26	IO_84	AE17
IO_35	R24	IO_85	AE16
IO_36	P25	IO_86	AD17
IO_37/WE	R25	IO_87	AF16
IO_38	R23	IO_88	AC16
IO_39/RDY	T25	IO_89	AD16
IO_40	T24	IO_90	AE15
IO_41/DI(7)	T23	IO_91	AC15
IO_42	U26	IO_92	AE14
IO_43/DI(6)	U24	IO_93	AF13
IO_44	U25	IO_94	AD15
IO_45	V24	IO_95	AE13

Table 28: DL6035/352 Pin Description

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
IO_96	AD14	IO_149/QCLK1BRN	U3
IO_97	AE12	IO_150	U2
IO_98	AD13	IO_151	T4
IO_99	AD12	IO_152	T2
IO_100	AC13	IO_153	R2
IO_101	AC12	IO_154	T3
IO_102	AF11	IO_155	P2
IO_103	AD11	IO_156	R3
IO_104	AE11	IO_157	P4
IO_105	AE10	IO_158	P1
IO_106	AC11	IO_159	P3
IO_107	AE9	IO_160/GSR	N2
IO_108	AD10	IO_161	N3
IO_109	AD9	IO_162	M2
IO_110	AE8	IO_163	M3
IO_111	AC9	IO_164/GCLK2	L2
IO_112	AE7	IO_165/GCLK2N	K1
IO_113	AF6	IO_166	M4
IO_114	AD8	IO_167	K2
IO_115	AE6	IO_168	L3
IO_116	AD7	IO_169	L4
IO_117	AC7	IO_170	J2
IO_118	AE5	IO_171	K3
IO_119	AD6	IO_172	H1
IO_120	AF4	IO_173	K4
IO_121	AF2	IO_174	H2
IO_122	AC6	IO_175	J3
IO_123	AE4	IO_176/QCLK2TR	G2
IO_124	AD5	IO_177/QCLK2TRN	F1
IO_125	AC5	IO_178	J4
IO_126	AD3	IO_179	F2
IO_127/TMS	AD4	IO_180/QCLK1TR	H3
IO_128/TCK	AE2	IO_181/QCLK1TRN	G3
IO_129/TDI	AD2	IO_182	E2
IO_130	AC3	IO_183	G4
IO_131	AC2	IO_184	D1
IO_132	AB4	IO_185	D2
IO_133	AB3	IO_186	F3
IO_134	AE1	IO_187	C2
IO_135	AA3	IO_188	F4
IO_136	AB2	IO_189	E3
IO_137	AB1	IO_190	D3
IO_138	Y4	IO_191	B2
IO_139	AA2	IO_193 (2)	C4
IO_140	Y3	IO_194	B3
IO_141	W4	IO_195	C5
IO_142	Y2	IO_196	B4
IO_143	W3	IO_197	A3
IO_144/QCLK2BR	W2	IO_198	D6
IO_145/QCKL2BRN	V3	IO_199	B5
IO_146	V2	IO_200	C7
IO_147	U4	IO_201	D8
IO_148/QCLK1BR	V1	IO_202	A5

Table 28: DL6035/352 Pin Description

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
IO_203	C8	IO_256	B23
IO_204	C6	VCC_IO	B1
IO_205	B6	VCC_IO	E1
IO_206	D9	VCC_IO	L1
IO_207	B7	VCC_IO	R1
IO_208	C9	VCC_IO	W1
IO_209	C10	VCC_IO	AC1
IO_210	B8	VCC_IO	AF5
IO_211	D11	VCC_IO	AF9
IO_212	A8	VCC_IO	AF12
IO_213	B9	VCC_IO	AF17
IO_214	C11	VCC_IO	AF20
IO_215	B10	VCC_IO	AF23
IO_216	D12	VCC_IO	AD26
IO_217	C12	VCC_IO	Y26
IO_218	A10	VCC_IO	T26
IO_219	C13	VCC_IO	K26
IO_220	B11	VCC_IO	H26
IO_221	B12	VCC_IO	C26
IO_222	C14	VCC_IO	A23
IO_223	B13	VCC_IO	A18
IO_224	D14	VCC_IO	A16
IO_225	A14	VCC_IO	A12
IO_226	C15	VCC_IO	A9
IO_227	B14	VCC_IO	A4
IO_228	D15	VCC_CORE/CLK	C1
IO_229	C16	VCC_CORE/CLK	J1
IO_230	A15	VCC_CORE/CLK	M1
IO_231	D16	VCC_CORE/CLK	T1
IO_232	B15	VCC_CORE/CLK	AA1
IO_233	B16	VCC_CORE/CLK	AD1
IO_234	C17	VCC_CORE/CLK	AF3
IO_235	B17	VCC_CORE/CLK	AF8
IO_236	D17	VCC_CORE/CLK	AF15
IO_237	C18	VCC_CORE/CLK	AF21
IO_238	B18	VCC_CORE/CLK	AF24
IO_239	C19	VCC_CORE/CLK	AE26
IO_240	A19	VCC_CORE/CLK	AB26
IO_241	B19	VCC_CORE/CLK	R26
IO_242	D19	VCC_CORE/CLK	M26
IO_243	B20	VCC_CORE/CLK	J26
IO_244	C20	VCC_CORE/CLK	E26
IO_245	C21	VCC_CORE/CLK	A24
IO_246	A21	VCC_CORE/CLK	A17
IO_247	D21	VCC_CORE/CLK	A11
IO_248	B21	VCC_CORE/CLK	A6
IO_249	A22	VCC_CORE/CLK	A2
IO_250	C22	VCC_PLL	E4
IO_251	B22	VCC_PLL	E23
IO_252	B24	GND_IO	D4
IO_253	C23	GND_IO	H4
IO_254	A25	GND_IO	N4
IO_255	D24	GND_IO	R4

Table 28: DL6035/352 Pin Description

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
GND_IO	V4	GND_CORE/CLK	G1
GND_IO	AA4	GND_CORE/CLK	N1
GND_IO	AC4	GND_CORE/CLK	U1
GND_IO	AC8	GND_CORE/CLK	Y1
GND_IO	AC10	GND_CORE/CLK	AF1
GND_IO	AC14	GND_CORE/CLK	AF7
GND_IO	AC19	GND_CORE/CLK	AF10
GND_IO	AC23	GND_CORE/CLK	AF14
GND_IO	W23	GND_CORE/CLK	AF19
GND_IO	U23	GND_CORE/CLK	AF26
GND_IO	P23	GND_CORE/CLK	AA26
GND_IO	J23	GND_CORE/CLK	V26
GND_IO	G23	GND_CORE/CLK	P26
GND_IO	D23	GND_CORE/CLK	F26
GND_IO	D20	GND_CORE/CLK	A26
GND_IO	D18	GND_CORE/CLK	A20
GND_IO	D13	GND_CORE/CLK	A13
GND_IO	D10	GND_CORE/CLK	A7
GND_IO	D7	GND_PLL	D5
GND_CORE/CLK	A1	GND_PLL	D22

Table 28: DL6035/352 Pin Description

Notes:
(1) IO_1 is not available due to the PLL1REST.
(2) IO_192 is not available due to the PLL2REST.

208-pin QFP - DL6035

Pin Description	208 QFP Pin No.	Pin Description	208 QFP Pin No.
VCC_PLL	1	VCC_CK	53
GND_CK	2	IO_128 TCK	54
VCC_CK	3	IO_127 TMS	55
GND_INT	4	SYSDONE	56
PLL2REST	5	IO_124	57
IO_190	6	IO_123	58
VCC_INT	7	GND_IO	59
IO_187	8	GND_INT	60
GND_IO	9	IO_120	61
IO_184	10	IO_119	62
VCC_IO	11	VCC_IO	63
IO_181 QCLK1TRN	12	VCC_INT	64
IO_180 QCLK1TR	13	IO_116	65
IO_177 QCLK2TRN	14	IO_115	66
SUBN-GND	15	IO_112	67
IO_176 QCLK2TR	16	IO_111	68
IO_172	17	IO_108	69
IO_171	18	IO_107	70
GND_IO	19	GND_IO	71
GND_INT	20	GND_INT	72
VCC_IO	21	IO_104	73
IO_166	22	VCC_IO	74
IO_165 GCLK2N	23	VCC_INT	75
IO_164 GCLK2	24	IO_99	76
IO_163	25	IO_96	77
GND_IO	26	IO_93	78
IO_161	27	IO_92	79
VCC_CK	28	IO_91	80
GND_CK	29	GND_IO	81
IO_160 GSR	30	IO_89	82
IO_159	31	VCC_INT	83
VCC_IO	32	IO_88	84
IO_157	33	IO_87	85
IO_156	34	VCC_IO	86
IO_155	35	GND_INT	87
GND_IO	36	IO_84	88
IO_153	37	IO_83	89
IO_152	38	IO_80	90
VCC_IO	39	IO_79	91
IO_149 QCLK1BRN	40	IO_76 DOUT	92
IO_148 QCLK1BR	41	GND_IO	93
IO_145 QCKL2BRN	42	IO_74 DONE	94
IO_144 QCLK2BR	43	VCC_INT	95
GND_INT	44	IO_72 M2	96
GND_IO	45	VCC_IO	97
VCC_INT	46	IO_70 M1	98
IO_136	47	PCKI/PCKO	99
VCC_IO	48	IO_68	100
6035 IO_131 **6035X** GTL_REF_EXT	49	IO_67 M0	101
IO_129 TDI	50	STRPGM	102
Blank Pin on the 35K 208 QFP	51	VCC_CK	103
GND_CK	52	GND_INT	104

Table 29: DL6035/208 Pin Description

Pin Description	208 QFP Pin No.	Pin Description	208 QFP Pin No.
GND_CK	105	GND_PLL	157
RESET	106	IO_256	158
IO_62 TDO	107	IO_255	159
IO_61 DI(0)	108	VCC_IO	160
VCC_INT	109	IO_254	161
IO_59 DI(1)	110	IO_253	162
GND_IO	111	VCC_INT	163
IO_57 DI(2)	112	GND_IO	164
GND_INT	113	IO_250	165
IO_55 DI(3)	114	GND_INT	166
VCC_IO	115	IO_246	167
IO_53 DI(4)	116	IO_245	168
IO_51 QCLK2BL	117	IO_242	169
IO_50 QCLK2BLN	118	IO_241	170
IO_49 DI(5)	119	VCC_IO	171
IO_47 QCLK1BL	120	IO_238	172
IO_46 QCLK1BLN	121	VCC_INT	173
IO_43 DI(6)	122	GND_IO	174
GND_IO	123	IO_234	175
IO_42	124	GND_INT	176
IO_41 DI(7)	125	IO_231	177
IO_39 RDY	126	IO_230	178
VCC_IO	127	IO_227	179
IO_37 WE	128	GND_IO	180
IO_35	129	IO_226	181
IO_34	130	IO_224	182
GND_CK	131	IO_223	183
VCC_CK	132	VCC_IO	184
IO_31 GCLK1	133	IO_222	185
IO_30 GCLK1N	134	IO_221	186
IO_28	135	IO_220	187
GND_IO	136	IO_219	188
IO_23	137	GND_IO	189
VCC_IO	138	IO_218	190
IO_19 QCLK2TL	139	IO_217	191
IO_18 QCLK2TLN	140	VCC_IO	192
IO_15 QCLK1TL	141	IO_214	193
IO_14 QCLK1TN	142	IO_213	194
IO_11	143	IO_210	195
GND_IO	144	IO_209	196
IO_8	145	IO_206	197
IO_7	146	IO_205	198
VCC_IO	147	GND_INT	199
IO_5	148	GND_IO	200
GND_INT	149	IO_202	201
IO_4	150	IO_201	202
IO_3	151	VCC_INT	203
PLL1REST	152	VCC_IO	204
VCC_INT	153	IO_198	205
VCC_CK	154	IO_194	206
GND_CK	155	IO_193	207
VCC_PLL	156	GND_PLL	208

Table 29: DL6035/208 Pin Description

352-pin SBGA - DL6020

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
RESET	AE25	IO_59/DI(1)	AB24
STRPGM	AE24	IO_61/DI(0)	AD25
PCKI/PCKO	AD22	IO_62/TDO	AB23
SYSDONE	AE3	IO_63	AD24
PLL1REST	B25	IO_64	AC24
PLL2REST	C3	IO_65	AD23
IO_2	C24	IO_66	AF25
IO_3	C25	IO_67/M0	AC22
IO_4	E24	IO_68	AE23
IO_5	F23	IO_69	AE22
IO_6	D25	IO_70/M1	AC21
IO_7	F24	IO_72/M2	AD21
IO_8	B26	IO_74/DONE	AE21
IO_9	D26	IO_76/DOUT	AE20
IO_10	G24	IO_77	AE19
IO_11	E25	IO_78	AD19
IO_12	H23	IO_79	AE18
IO_13	H24	IO_81	AD18
IO_14/QCLK1TLN	F25	IO_82	AF18
IO_15/QCLK1TL	J24	IO_83	AC17
IO_17	K23	IO_85	AE16
IO_18/QCLK2TLN	G26	IO_87	AF16
IO_19/QCLK2TL	K24	IO_88	AC16
IO_20	H25	IO_89	AD16
IO_22	J25	IO_91	AC15
IO_24	K25	IO_93	AF13
IO_25	L25	IO_94	AD15
IO_26	M23	IO_95	AE13
IO_28	M24	IO_96	AD14
IO_30/GCLK1N	M25	IO_98	AD13
IO_31/GCLK1	N24	IO_99	AD12
IO_32	N25	IO_100	AC13
IO_33	P24	IO_101	AC12
IO_34	N26	IO_102	AF11
IO_35	R24	IO_103	AD11
IO_36	P25	IO_105	AE10
IO_37/WE	R25	IO_106	AC11
IO_39/RDY	T25	IO_108	AD10
IO_41/DI(7)	T23	IO_110	AE8
IO_43/DI(6)	U24	IO_112	AE7
IO_44	U25	IO_113	AF6
IO_46/QCLK1BLN	V25	IO_115	AE6
IO_47/QCLK1BL	V23	IO_117	AC7
IO_49/DI(5)	W24	IO_118	AE5
IO_50/QCLK2BLN	W25	IO_119	AD6
IO_51/QCLK2BL	Y24	IO_120	AF4
IO_53/DI(4)	AA25	IO_122	AC6
IO_55/DI(3)	AB25	IO_123	AE4
IO_57/DI(2)	AA23	IO_124	AD5
IO_58	AC26	IO_125	AC5

Table 30: DL6020 Pin Description

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
IO_126	AD3	IO_196	B4
IO_127/TMS	AD4	IO_197	A3
IO_128/TCK	AE2	IO_198	D6
IO_129/TDI	AD2	IO_199	B5
IO_130	AC3	IO_201	D8
IO_131	AC2	IO_202	A5
IO_132	AB4	IO_204	C6
IO_133	AB3	IO_205	B6
IO_134	AE1	IO_207	B7
IO_135	AA3	IO_208	C9
IO_137	AB1	IO_210	B8
IO_138	Y4	IO_212	A8
IO_139	AA2	IO_213	B9
IO_140	Y3	IO_215	B10
IO_142	Y2	IO_216	D12
IO_143	W3	IO_217	C12
IO_144/QCLK2BR	W2	IO_219	C13
IO_145/QCKL2BRN	V3	IO_221	B12
IO_146	V2	IO_222	C14
IO_148/QCLK1BR	V1	IO_223	B13
IO_149/QCLK1BRN	U3	IO_224	D14
IO_151	T4	IO_225	A14
IO_152	T2	IO_226	C15
IO_154	T3	IO_227	B14
IO_156	R3	IO_229	C16
IO_158	P1	IO_230	A15
IO_159	P3	IO_232	B15
IO_160/GSR	N2	IO_233	B16
IO_162	M2	IO_235	B17
IO_164/GCLK2	L2	IO_237	C18
IO_165/GCLK2N	K1	IO_238	B18
IO_167	K2	IO_240	A19
IO_168	L3	IO_242	D19
IO_170	J2	IO_243	B20
IO_171	K3	IO_245	C21
IO_173	K4	IO_247	D21
IO_174	H2	IO_248	B21
IO_176/QCLK2TR	G2	IO_249	A22
IO_177/QCLK2TRN	F1	IO_250	C22
IO_178	J4	IO_251	B22
IO_180/QCLK1TR	H3	IO_252	B24
IO_181/QCLK1TRN	G3	IO_253	C23
IO_183	G4	IO_254	A25
IO_185	D2	IO_255	D24
IO_186	F3	IO_256	B23
IO_187	C2	VCC_IO	B1
IO_188	F4	VCC_IO	E1
IO_189	E3	VCC_IO	L1
IO_190	D3	VCC_IO	R1
IO_191	B2	VCC_IO	W1
IO_193	C4	VCC_IO	AC1
IO_194	B3	VCC_IO	AF5
IO_195	C5	VCC_IO	AF9

Table 30: DL6020 Pin Description

Pin Description	352 SBGA Ball No.
VCC_IO	AF12
VCC_IO	AF17
VCC_IO	AF20
VCC_IO	AF23
VCC_IO	AD26
VCC_IO	Y26
VCC_IO	T26
VCC_IO	K26
VCC_IO	H26
VCC_IO	C26
VCC_IO	A23
VCC_IO	A18
VCC_IO	A16
VCC_IO	A12
VCC_IO	A9
VCC_IO	A4
VCC_CORE/CLK	C1
VCC_CORE/CLK	J1
VCC_CORE/CLK	M1
VCC_CORE/CLK	T1
VCC_CORE/CLK	AA1
VCC_CORE/CLK	AD1
VCC_CORE/CLK	AF3
VCC_CORE/CLK	AF8
VCC_CORE/CLK	AF15
VCC_CORE/CLK	AF21
VCC_CORE/CLK	AF24
VCC_CORE/CLK	AE26
VCC_CORE/CLK	AB26
VCC_CORE/CLK	R26
VCC_CORE/CLK	M26
VCC_CORE/CLK	J26
VCC_CORE/CLK	E26
VCC_CORE/CLK	A24
VCC_CORE/CLK	A17
VCC_CORE/CLK	A11
VCC_CORE/CLK	A6
VCC_CORE/CLK	A2
VCC_PLL	E4
VCC_PLL	E23
GND_IO	D4
GND_IO	H4

Pin Description	352 SBGA Ball No.
GND_IO	N4
GND_IO	R4
GND_IO	V4
GND_IO	AA4
GND_IO	AC4
GND_IO	AC8
GND_IO	AC10
GND_IO	AC14
GND_IO	AC19
GND_IO	AC23
GND_IO	W23
GND_IO	U23
GND_IO	P23
GND_IO	J23
GND_IO	G23
GND_IO	D23
GND_IO	D20
GND_IO	D18
GND_IO	D13
GND_IO	D10
GND_IO	D7
GND_CORE/CLK	A1
GND_CORE/CLK	G1
GND_CORE/CLK	N1
GND_CORE/CLK	U1
GND_CORE/CLK	Y1
GND_CORE/CLK	AF1
GND_CORE/CLK	AF7
GND_CORE/CLK	AF10
GND_CORE/CLK	AF14
GND_CORE/CLK	AF19
GND_CORE/CLK	AF26
GND_CORE/CLK	AA26
GND_CORE/CLK	V26
GND_CORE/CLK	P26
GND_CORE/CLK	F26
GND_CORE/CLK	A26
GND_CORE/CLK	A20
GND_CORE/CLK	A13
GND_CORE/CLK	A7
GND_PLL	D5
GND_PLL	D22

Table 30: DL6020 Pin Description

Note:
Pins that are not shown should be left disconnected on the board.

352-pin SBGA - DL6009

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
RESET	AE25	IO_93	AF13
STRPGM	AE24	IO_94	AD15
PCKI/PCKO	AD22	IO_96	AD14
SYSDONE	AE3	IO_98	AD13
PLL1REST	B26	IO_101	AC12
PLL2REST	C3	IO_103	AD11
IO_3	C25	IO_105	AE10
IO_5	F23	IO_106	AC11
IO_7	F24	IO_108	AD10
IO_9	D26	IO_110	AE8
IO_11	E25	IO_112	AE7
IO_14/QCLK1TLN	F25	IO_115	AE6
IO_15/QCLK1TL	J24	IO_117	AC7
IO_18/QCLK2TLN	G26	IO_120	AF4
IO_19/QCLK2TL	K24	IO_122	AC6
IO_22	J25	IO_123	AE4
IO_26	M23	IO_125	AC5
IO_30/GCLK1N	M25	IO_127/TMS	AD4
IO_31/GCLK1	N24	IO_128/TCK	AE2
IO_33	P24	IO_129/TDI	AD2
IO_35	R24	IO_132	AB4
IO_37/WE	R25	IO_135	AA3
IO_39/RDY	T25	IO_137	AB1
IO_41/DI(7)	T23	IO_138	Y4
IO_43/DI(6)	U24	IO_140	Y3
IO_46/QCLK1BLN	V25	IO_142	Y2
IO_47/QCLK1BL	V23	IO_144/QCLK2BR	W2
IO_49/DI(5)	W24	IO_145/QCKL2BRN	V3
IO_50/QCLK2BLN	W25	IO_148/QCLK1BR	V1
IO_51/QCLK2BL	Y24	IO_149/QCLK1BRN	U3
IO_53/DI(4)	AA25	IO_151	T4
IO_55/DI(3)	AB25	IO_154	T3
IO_57/DI(2)	AA23	IO_156	R3
IO_59/DI(1)	AB24	IO_158	P1
IO_61/DI(0)	AD25	IO_159	P3
IO_62/TDO	AB23	IO_160/GSR	N2
IO_64	AC24	IO_162	M2
IO_65	AD23	IO_164/GCLK2	L2
IO_67/M0	AC22	IO_165/GCLK2N	K1
IO_68	AE23	IO_167	K2
IO_70/M1	AC21	IO_170	J2
IO_72/M2	AD21	IO_173	K4
IO_74/DONE	AE21	IO_176/QCLK2TR	G2
IO_76/DOUT	AE20	IO_177/QCLK2TRN	F1
IO_79	AE18	IO_180/QCLK1TR	H3
IO_82	AF18	IO_181/QCLK1TRN	G3
IO_85	AE16	IO_183	G4
IO_88	AC16	IO_185	D2
IO_89	AD16	IO_188	F4
IO_91	AC15	IO_189	E3

Table 31: DL6009 Pin Description

Pin Description	352 SBGA Ball No.
IO_194	B3
IO_196	B4
IO_198	D6
IO_199	B5
IO_201	D8
IO_202	A5
IO_204	C6
IO_205	B6
IO_207	B7
IO_210	B8
IO_212	A8
IO_213	B9
IO_216	D12
IO_219	C13
IO_222	C14
IO_223	B13
IO_226	C15
IO_229	C16
IO_232	B15
IO_233	B16
IO_235	B17
IO_237	C18
IO_240	A19
IO_242	D19
IO_245	C21
IO_247	D21
IO_249	A22
IO_251	B22
IO_252	B24
IO_253	C23
IO_255	D24
IO_256	B23
VCC_IO	B1
VCC_IO	E1
VCC_IO	L1
VCC_IO	R1
VCC_IO	W1
VCC_IO	AC1
VCC_IO	AF5
VCC_IO	AF9
VCC_IO	AF12
VCC_IO	AF17
VCC_IO	AF20
VCC_IO	AF23
VCC_IO	AD26
VCC_IO	Y26
VCC_IO	T26
VCC_IO	K26
VCC_IO	H26
VCC_IO	C26
VCC_IO	A23
VCC_IO	A18
VCC_IO	A16

Pin Description	352 SBGA Ball No.
VCC_IO	A12
VCC_IO	A9
VCC_IO	A4
VCC_CORE/CLK	C1
VCC_CORE/CLK	J1
VCC_CORE/CLK	M1
VCC_CORE/CLK	T1
VCC_CORE/CLK	AA1
VCC_CORE/CLK	AD1
VCC_CORE/CLK	AF3
VCC_CORE/CLK	AF8
VCC_CORE/CLK	AF15
VCC_CORE/CLK	AF21
VCC_CORE/CLK	AF24
VCC_CORE/CLK	AE26
VCC_CORE/CLK	AB26
VCC_CORE/CLK	R26
VCC_CORE/CLK	M26
VCC_CORE/CLK	J26
VCC_CORE/CLK	E26
VCC_CORE/CLK	A24
VCC_CORE/CLK	A17
VCC_CORE/CLK	A11
VCC_CORE/CLK	A6
VCC_CORE/CLK	A2
VCC_PLL	E4
VCC_PLL	E23
GND_IO	D4
GND_IO	H4
GND_IO	N4
GND_IO	R4
GND_IO	V4
GND_IO	AA4
GND_IO	AC4
GND_IO	AC8
GND_IO	AC10
GND_IO	AC14
GND_IO	AC19
GND_IO	AC23
GND_IO	W23
GND_IO	U23
GND_IO	P23
GND_IO	J23
GND_IO	G23
GND_IO	D23
GND_IO	D20
GND_IO	D18
GND_IO	D13
GND_IO	D10
GND_IO	D7
GND_CORE/CLK	A1
GND_CORE/CLK	G1
GND_CORE/CLK	N1

Table 31: DL6009 Pin Description

Pin Description	352 SBGA Ball No.	Pin Description	352 SBGA Ball No.
GND_CORE/CLK	U1	GND_CORE/CLK	V26
GND_CORE/CLK	Y1	GND_CORE/CLK	P26
GND_CORE/CLK	AF1	GND_CORE/CLK	F26
GND_CORE/CLK	AF7	GND_CORE/CLK	A26
GND_CORE/CLK	AF10	GND_CORE/CLK	A20
GND_CORE/CLK	AF14	GND_CORE/CLK	A13
GND_CORE/CLK	AF19	GND_CORE/CLK	A7
GND_CORE/CLK	AF26	GND_PLL	D5
GND_CORE/CLK	AA26	GND_PLL	D22

Table 31: DL6009 Pin Description

Note:
Pins that are not shown should be left disconnected on the board.

Package Drawings

352-pin SBGA

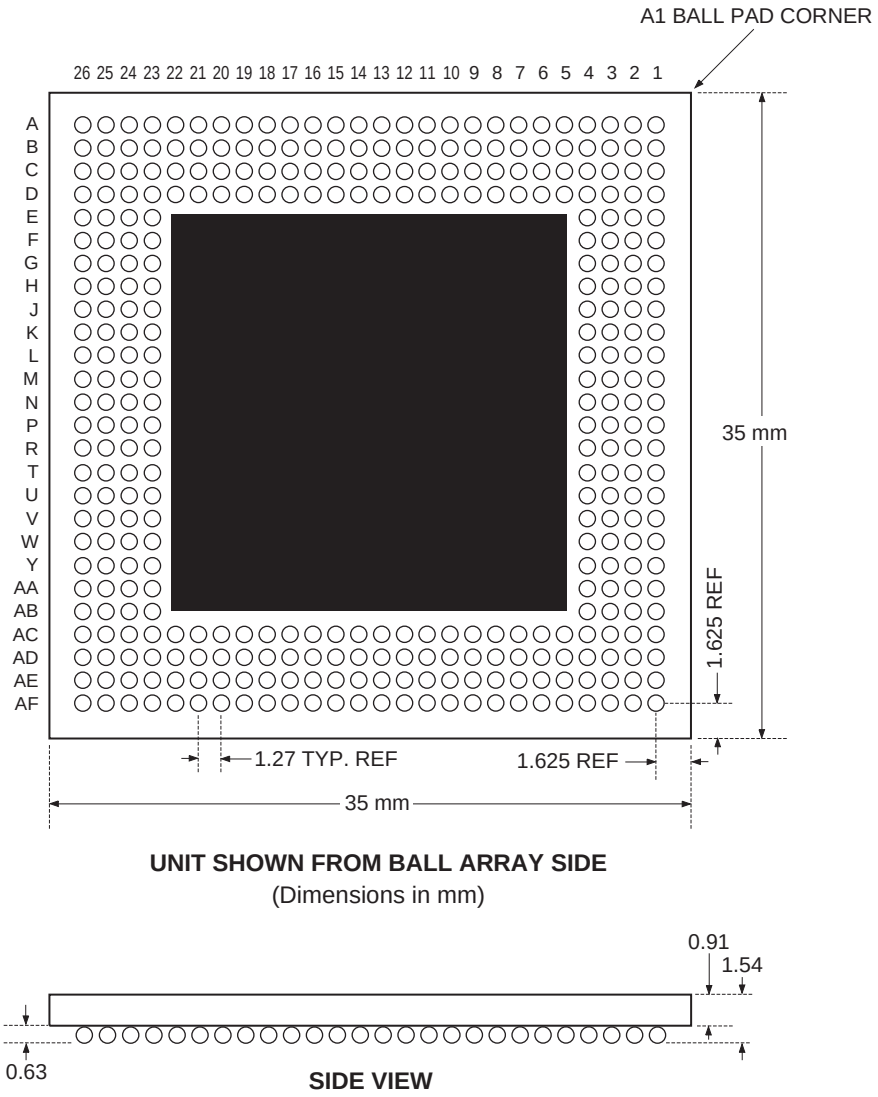


Figure 21: Package Drawing of 352-pin SBGA

208-pin Thermal Enhanced PQFP (PQ208)

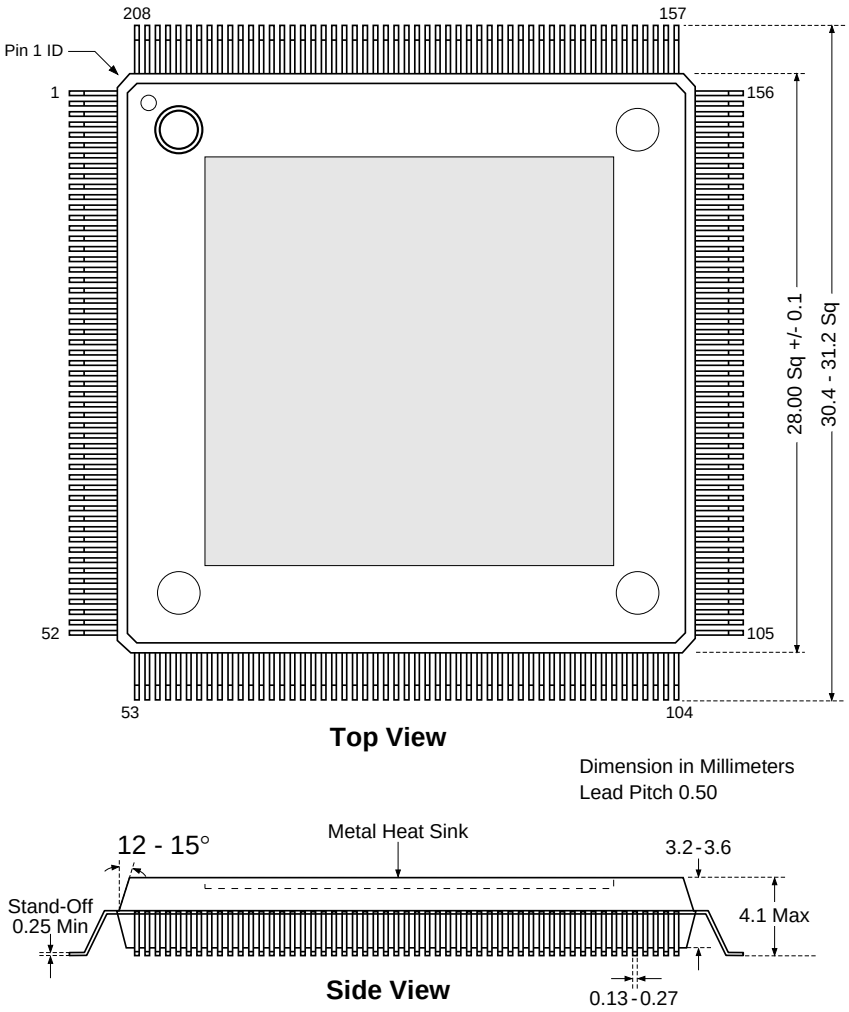
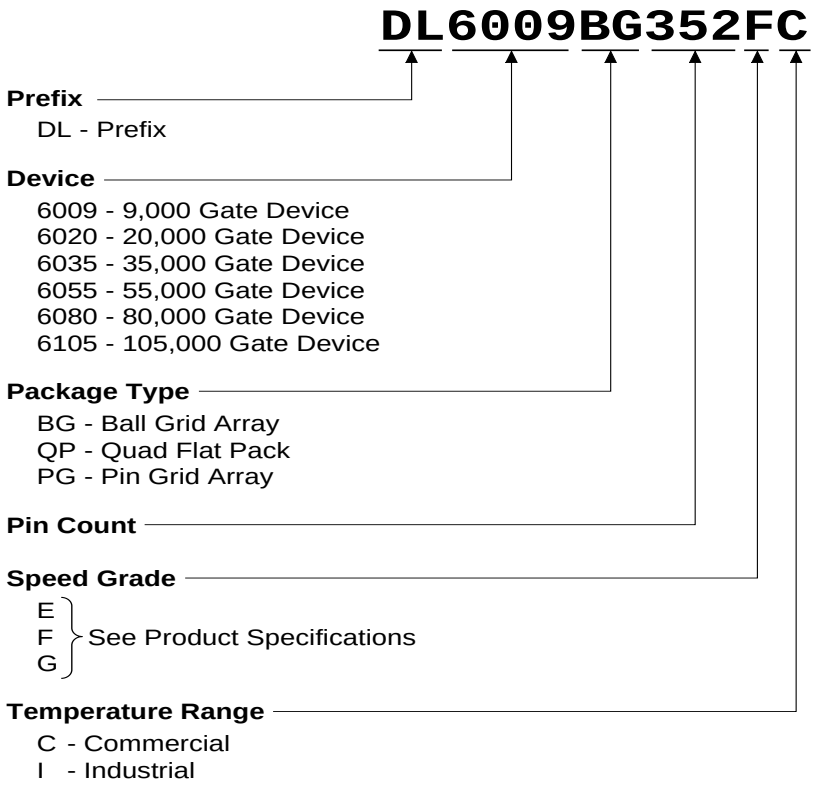


Figure 22: Package Drawing of 208-pin PQFP

Ordering Information

Order codes are shown below.



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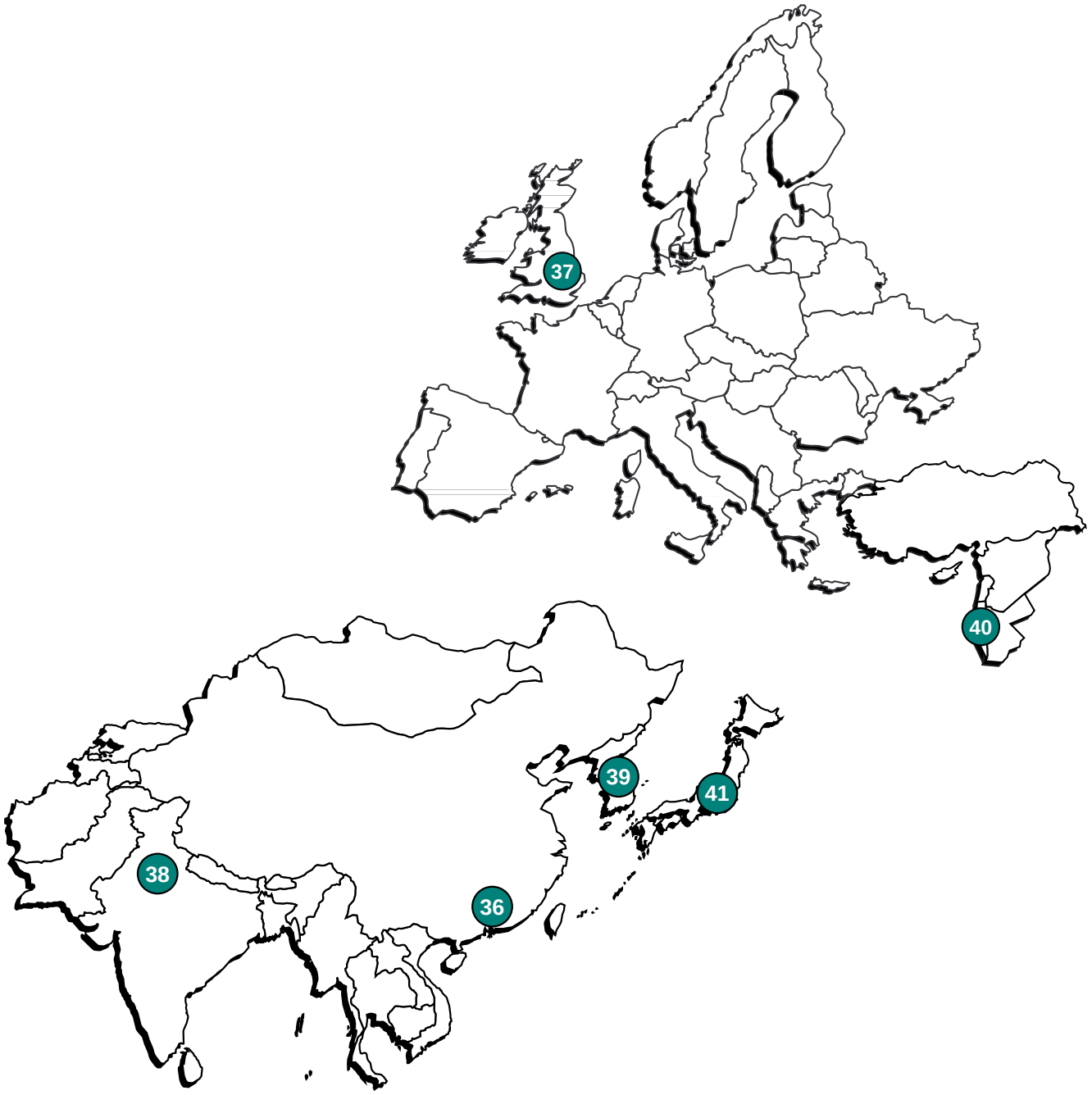

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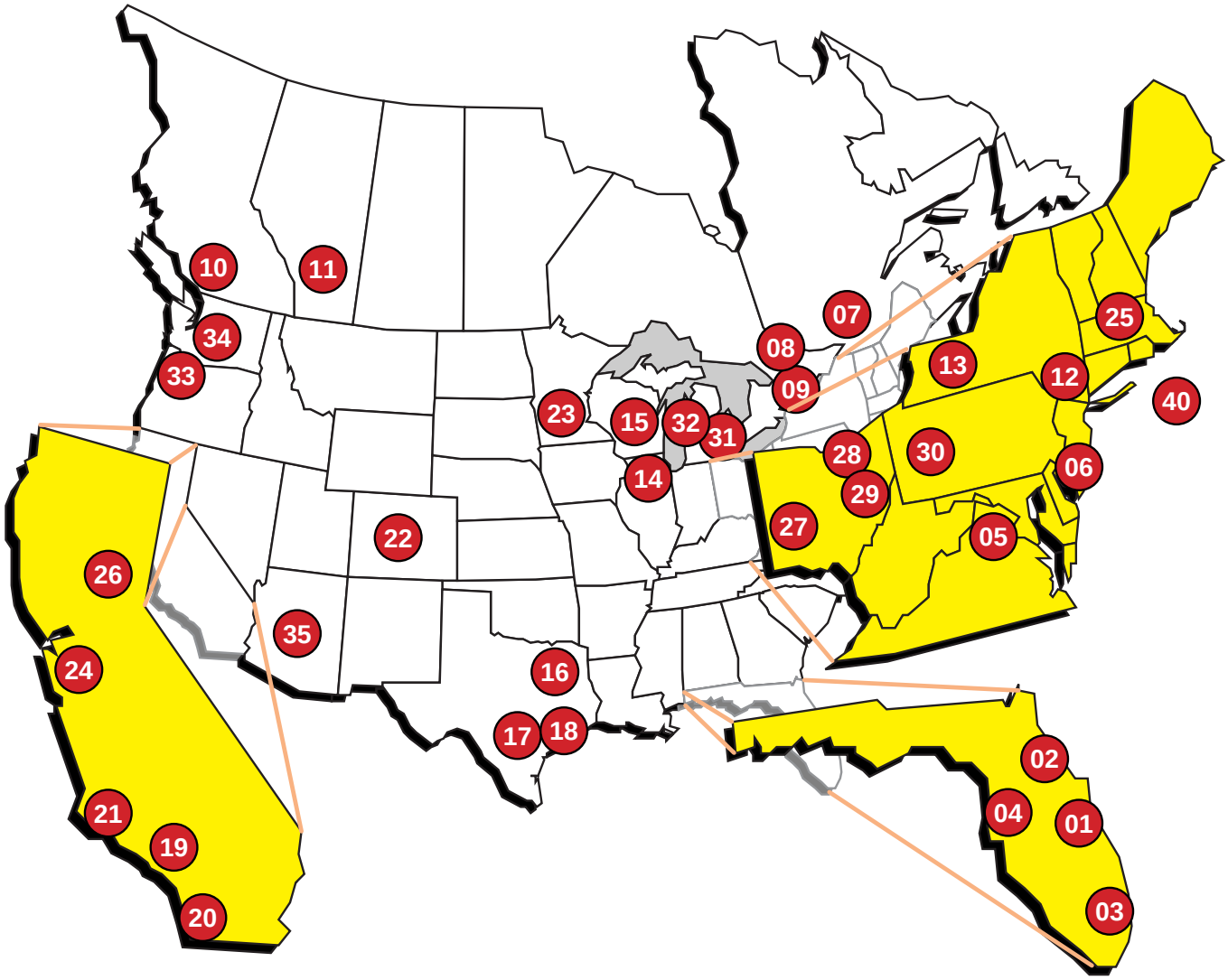

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