

## DM74LS166 8-Bit Parallel-In/Serial-Out Shift Register

### General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When HIGH, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When LOW, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

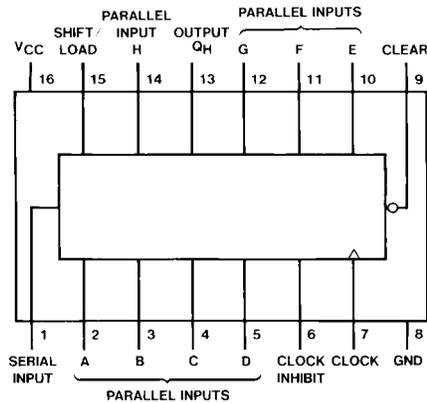
Clocking is accomplished on the LOW-to-HIGH level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs HIGH inhibits clocking; holding either LOW enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is HIGH. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

### Ordering Code:

Order Number	Package Number	Package Description
DM74LS166M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS166WM	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS166N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

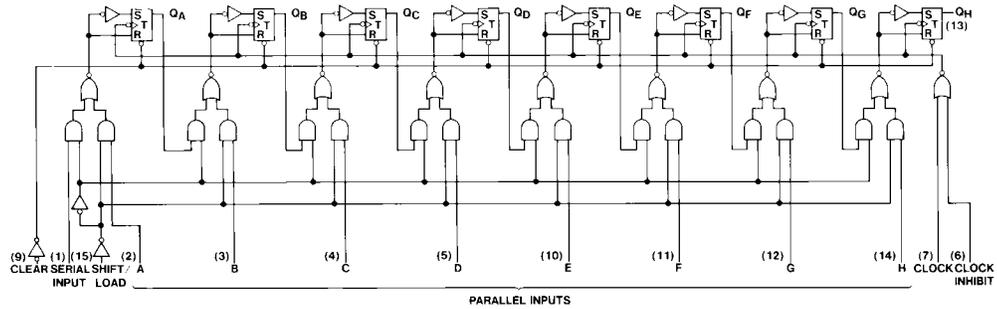


### Function Table

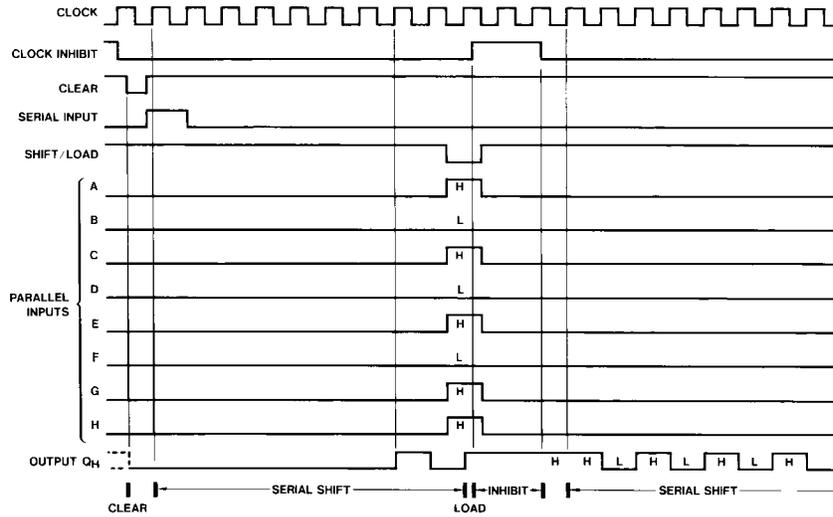
Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock	Clock	Serial	Parallel	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>H</sub>
					A...H			
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q <sub>An</sub>	Q <sub>Gn</sub>
H	H	L	↑	L	X	L	Q <sub>An</sub>	Q <sub>Gn</sub>
H	X	H	↑	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>H0</sub>

H = HIGH Level (steady state)  
 L = LOW Level (steady state)  
 X = Don't Care (any input, including transitions)  
 ↑ = Transition from LOW-to-HIGH level  
 a...h = The level of steady-state input at inputs A through H, respectively  
 Q<sub>A0</sub>, Q<sub>B0</sub>, Q<sub>H0</sub> = The level of Q<sub>A</sub>, Q<sub>B</sub>, Q<sub>H</sub>, respectively, before the indicated steady-state input conditions were established  
 Q<sub>An</sub>, Q<sub>Gn</sub> = The level of Q<sub>A</sub>, Q<sub>G</sub>, respectively, before the most recent ↑ transition of the clock

### Logic Diagram



### Timing Diagram



Typical Clear, Shift, Load, Inhibit and Shift Sequences

**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			-0.4	mA
$I_{OL}$	LOW Level Output Current			8	mA
$f_{CLK}$	Clock Frequency (Note 2)	0		25	MHz
	Clock Frequency (Note 3)	0		20	MHz
$t_W$	Pulse Width (Note 4)	Clock	20		ns
		Clear	20		
$t_{SU}$	Setup Time (Note 4)	Mode	30		ns
		Data	20		
$t_H$	Hold Time (Note 4)	0			ns
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 2:**  $C_L = 15$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 3:**  $C_L = 50$  pF,  $R_L = 2$  k $\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 4:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -18$ mA			-1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$	2.7	3.4		V
		$V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$				
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$		0.35	0.5	V
		$V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$				
		$I_{OL} = 4$ mA, $V_{CC} = \text{Min}$				
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 7\text{V}$			0.1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 2.7\text{V}$			20	$\mu\text{A}$
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 0.4\text{V}$			-0.4	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 6)	-20		-100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 7)		22	38	mA

**Note 5:** All typicals are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 6:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

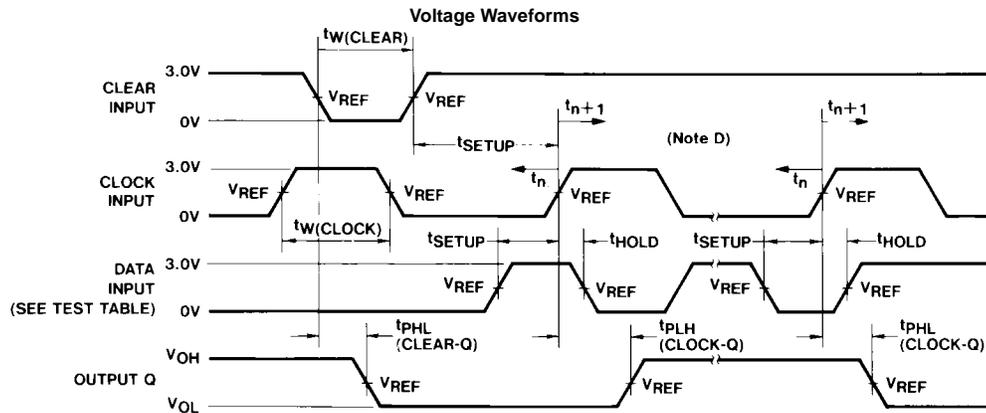
**Note 7:** With all outputs OPEN, 4.5V applied to the serial input, all other inputs except the CLOCK grounded,  $I_{CC}$  is measured after a momentary ground, then 4.5V is applied to the CLOCK.

## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\text{ k}\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		25		20		MHz
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Output	8	35		38	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Output	8	35		41	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Output	6	30		36	ns

## Parameter Measurement Information



**Test Table for Synchronous Inputs**

Data Input for Test	Shift/Load	Output Tested (See Note C)
H	0V	$Q_H$ at $T_{N+1}$
Serial Input	4.5V	$Q_H$ at $T_{N+8}$

**Note A:** The clock pulse has the following characteristics:  $t_{W(\text{clock})} \geq 20\text{ ns}$  and  $\text{PRR} = 1\text{ MHz}$ . The clear pulse has the following characteristics:

$t_{W(\text{clear})} \geq 20\text{ ns}$  and  $t_{\text{HOLD}} = 0\text{ ns}$ . When testing  $f_{MAX}$ , vary the clock PRR.

**Note B:** A clear pulse is applied prior to each test.

**Note C:** Propagation delay times ( $t_{PLH}$  and  $t_{PHL}$ ) are measured at  $t_{n+1}$ . Proper shifting of data is verified at  $t_{n+8}$  with a functional test.

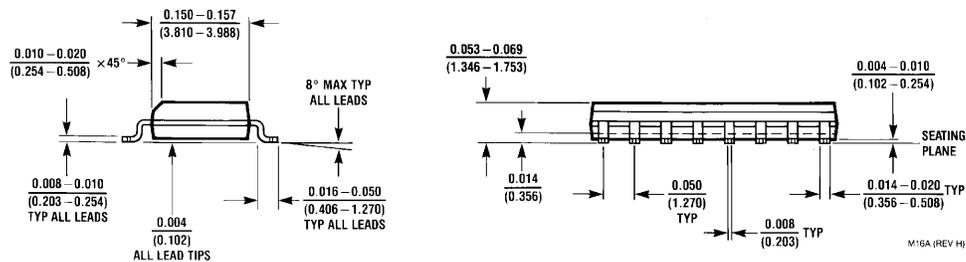
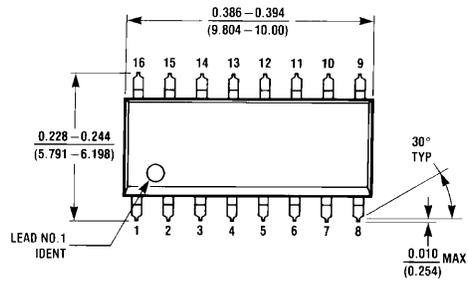
**Note D:**  $t_n$  = bit time before clocking transition

$t_{n+1}$  = bit time after one clocking transition

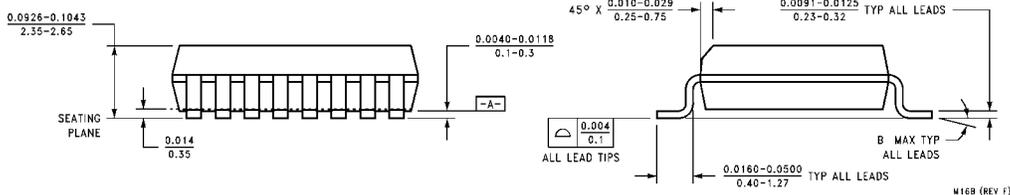
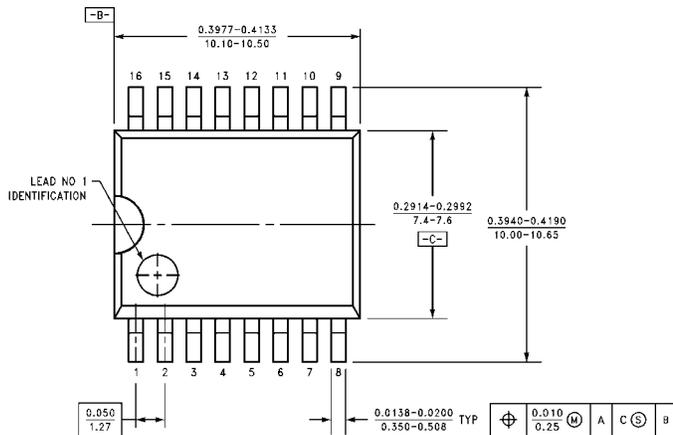
$t_{n+8}$  = bit time after eight clocking transitions

**Note E:**  $V_{REF} = 1.3V$ .

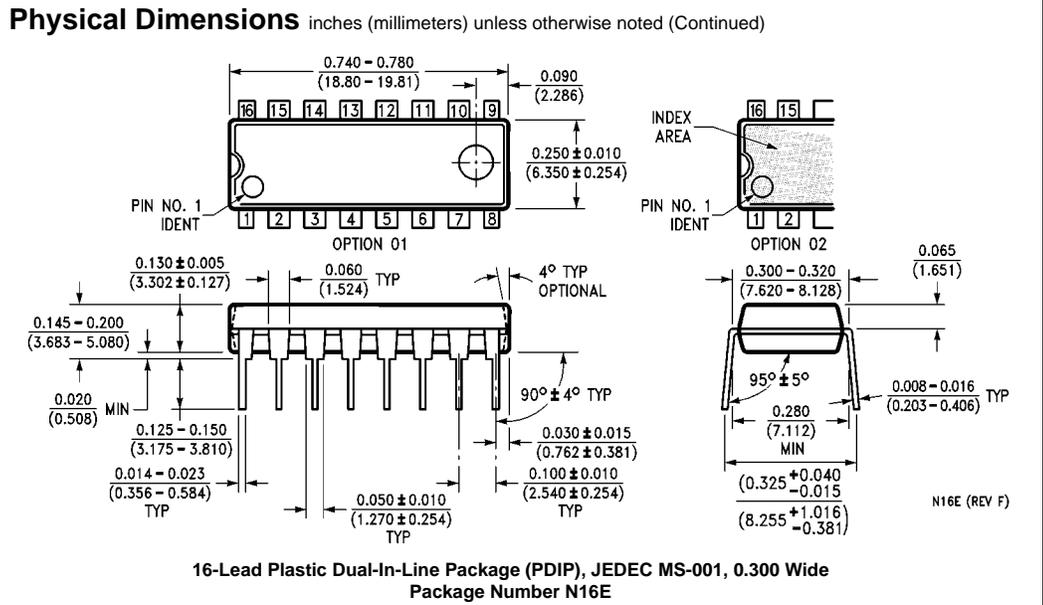
**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**



**16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M16B**



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)