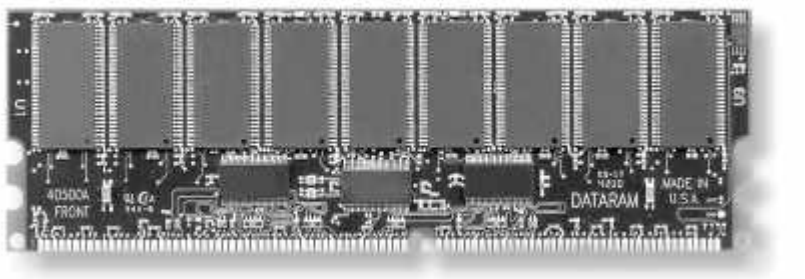
# DTM63627

## 1GMB - 128Mx72, 184-Pin Registered DDR SDRAM DIMM




**Identification**
DTM63627: 128Mx72

**Performance Range**
PC 2100 266MHz/CL=2.5
PC 1600 200MHz/CL=2

### Features

- Utilizes 133MHz DDR SDRAM
- Auto & self refresh capability (8192 cycles/64 ms)
- SSTL_2 compatible inputs and outputs
- VDD/VDDQ= 2.5V +/- 0.2V
- MRS cycle, with address key, programs Latency (Access from Column address) Burst length (2,4, and 8 page)
- Data scramble(Sequential & Interleave)
- Serial Presence Detect
- 184-pin JEDEC DIMM, double sided assembly, 5.25” wide by 1.70” high
- Commands entered on each positive CK edge
- DQS edge-aligned with Data for Reads; center-aligned with Data for Writes
- Two Data accesses per clock cycle
- DTM63627 is two Physical Banks
- SDRAM Addressing (13/11/2)(ROW/COL/BANK)

### Description

The Dataram DTM63627 assembly is a Registered 128Mx72 DDR Synchronous Dynamic RAM high-density memory module. The DTM63627 consists of eighteen CMOS externally stacked 128M x 4 bit DDR Synchronous DRAMs in two 66-pin TSOP-II 400mil packages. Two 13-bit to 26-bit registers for address and control, one PLL, and one 2K EEPROM for serial presence detect is used on all assemblies. These DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. Synchronous design allows for precise cycle control with the use of a differential system clock.

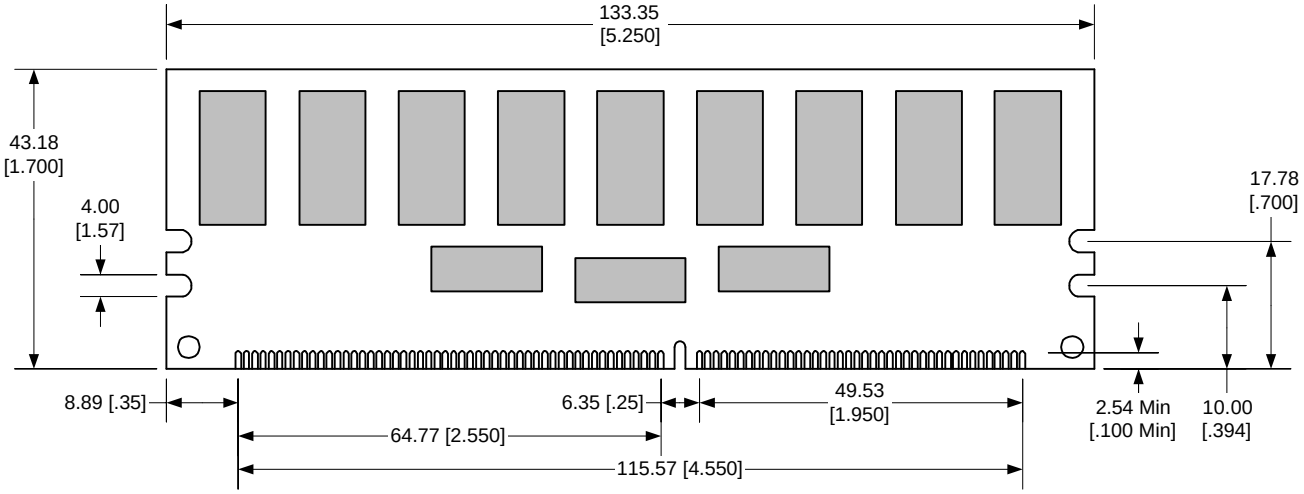
### Pin Configurations

| Front side | | | | | | | | Back side | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF | 24 | DQ17 | 47 | DQS8 | 70 | VDD | 93 | VSS | 116 | VSS | 139 | VSS | 162 | DQ47 |
| 2 | DQ0 | 25 | DQS2 | 48 | A0 | 71 | NC | 94 | DQ4 | 117 | DQ21 | 140 | DQS17 | 163 | NC |
| 3 | VSS | 26 | VSS | 49 | CB2 | 72 | DQ48 | 95 | DQ5 | 118 | A11 | 141 | A10 | 164 | VDDQ |
| 4 | DQ1 | 27 | A9 | 50 | VSS | 73 | DQ49 | 96 | VDDQ | 119 | DQS11 | 142 | CB6 | 165 | DQ52 |
| 5 | DQS0 | 28 | DQ18 | 51 | CB3 | 74 | VSS | 97 | DQS9 | 120 | VDD | 143 | VDDQ | 166 | DQ53 |
| 6 | DQ2 | 29 | A7 | 52 | BA1 | 75 | NC | 98 | DQ6 | 121 | DQ22 | 144 | CB7 | 167 | NC |
| 7 | VDD | 30 | VDDQ | 53 | DQ32 | 76 | NC | 99 | DQ7 | 122 | A8 | 145 | VSS | 168 | VDD |
| 8 | DQ3 | 31 | DQ19 | 54 | VDDQ | 77 | VDDQ | 100 | VSS | 123 | DQ23 | 146 | DQ36 | 169 | DQS15 |
| 9 | NC | 32 | A5 | 55 | DQ33 | 78 | DQS6 | 101 | NC | 124 | VSS | 147 | DQ37 | 170 | DQ54 |
| 10 | /RESET | 33 | DQ24 | 56 | DQS4 | 79 | DQ50 | 102 | NC | 125 | A6 | 148 | VDD | 171 | DQ55 |
| 11 | VSS | 34 | VSS | 57 | DQ34 | 80 | DQ51 | 103 | NC | 126 | DQ28 | 149 | DQS13 | 172 | VDDQ |
| 12 | DQ8 | 35 | DQ25 | 58 | VSS | 81 | VSS | 104 | VDDQ | 127 | DQ29 | 150 | DQ38 | 173 | NC |
| 13 | DQ9 | 36 | DQS3 | 59 | BA0 | 82 | NC | 105 | DQ12 | 128 | VDDQ | 151 | DQ39 | 174 | DQ60 |
| 14 | DQS1 | 37 | A4 | 60 | DQ35 | 83 | DQ56 | 106 | DQ13 | 129 | DQS12 | 152 | VSS | 175 | DQ61 |
| 15 | VDDQ | 38 | VDD | 61 | DQ40 | 84 | DQ57 | 107 | DQS10 | 130 | A3 | 153 | DQ44 | 176 | VSS |
| 16 | NC | 39 | DQ26 | 62 | VDDQ | 85 | VDD | 108 | VDD | 131 | DQ30 | 154 | /RAS | 177 | DQS16 |
| 17 | NC | 40 | DQ27 | 63 | /WE | 86 | DQS7 | 109 | DQ14 | 132 | VSS | 155 | DQ45 | 178 | DQ62 |
| 18 | VSS | 41 | A2 | 64 | DQ41 | 87 | DQ58 | 110 | DQ15 | 133 | DQ31 | 156 | VDDQ | 179 | DQ63 |
| 19 | DQ10 | 42 | VSS | 65 | CAS | 88 | DQ59 | 111 | CKE | 134 | CB4 | 157 | /S0 | 180 | VDDQ |
| 20 | DQ11 | 43 | A1 | 66 | VSS | 89 | VSS | 112 | VDDQ | 135 | CB5 | 158 | /S1 | 181 | SA0 |
| 21 | CKE0 | 44 | CB0 | 67 | DQS5 | 90 | WP* | 113 | NC | 136 | VDDQ | 159 | DQS14 | 182 | SA1 |
| 22 | VDDQ | 45 | CB1 | 68 | DQ42 | 91 | SDA | 114 | DQ20 | 137 | CK0 | 160 | VSS | 183 | SA2 |
| 23 | DQ16 | 46 | VDD | 69 | DQ43 | 92 | SCL | 115 | A12 | 138 | /CK0 | 161 | DQ46 | 184 | VDDSPD |

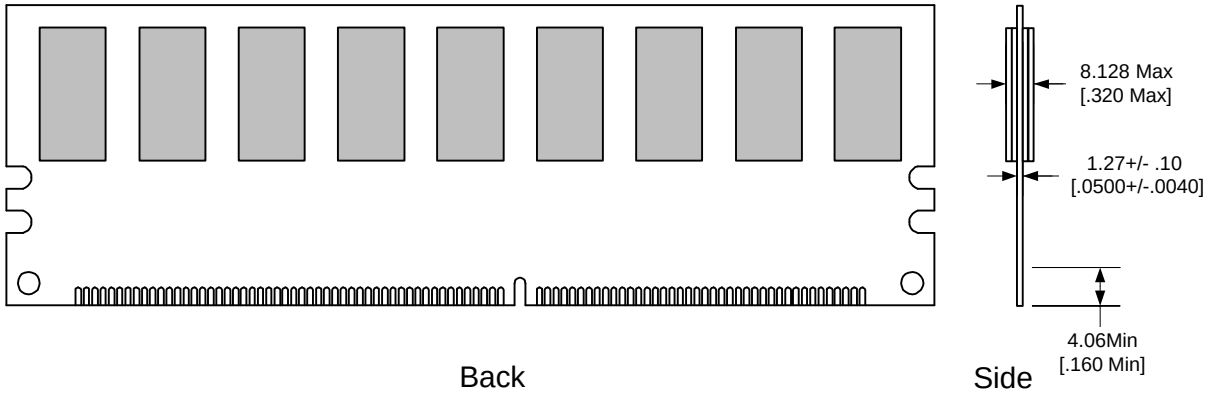
**NC = No connect** *** = Not Used**

### Pin Names

| Pin Names | Function |
|---|---|
| /RAS | Row address strobe |
| /CAS | Column address strobe |
| /WE | Write enable |
| /S[1:0] | Chip select |
| CK0,/CK0 | Differential Clock inputs |
| CKE[1:0] | Clock enable input |
| BA[1:0] | Bank select input |
| A[12:0] | Address input(Multiplexed) |
| VREF | SSTL_2 reference input |
| VDDID | VDD identification flag |
| SCL | Serial clock |
| SDA | Serial Data I/O |
| SA[2:0] | Address EEPROM |
| CB[7:0] | Data I/Os: Check bits |
| DQS[17:0] | Data strobes |
| DQ[63:0] | Data I/Os: Data bus |
| VDDQ | DQ power supply: 2.5V +/- .2V |
| VDD | Power supply: 2.5V +/- .2V |
| VSS | Ground |
| VDDSPD | Serial EEPROM power supply |
| /RESET | Reset Enable |
| NC | No connects |




Front

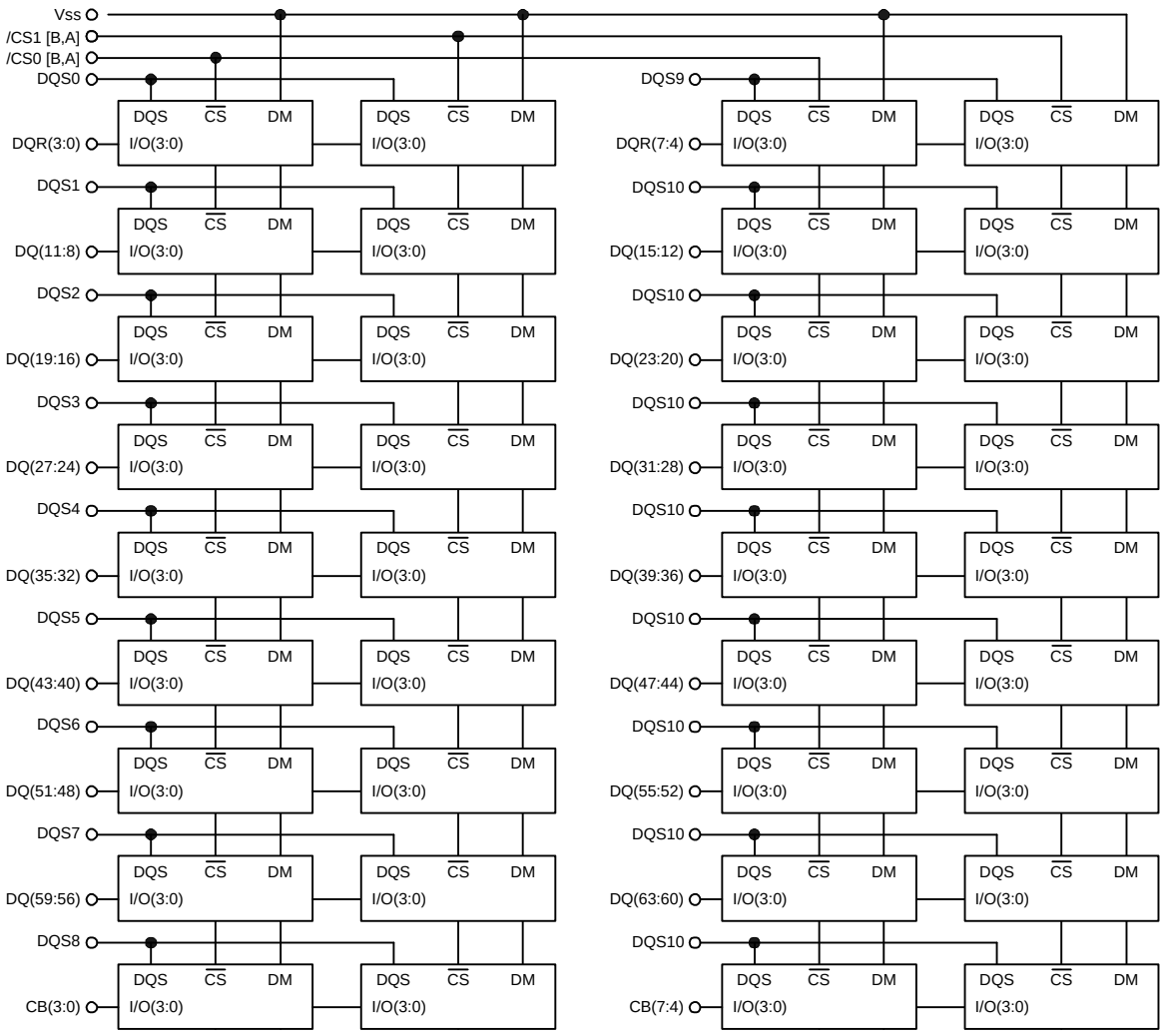


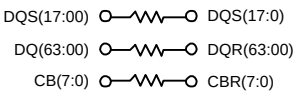

Back

Side

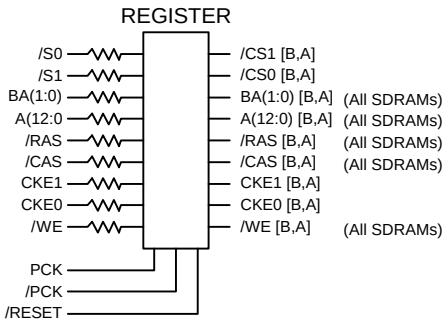
**Notes**

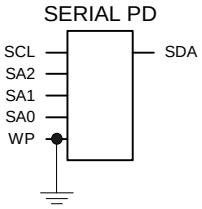
Tolerances on all dimensions except where otherwise indicated are ±.005 (.13).
The device used is 128Mx4 STACKED SDRAM, TSOP
All dimensions are expressed: inches [millimeters]

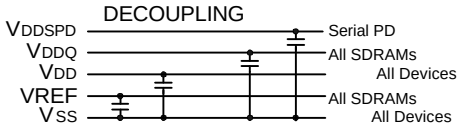



CK0, /CK0 -------- PLL*




NOTES

1. DQ/DQS/CB resistors are 22 ohms.
2. VDD=VDDQ
3. Address and control resistors are 22 ohms.
4. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER | SYMBOL | Rating | Unit |
|---|---|---|---|
| **Ambient Temperature** | TA | 0 ~ 70 | °C |
| **Storage Temperature** | TSTG | -55 ~ 125 | °C |
| **Voltage on Any Pin relative to VSS** | VIN,VOUT | -0.5 ~ 3.6 | V |
| **Voltage on VDDQ relative to VSS** | VDD | -0.5 ~ 0.6 | V |
| **Voltage on VDDQ relative to VSS** | VDDQ | -0.5 ~ 3.6 | V |
| **Output Short Circuit Current** | IOS | 50 | mA |
| **Power Dissipation** | PD | 36 | W |
| **Soldering Temperature Time** | TSOLDER | 260 10 | °C |

Note: Operation at above absolute maximum rating can adversely affect device reliability.

**DC OPERATING CONDITIONS** ($T_A$ = 0 to 70ºC, Voltage referenced to $V_{ss}$=0V)

| PARAMETER | Symbol | Minimum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| **Power Supply Voltage** | $V_{DD}$ | 2.3 | 2.5 | 2.7 | V | |
| **Power Supply Voltage** | $V_{DDQ}$ | 2.3 | 2.5 | 2.7 | V | 1 |
| **Input High Voltage** | $V_{IH}$ | $V_{REF}$ + 0.15 | - | $V_{DDQ}$ +0.3 | V | |
| **Input Low Voltage** | $V_{IL}$ | -0.3 | - | $V_{REF}$ – 0.15 | V | 2 |
| **Termination Voltage** | $V_{TT}$ | $V_{REF}$ + 0.04 | $V_{REF}$ | $V_{REF}$+0.04 | V | |
| **Reference Voltage** | $V_{REF}$ | 1.15 | 1.25 | 1.35 | V | 3 |

Notes:
(1) $V_{DDG}$ must not exceed the level of $V_{DD}$
(2) $V_{IL}$ (min) is acceptable- 1.5V AC pulse width with < 5ns of duration
(3) The value of $V_{REF}$ is approximately equal to 0.5$V_{DDQ}$.

**CAPACITANCE** ($T_A$ = 25°C, f=100MHz))

| PARAMETER | Pin | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| **Input capacitance** | A0-A12,BA0,BA1 | CIN1 | 2.5 | 3.5 | pF |
| **Input capacitance** | RAS, CAS, WE | CIN2 | 2.5 | 3.5 | pF |
| **Input capacitance** | CKE0, /CKE1 | CIN3 | 2.5 | 3.5 | pF |
| **Input capacitance** | CSO, CS1 | CIN4 | 2.5 | 3.5 | pF |
| **Data input/output Capacitance** | DQ0-DQ63, DQS0-DQS17 | CI01 | 8 | 10 | pF |
| **Data input/output Capacitance** | CB0~CB7 | C102 | 8 | 10 | pF |

NOTE:
1. VDD=min. to max., VDDQ=2.3V to 2.7V, VODC=VDDQ/2, Vopeak-to-peak=0.2V
2. Pins not under test are tied tto GND.
3. These values are guaranteed by design and are tested on a sample basis only

**DC CHARACTARISTICS I** ($T_A$ = 0 to 70°C, Voltage referenced to $V_{ss}$ = 0V)

| PARAMETER | Symbol | Minimum | Maximum | Unit | Note |
|---|---|---|---|---|---|
| **Input Leakage Current** | $I_{LI}$ | -5 | 5 | UA | 1, 3 |
| **Output Leakage Current** | $I_{Lo}$ | -5 | 5 | UA | 2, 3 |
| **Output High Voltage** | $V_{OH}$ | $V_{TT}$ + 0.76 | - | V | IOH=+15.2mA |
| **Output Low Voltage** | $V_{OL}$ | - | $V_{TT}$ + 0.76 | V | IOL=+15.2mA |

**Note:** 1. $V_{IH=0}$ to 3.6V, All other pins are not tested under $V_{IH=}$OV
2. $D_{OUT}$ is disabled, $V_{OUT=}$0 to 2.7V
3. These values are device characteristics

**DC CHARACTARISTICS II** ($T_A$ = 0 to 70°C, Voltage referenced to $V_{ss}$ = 0V)

| PARAMETER | Symbol | Test Condition | | Max | Unit | Note |
|---|---|---|---|---|---|---|
| **Operating Current** | IDD1 | Burst length=2, One bank active<br>tRC ≥ tRC(min), $I_{OL=}$0mA | | 2610 | mA | 1 |
| **Precharge Standby current in Power Down Mode** | IDD2P | CKE ≤ $V_{IL}$(max),tCK=min | | 540 | mA | |
| **Precharge Standby current in Non Power Down Mode** | IDD2N | CKE ≥ $V_{IH}$(min),CS≥ $V_{IH}$(min),Tck=min<br>Input signals are changed one time during 2 clks | | 1260 | mA | |
| **Active Standby Current In Power Down Mode** | IDD3P | CKE ≤ $V_{IL}$(max),tCK=min | | 540 | mA | |
| **Active Standby Current In Non Power Down Mode** | IDD3N | CKE ≥ $V_{IH}$(min),CS≥ $V_{IH}$(min),tCK=min<br>Input signals are changed one time during 2 clks | | 2160 | mA | |
| **Burst Mode Operating Current** | IDD4 | tCK ≥ tCK=(min), $I_{OL=}$0mA<br>All banks active | CL=2.5 | 3600 | mA | |
| | | | CL=2 | 2340 | | |
| **Auto Refresh Current** | IDD5 | tRC ≥ tRCF(min), All banks active | | 6120 | mA | 1,2 |
| **Self Refresh Current** | IDD6 | CKE ≤ 0.2V | | 72 | mA | |

**Note:** 1. IDD1, IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRFC (Auto Refresh row Cycle time) is shown at AC CHARACTERICS.

**AC OPERATING CONDITIONS** ($T_A$ = 0 to 70ºC, Voltage referenced to $V_{ss}$=0V)

| PARAMETER | Symbol | Minimum | Maximum | Unit | Note |
|---|---|---|---|---|---|
| **Input High (Logic 1) Voltage, DQ,DQS and DM signals** | $V_{IH(AC)}$ | VREF=0.31 | | V | |
| **Input High (Logic 0) Voltage, DQ,DQS and DM signals** | $V_{IL(AC)}$ | | VREF=0.31 | V | |
| **Input Differential Voltage, CK AND/CK inputs** | $V_{ID(AC)}$ | 0.7 | VDDQ+0.6 | V | 1 |
| **Input Crossing Point Voltage, CK AND/CK inputs** | $V_{IX(AC)}$ | 0.5*VDDQ-0.2 | 0.5*VDDQ+0.2 | V | 2 |

Note:
(1) VID is the magnitude of the difference between the input level on CK and the input on CK.
(2) The value of VIX s expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

**AC OPERATING TEST CONDITIONS** ($T_A$ = 0 to 70ºC, Voltage referenced to $V_{ss}$=0V)

| PARAMETER | Value | Unit |
|---|---|---|
| **Reference Voltage** | $V_{DDQ}$ X 0.5 | V |
| **Termination Voltage** | $V_{DDQ}$ X 0.5 | V |
| **AC Input High Level Voltage ($V_{IH}$´min)** | $V_{REF}$ + 0.31 | V |
| **AC Input Low Level Voltage ($V_{IL}$´max)** | $V_{REF}$ | V |
| **Input Timing Measurement Reference Level Voltage** | $V_{TT}$ | V |
| **Input Signal maximum peak swing** | 1.5 | V |
| **Input minimum Signal Slew Rate** | 1 | V/ns |
| **Termination Resistor ($R_T$)** | 50 | ? |
| **Series Resistor** | 22 | ? |
| **Output Load Capacitance for Access Time Measurement (CL)** | 30 | pF |

**AC OPERATING CONDITIONS** (AC operating conditions unless otherwise noted)

| PARAMETER | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Row Cycle Time | | tRC | 65 | - | ns | |
| Auto Refresh Row Cycle Time | | tRFC | 75 | - | ns | |
| Row Active Time | | tRAS | 45 | 120K | ns | |
| Row Address to Column Address Delay | | tRCD | 20 | - | ns | |
| Row Active to row Active Delay | | tRRD | 15 | - | ns | |
| Column Address to Column Address Delay | | tCCD | 1 | - | CLK | |
| Row Precharge time | | tRP | 20 | - | ns | |
| Write Recovery Time | | tWR | 15 | - | ns | |
| Last Data-In to Read Command | | tDRL | 1 | - | CLK | |
| Auto Precharge Write Recovery + Precharge Time | | tDAL | 35 | - | ns | |
| System Clock Cycle Time | CAS Latency = 2.5 | tCK | 7.5 | 15 | ns | |
| | CAS Latency = 2 | | 10 | 15 | ns | |
| Clock High Level Width | | tCH | 0.45 | 0.55 | CLK | |
| Clock Low Level Width | | tCL | 0.45 | 0.55 | CLK | |
| Data-Out edge to Clock edge Skew | | tAC | -0.75 | 0.75 | ns | |
| DQS-Out edge to Clock edge skew | | tDQSCK | -0.75 | 0.5 | ns | |
| DQS-Out edge to Data-out edge skew | | tDQSQ | - | - | ns | |
| Data-Out hold time from DQS | | tQH | tHpmin -0.75ns | - | ns | 1 |
| Clock Half Period | | tHP | tCH/L min | - | ns | 1 |
| Input Setup Time (fast slew rate) | | tIS | 0.9 | - | ns | 2,3,5,6 |
| Input Hold Time (fast slew rate) | | tIH | 0.9 | - | ns | 2,3,5,6 |
| Input Setup Time (slow slew rate) | | tIS | 1.0 | - | ns | 2,4,5,6 |
| Input Hold Time (slow slew rate) | | tIH | 1.0 | - | ns | 2,4,5,6 |
| Input Pulse Width | | tIPW | 2.2 | - | ns | 6 |
| Write DQS High Level Width | | tDQSH | 0.4 | 0.6 | CLK | |
| Write DQS Low Level Width | | tDQSL | 0.4 | 0.6 | CLK | |
| CLK to First Rising edge to DQS-In | | tDQSS | 0.75 | 1.25 | CLK | |
| Data-In Setup Time to DQS-In (DQ & DM) | | tDS | 0.5 | - | ns | 7 |
| Data-In Hold Time to DQS-In (DQ & DM) | | tDH | 0.5 | - | ns | 7 |

**AC OPERATING CONDITIONS**

(AC operating conditions unless otherwise noted)

| PARAMETER | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| **DQ Input Pulse Width** | $^{t}$DIPW | 1.75 | - | Ns | |
| **Read DQS Preamble Time** | $^{t}$RPRE | 0.9 | 1.1 | CLK | |
| **Read DQS Postamble Time** | $^{t}$RPST | 0.4 | 0.6 | CLK | |
| **Write DQS Preamble Setup Time** | $^{t}$WPRES | 0- | - | CLK | |
| **Write DQS Preamble Hold Time** | $^{t}$WPREH | 0.25 | - | CLK | |
| **Write DQS Postamble Time** | $^{t}$WPST | 0.4 | 0.6 | CLK | |
| **Mode Register Set Delay** | $^{t}$MRD | 2 | - | CLK | |
| **Power Down Exit time** | $^{t}$PDEX | 10 | - | ns | |
| **Exit Self Refresh to Non-Read Command** | $^{t}$XSNR | 75 | - | ns | |
| **Exit Self Refresh to Read Command** | $^{t}$XSRD | 200 | - | CLK | 8 |
| **Average Periodic Refresh Interval** | $^{t}$REFI | - | 15.6 | us | |

**Note:**

1. This calculation accounts for $^{t}$DQSQ(max), the pulse width distortion of on-chip and jitter.
2. Data sampled at the rising edges of the clock: AO~A11, BA0~BA1, CKE, SO, ISI, RAS, CAS, WE
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
5. CK,/CK slew rates are >=1.0V/ns
6. These PRAMETERs guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(DQS)
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self refresh Exit and lock the internal DLL circuit of DDR SDRAM.

**Simplified Command Truth Table**

| Command | | CKEn-1 | CKEn | S0,S1 | RAS | CAS | WE | ADDR | A10/AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Ambient Temperature | | H | X | L | L | L | L | OP code | | | 1,2 |
| Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Device Deselect | | H | X | H | X | X | X | x | | | 1 |
| No Operation | | | | L | H | H | H | | | | |
| Bank Active | | H | X | L | L | H | H | RA | | V | 1 |
| Read | | H | X | L | H | H | H | CA | L | V | 1 |
| Read with Autoprecharge | | | | | | | | | H | | 1,3 |
| Write | | H | X | L | H | H | L | CA | L | V | 1 |
| Write with Autoprecharge | | | | | | | | | H | | 1,4 |
| Precharge All Banks | | H | X | L | L | H | L | X | H | V | 1,5 |
| Precharge Selected Bank | | | | | | | | | L | | 1 |
| Read Burst Stop | | H | X | L | H | H | L | X | | | 1 |
| Auto Refresh | | H | H | L | L | L | H | X | | | 1 |
| Self Refresh | Entry | H | L | L | L | L | L | X | | | 1 |
| | | L | H | H | X | X | X | | | | 1 |
| | Exit | | | L | H | H | H | | | | |
| Precharge Power Down Mode | Entry | L | H | H | X | X | X | X | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| Active Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | V | V | V | | | | 1 |
| | Exit | H | H | X | | | | | | | 1 |

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP code=Operand Code, NOP=No Operation)

1. DM states are "Don't Care". Refer to below Write Mask Truth Table.
2. OP Code (Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Registering during Extended MRS or MRS. Before entering Mode Register Set Mode, all banks must be in a percharge state and MRS command can be issued after $^{t}$RP period from Precharge command.
3. If a read with Autoprecharge command is detected my memory component in CLK(n), then there will be no command presented to activated bank until CLK(N+bl/2+ $^{t}$RP).
4. If a Write with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+ $^{t}$DPL+ $^{t}$RP). Last Data-In to Precharge delay ($^{t}$DPL) which is also called Write Recovery Time ($^{t}$WR) is needed to guarantee that the last data has been completely written.
5. If 10/AP id "High" when row Precharge command being issued, BA 0/AB1 are ignored and all banks are selected to be precharged.

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