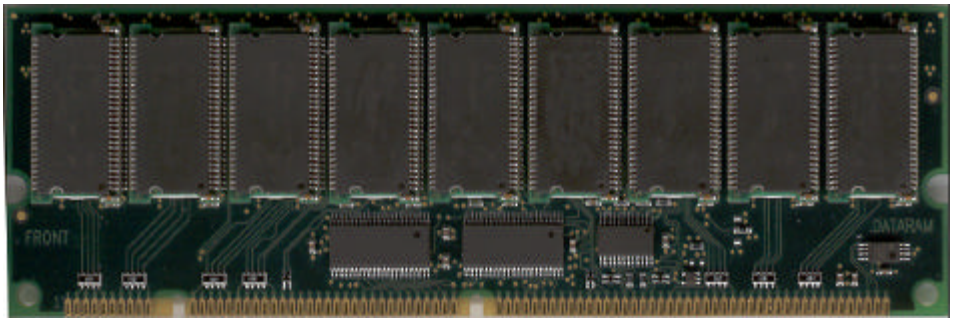
DTM60192

1024MB-128Mx72, 168-Pin Registered PC133/PC100 SDRAM DIMM



Identification

DTM60192: 128Mx72

Performance range

133MHz (7.5ns @ CL=3)
100MHz (10ns @ CL=2)

Features

- Burst mode operation
- Auto and self refresh capability (8192 Cycle/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs Latency (Access from column address), Burst length (1, 2, 4 and 8), Data scramble (Sequential and Interleave)
- Serial presence detect with EEPROM
- 168-pin PC133 DIMM double-sided assembly 5.250” wide by 1.70” high

Description

The Dataram DTM60192 is a registered 128Mx72 and Synchronous Dynamic RAM high-density memory module. The assembly consists of eighteen stacked 128Mx4 bit SDRAMs in two TSOP-11 400 mil packages. Three 18-bit Drive ICs for input control, one PLL for clock, and one 2K EEPROM for Serial Presence Detect are also installed on a 168-pin glass-epoxy substrate. Synchronous design allows precise cycle control with the use of a system clock. The DTM60192 is a Dual in-line Memory Module intended for mounting into a 168-pin connector socket.

Pin Configurations

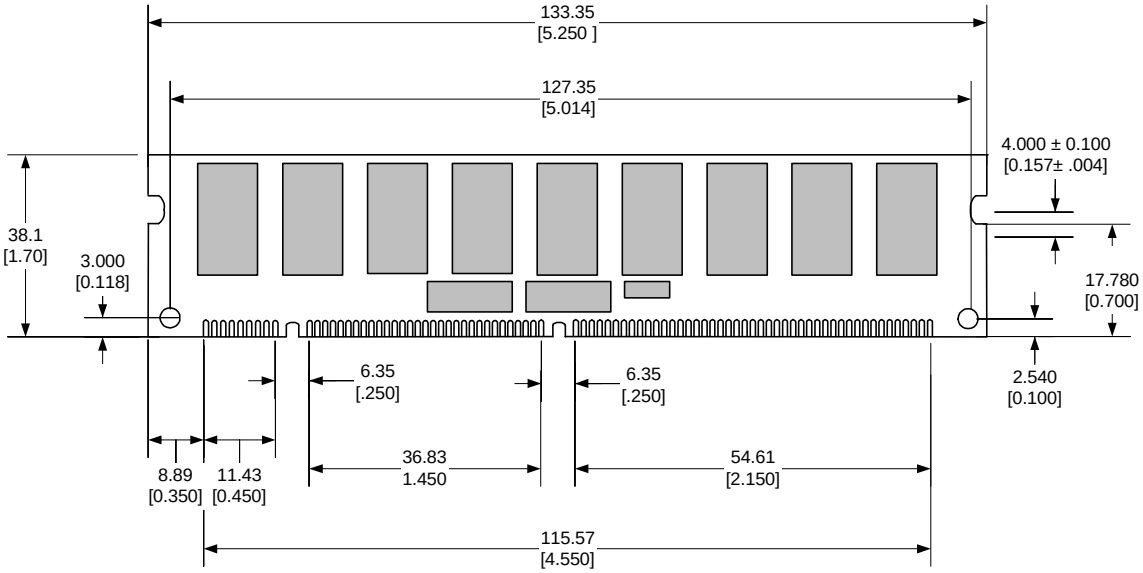
Front side						Back side					
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	NC	59	Vdd	87	DQ33	115	$\overline{RAS}$	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	NC	90	Vdd	118	A3	146	NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vdd	101	DQ45	129	$\overline{S3}$	157	Vdd
18	Vdd	46	DQMB2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	NC	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQMB0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

Pin Names

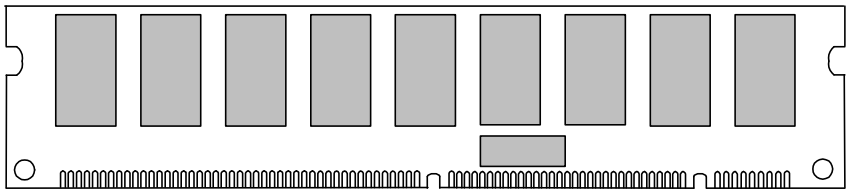
Pin name	Function
A0-A12	Address input (Multiplexed)
BA0-BA1	Select bank
DQ0-DQ63	Data input/output
CB0-CB7	Check bit (Data-in/data-out)
CK0-3	Clock input
CKE0-1	Clock enable input
$\overline{S0}$-$\overline{S3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQMB0-7	Data mask
Vdd	Power supply (3.3V)
Vss	Ground
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0-2	Address in EEPROM
NC	No connection
WP	Write protection

*These pins are not used in this module.
**These pins should be NC in the system, which does not support SPD.

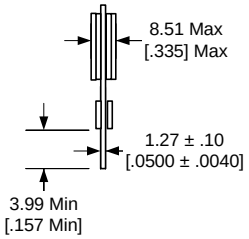
Front View



Back View



Side View

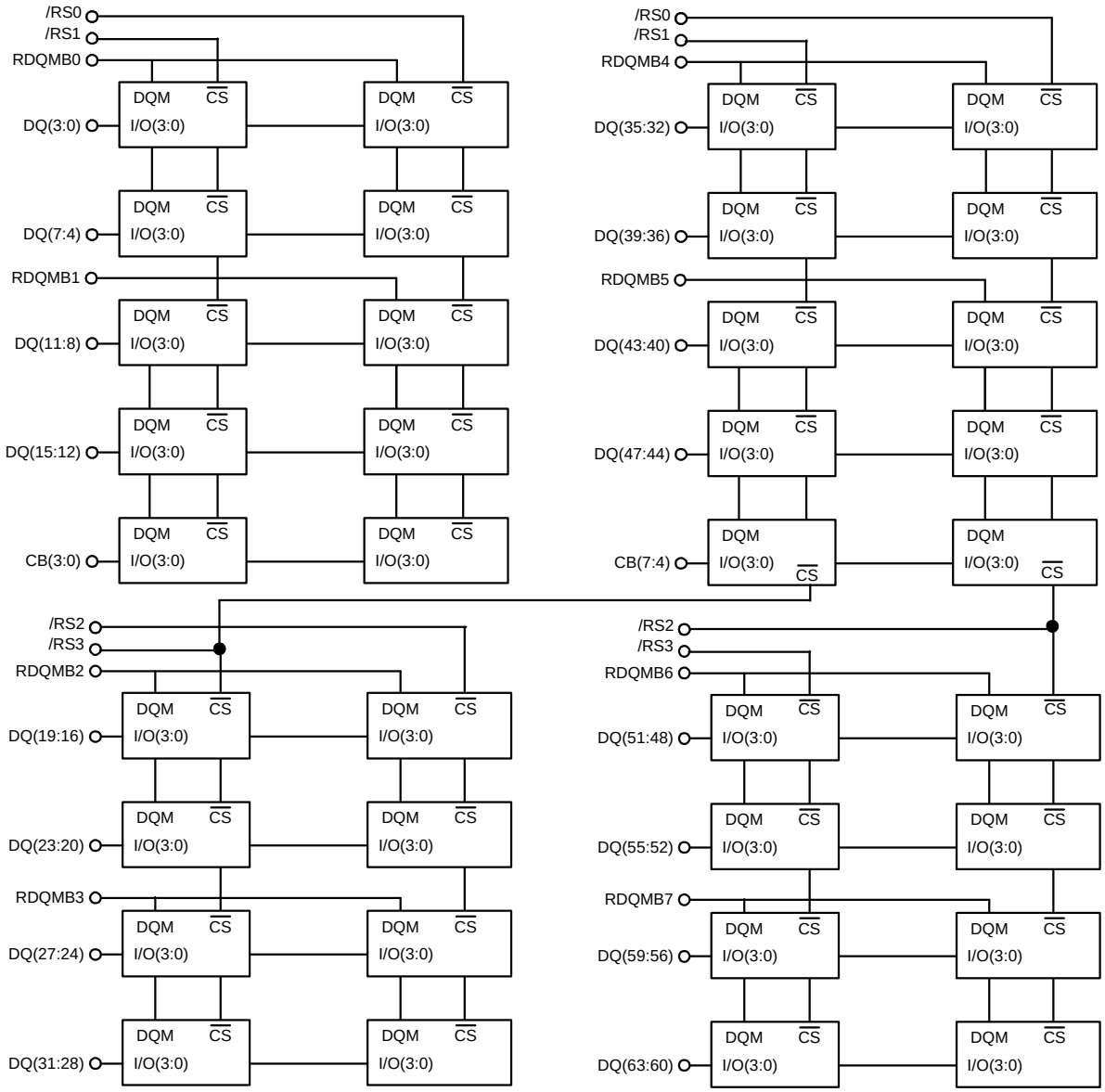


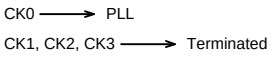
Notes

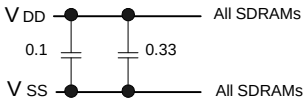
Tolerances on all dimensions except where otherwise indicated are ±. .13 [.005].

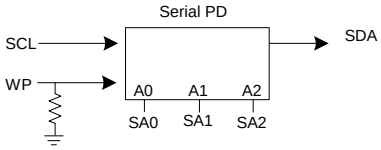
The device used is 128Mx4 SDRAM, TSOP.

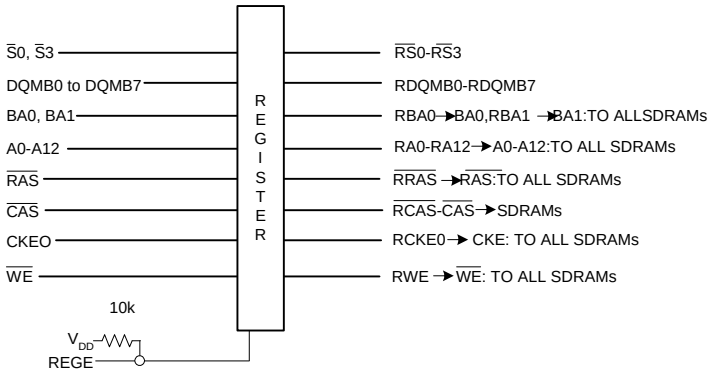
All dimensions are expressed: millimeters [inches].


/RS0
/RS1
RDQMB0
DQ(3:0)
DQ(7:4)
RDQMB1
DQ(11:8)
DQ(15:12)
CB(3:0)
/RS2
/RS3
RDQMB2
DQ(19:16)
DQ(23:20)
RDQMB3
DQ(27:24)
DQ(31:28)
/RS0
/RS1
RDQMB4
DQ(35:32)
DQ(39:36)
RDQMB5
DQ(43:40)
DQ(47:44)
CB(7:4)
/RS2
/RS3
RDQMB6
DQ(51:48)
DQ(55:52)
RDQMB7
DQ(59:56)
DQ(63:60)
DQM
CS
I/O(3:0)


CK0 → PLL
CK1, CK2, CK3 → Terminated


V DD
All SDRAMs
0.1
0.33
V SS
All SDRAMs


Serial PD
SCL
SDA
WP
A0
A1
A2
SA0
SA1
SA2


S0, S3
DQMB0 to DQMB7
BA0, BA1
A0-A12
RAS
CAS
CKEO
WE
10k
VDD
REGE
REGISTER
RS0-RS3
RDQMB0-RDQMB7
RBA0→BA0,RBA1 →BA1:TO ALLSDRAMs
RA0-RA12→A0-A12:TO ALL SDRAMs
RRAS →RAS:TO ALL SDRAMs
RCAS-CAS→SDRAMs
RCKE0→ CKE: TO ALL SDRAMs
RWE →WE: TO ALL SDRAMs

Absolute maximum ratings

	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 to +4.6	V
Storage temperature	T_{stg}	-55 to +150	°C
Power dissipation	P_D	27	W
Short-circuit output current	I_{OS}	50	mA

NOTE:

Permanent damage to the device may occur if absolute maximum ratings are exceeded. Operation should be restricted to the conditions detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect relaibility.

DC operating conditions and characteristics (Voltage referenced to V_{SS} = 0V; T_A = 0 to 70°C)

	Symbol	Minimum	Typical	Maximum	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OH}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-4	-	4	uA	3
Input leakage current (I/O Pins)	I_{IL}	-3	-	3	uA	3,4

NOTES:

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input OV ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. D_{OUT} is disabled, OV ≤ V_{OUT} ≤ V_{DDQ}

Capacitance (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V ± 200mV))

	Symbol	Maximum	Unit
Input capacitance (A0-A12)	C_{IN1}	19	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	19	pF
Input capacitance (CKE0)	C_{IN3}	19	pF
Input capacitance (CLK0)	C_{IN4}	18	pF
Input capacitance ($\overline{CS0}$-$\overline{CS3}$)	C_{IN5}	15	pF
Input capacitance (DQM0-DQM7)	C_{IN6}	14	pF
Input capacitance (BA0-BA1)	C_{IN7}	19	pF
Input/Output capacitance (DQ0-DQ63)	C_{OUT}	13	pF
Input/Output capacitance (CB0-CB7)	C_{OUT1}	13	pF

DC characteristics (Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

	Symbol	Test Condition	Maximum	Unit	Notes
Operating current (Active mode)	I_{DD1}	Burst length = 2 $t_{RC} \geq t_{RC}$ (min) I_{OL} = 0 mA	3960	mA	1
Precharge standby current in power-down mode	$I_{DD2}P$	CKE ≤ V_{IL} (max), t_{cc} = 15ns	356	mA	3
	$I_{DD2}PS$	CKE & CLK ≤ V_{IL} (max), t_{cc} = 15ns ∝	117	mA	3
Precharge standby current in non power-down mode	$I_{DD2}N$	CKE ≥ V_{IH} (min), CS ≥ V_{IH} (min), t_{cc} = 15 ns Input signals are changed one time during 30ns	760	mA	3
	$I_{DD2}NS$	CKE ≥ V_{IH} (min), CLK ≥ V_{IL} (max), t_{cc} = ∝ Input signals are stable	270	mA	3
Active standby current in power-down mode	$I_{DD3}P$	CKE ≤ V_{IL} (max), t_{cc} = 15ns	446	mA	3
Active standby current in non power-down mode	$I_{DD3}N$	CKE ≥ V_{IH} (min), CS ≥ V_{IH} (min), t_{cc} = 15 ns Input signals are changed one time during 30ns	1120	mA	3
Operating current (Burst mode)	I_{DD4}	I_{OL} = 0 mA Page Burst 2 Blanks activated t_{CCD} = 2 CLK	4140	mA	1
Refresh current	I_{DD5}	$t_{RC} = t_{RC}$ (min)	7200	mA	2
Self Refresh current	I_{DD6}	CKE ≤ 0.2V	276	mA	3

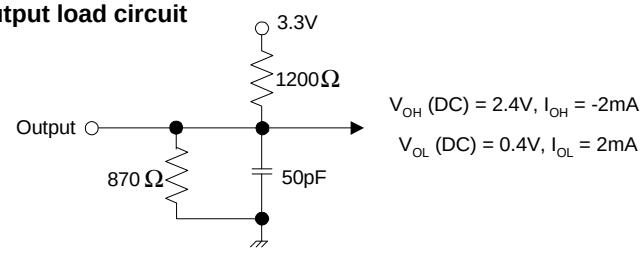
NOTES:

1. Measured with outputs open.
2. Drive IC's not active, PLL is active.
3. Measured with 1 PLL and 3 Drive ICs.

AC operating test conditions (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Figure 1	

DC output load circuit



AC output load circuit

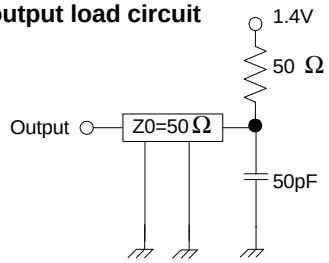


Figure 1

Operating AC parameter (AC operating conditions unless otherwise noted)

	Symbol	Time	Unit	Note
Row active to row active delay	t_{RRD} (min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD} (min)	20	ns	1
Row precharge time	t_{RP} (min)	20	ns	1
Row active time	t_{RAS} (min)	45	ns	1
	t_{RAS} (max)	100	us	
Row cycle time	t_{RC} (min)	67.5	ns	1
Last data into row precharge	t_{RDL} (min)	1	CLK	2
Col. address to col. address delay	t_{CCD} (min)	1	CLK	3

NOTES:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC characteristics (AC operating conditions unless otherwise noted)

	CAS	Symbol	Minimum	Maximum	Unit	Notes
CLK cycle time	CAS latency = 3	tCK	7.5		ns	1
	CAS latency = 2	tCK	10		ns	1
CLK to valid output delay	CAS latency = 3	tAC		5.4	ns	1, 2
	CAS latency = 2	tAC		6	ns	1, 2
Output data hold time		tOH	2.45		ns	1, 2
CLK high pulse width		tCKH	2.5		ns	3
CLK low pulse width		tCKL	2.5		ns	3
Input setup time		tDS	1.5		ns	3
Input hold time		tDH	0.8		ns	3
CLK to output in Low-Z		tLZ	1		ns	2
CLK to output in Hi-Z	CAS latency = 3	tHZ		5.4	ns	1
CLK to output in Hi-Z	CAS latency = 2	tHZ		6	ns	1

NOTES:

1. Parameters depend on programmed CAS latency. DIMM CAS latency = Device CL + 1 for Register Mode.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr and tf) = 1ns.
   If tr and tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1] ns should be added to the parameter.

DATARAM

DATARAM CORPORATION, P.O.Box 7528, Princeton, NJ 08543-7528; Voice: 609-799-0071, Fax: 609-799-6734; www.dataram.com

DATARAM International, Soenderhoej 22, 8260 Viby J / Aarhus, Denmark; Voice: +45 70 212 212, Fax: +45 70 212 211, Fax Sales: +45 70 212 216; www.dataram.dk