National Semiconductor

PRELIMINARY
April 1994

DP84600R/DP84605R
Thin-Film/MIG Head Read/Write Preamplifier

General Description

The DP84600R/DP84605R are 5V, high performance, four channel, low power, read preamplifiers/write current drivers designed for two-terminal recording head applications. An idle mode is available which conserves power to a level of 0.5 mW (typically) when activated. Power supply fault protection is included to disable the write current generator whenever the supply voltage is below 4V. Both parts incorporate 300Ω write damping.

The DP84600R has a read gain of 300 versus 200 for the DP84605R.

Upon request, other options such as other read gains, PECL inputs, no damping, and different packaging are available.

Features

- Low input capacitance: 12 pF typical
- Low input noise: 0.49 nV/$\sqrt{\text{Hz}}$ typical
- Low power: 100 mW typical in read mode
- Very low idle power: 0.5 mW typical
- Programmable write current source (1 mA–40 mA)
- Low power supply protection in write mode
- Head short to ground protection
- Plug compatible to VTC VM7204/7104/7114
- Single 5V power supply

Block Diagram

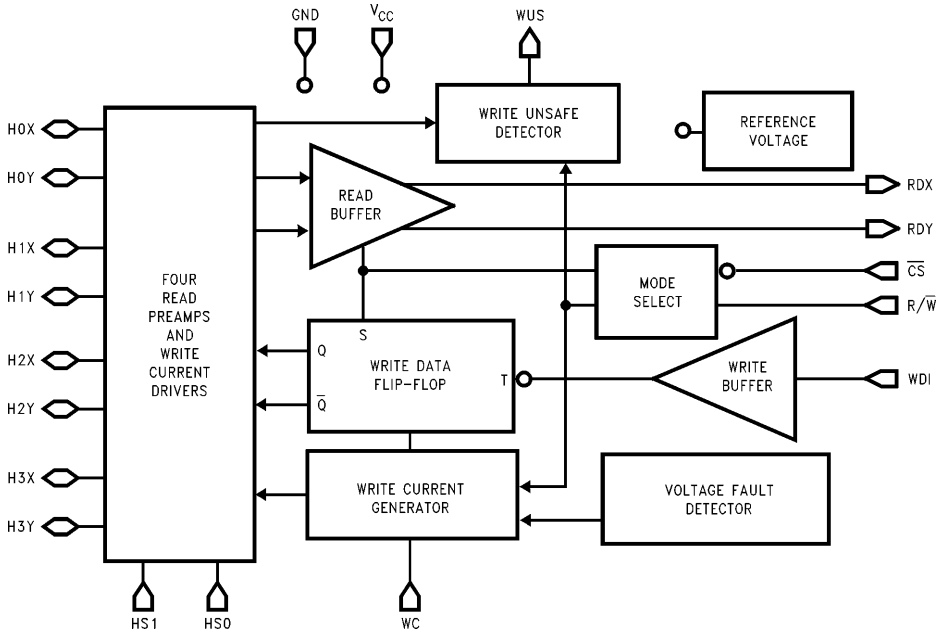

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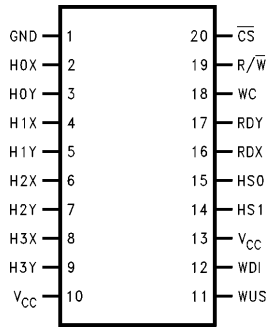
FIGURE 1. Circuit Block Diagram

This Preliminary document contains information on a product under development. Specifications contained within are based on design targets or a limited amount of data and are subject to change without notice. National Semiconductor reserves the right to change or discontinue this product without notice.

TABLE I. Pin Descriptions

Pin Name	Pin Type	Pin Function Description
V_{CC}	Power Supply	Power supply Pin (5V ±10%). These pins (10 and 13) are internally shorted.
WDI	Input (TTL)	Each negative transition on WDI toggles the head current between the X and Y head connections.
HS0, HS1	Input (TTL)	Logic levels are applied to these pins to select 1 of 4 heads (see Table II).
R/$\overline{W}$	Input (TTL)	A logic high level selects the read mode while a low logic level selects the write mode. The $\overline{CS}$ pin must be at a low logic level for this operation to be active (see Table III).
$\overline{CS}$	Input (TTL)	A high logic level disables the operation of the device and puts the read data outputs (RDX, RDY) into a high impedance state.
H0X, H0Y through H3X, H3Y	Outputs	X and Y connections to the read/write heads.
$\overline{WUS}$	Output	A logic high level at this pin indicates that one of several conditions has been detected by internal circuitry which makes writing unsafe.
RDX, RDY	Output	Differential read data outputs.
WC	Output	A resistor is connected from this pin to ground to control the magnitude of the write current (see formula in Write Mode description).
GND	Ground	Device ground.

Connection Diagram



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Order Number DP84600R or DP84605R
See NS Package Number M20B or MSA20

FIGURE 2. Connection Diagram

Basic Circuit Operation

The DP84600R/DP84605R can address up to four two-terminal thin-film heads, providing the write current drive in the write mode or read data amplification in the read mode.

Head selection is controlled by the logic states on two pins, HEAD SELECT 0 (HS0) and HEAD SELECT 1 (HS1). Table II defines the results of each combination of these two pins. These pins have internal pull-down current so that head 0 is selected if an open condition exists on these pins.

TABLE II. Head Selection

HS1	HS0	Head Selected
0	0	0
0	1	1
1	0	2
1	1	3

The selection of device mode (write, read or idle) is also controlled by two pins, CHIP SELECT ($\overline{CS}$) and READ/$\overline{WRITE}$ (R/$\overline{W}$). Table III defines the results of each combination of these two pins. These pins have internal pull-up resistors so that the idle condition is selected if an open condition exists on these pins.

TABLE III. Mode Selection

$\overline{CS}$	R/$\overline{W}$	Mode Selected
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

Write Mode

The write mode is entered by setting both $\overline{CS}$ and R/$\overline{W}$ to logical low values. In the write mode, the device acts as a current switch which toggles between the X and Y sides of the selected head on each high-to-low logic level transition of the WRITE DATA INPUT (WDI). When entering the write mode from the read mode, the write data flip-flop is initialized to pass current into the X side of the selected head. The magnitude of the write current is set by an external resistor, R_{WRITE} connected between the WC pin and ground. The relationship between the write current and the write resistor is:

$$I_{WRITE} = A_{WC} \times \frac{V_{WC}}{R_{WRITE}}$$

where A_{WC} is the current gain (see Write Mode DC Electrical Characteristics Table).

Write Mode (Continued)

The portion of the write current that passes through the head (I_h) is defined as:

$$I_h = \frac{I_{WRITE}}{1 + R_h/R_d}$$

where: R_h = the sum of the head and external wire resistance
and R_d = the damping resistance (if any).
$R_d = \infty$ for no damping.

When entering the write mode, the write unsafe detector circuitry is enabled. This circuit issues a high level output at the WRITE UNSAFE (WUS) output when any of the following conditions exist:

1) Write data input frequency is too low.
2) The device is in the read mode.
3) The chip is disabled.
4) No write current exists.
5) The head is an open circuit.

The WUS pin is an open-collector output and requires an external pull-up resistor. After the fault condition has been removed, two negative transitions of the WDI pin are required to clear the write unsafe circuitry.

A power supply fault detection circuit is provided on chip. This circuit will disable the write current generator during device power-up, power-down or when a power supply fault occurs. This will prevent the possibility of writing bad data onto the media.

Read Mode

The read mode is entered by setting $\overline{CS}$ to a low logic level and R/$\overline{W}$ to a high logic level. In this mode the write current generator is disabled and a low noise differential amplifier is enabled. The amplified head read-back signal is available at the RDX and RDY pins. These outputs are differential emitter-followers and should be AC coupled to the load.

During the write or idle modes, the read amplifier is disabled and the RDX, RDY outputs are forced to a high impedance state. This allows these outputs to be wire-ORed with outputs from other devices to support multiple read/write applications.

Idle Mode

The idle mode is entered by applying a logical high level to the $\overline{CS}$ pin. In this mode the RDX and RDY outputs are in a high impedance state and the device is disabled. This will reduce the power consumption to a mimmum value when the device is not needed, which is particulariy important for battery applications

Absolute Maximum Ratings

Operation beyond these limits may permanently damage the device.

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Digital Input Voltage	−0.3V to (V_{CC} + 0.3)V
Maximum Head Port Voltage	−0.3V to (V_{CC} + 0.3)V
Maximum Output Current (RDX, RDY)	−10 mA
Maximum Output Write Current	60 mA
ESD Susceptibility (Note 1)	2000V
Storage Temperature Range	−65°C to +150°C

Note 1: Human body model is used. (120 pF through 1.5 kΩ)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5	5.5	V
Operating Free Air Temperature Range (T_A)	0		70	°C

General DC Electrical Characteristics

Guaranteed over recommended operating free air temperature and supply voltage range unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
I_{CCR}	Supply Current (Read Mode)	$\overline{CS}$ = L, R/$\overline{W}$ = H		20	28	mA	Note A
I_{CCW}	Supply Current (Write Mode)	$\overline{CS}$ = R/$\overline{W}$ = L		20 + 1.1 (I_W)	27 + 1.1 (1_W)	mA	Note A
I_{CCI}	Supply Current (Idle Mode)	$\overline{CS}$ = H		0.1	0.27	mA	Note A
PD_R	Power Dissipation (Read Mode)	$\overline{CS}$ = L, R/$\overline{W}$ = H		100	154	mW	Note A
PD_W	Power Dissipation (Write Mode)	$\overline{CS}$ = L, R/$\overline{W}$ = L		100 + 5.5 (I_W)	150 + 6 (I_W)	mW	Note A
PD_I	Power Dissipation (Idle Mode)	$\overline{CS}$ = H		0.5	1.5	mW	Note A
$V_{IH(TTL)}$	TTL Input High Voltage		2		V_{CC} + 0.3	V	Note A
$V_{IL(TTL)}$	TTL Input Low Voltage		−0.3		0.8	V	Note A
$I_{IH(TTL)}$	TTL Input High Current		−100		100	μA	Note A
$I_{IL(TTL)}$	TTL Input Low Current		−100		100	μA	Note A

Note 1: Typical values are specified at 25°C and 5V supply.

Note A: This parameter is guaranteed by outgoing testing.

DC and AC Electrical Characteristics—Read Mode

Guaranteed over recommended operating conditions (see table) unless otherwise specified. Read characteristics: $C_{L(RDX, RDY)} < 20$ pF, $R_{L(RDX, RDY)} = 1\ k\Omega$

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
A_V	Differential Voltage Gain (Note 2)	$V_{IN} = 1\ mV_{PP}$ @ 1 MHz DP84600R Only	25	300	350	V/V	Note A
A_V	Differential Voltage Gain	$V_{IN} = 1\ mV_{PP}$ @1 MHz DP84605R Only	160	200	240	V/V	Note A
V_N	Input Noise Voltage	BW = 15 MHz, $L_h = R_h = 0$		0.49	0.65	$nV/\sqrt{Hz}$	Note B
I_N	Input Noise Current			3		$pA/\sqrt{Hz}$	Note B
C_I	Differential Input Capacitance	$V_{IN} = 1\ mV_{PP}$, f = 5 MHz		12	17	pF	Note B
R_I	Differential Input Resistance	f = 5 MHz, $V_{IN} = 1\ mV_{PP}$	720	1250		Ω	Note A
V_{IRANGE}	Input Voltage Dynamic Range	f = 5 MHz, (Note 3)	4	6		mV_{PP}	Note A
$V_{O(OFF)}$	Output Offset Voltage		−150		150	mV	Note A
$R_{O(SE)}$	Single Ended Output Resistance	f = 5 MHz			40	Ω	Note B
I_{OUT}	Output Current	AC Coupled Load, RDX to RDY	1.5	2		mA	Note A
$V_{O(CM)}$	Common Mode Output Voltage at RDX, RDY Pins		2	$V_{CC} - 2.4$	3.5	V	Note A
BW_{1dB}	Voltage Bandwidth −1 dB	$V_{IN} = 1\ mV_{PP}$, $Z_{SOURCE} < 5\Omega$	40	60		MHz	Note B
BW_{3dB}	Voltage Bandwidth −3 dB	$V_{IN} = 1\ mV_{PP}$, $Z_{SOURCE} < 5\Omega$	80	100		MHz	Note B
CMMR	Common Mode Rejection Ratio	$V_{CM} = 100\ mV_{PP}$, @5 MHz	60	90		dB	Note A
PSRR	Power Supply Rejection Ratio	$\Delta V_{CC} = 100\ mV_{PP}$, @5 MHz	60	90		dB	Note A
CSRR	Channel Separation	Unselected Channel $100\ mV_{PP}$	50	60		dB	Note A

Note 1: Typical values are specified at 25°C and 5V supply.

Note 2: Various gain options exist from 160 to 300. See order information.

Note 3: The dynamic input voltage range limit is defined as the point where the gain falls to 90% of its small signal gain value.

Note A: This parameter is guaranteed by outgoing testing.

Note B: The limit values have been determined by characterization data. No outgoing tests are performed.

DC Electrical Characteristics—Write Mode

Guaranteed over recommended operating conditions (see table) unless otherwise specified. Write characteristics: $I_W = 20$ mA, $L_h = 1\ \mu H$, $R_h = 30\Omega$

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
K_W	Write Current Constant	$K_W = A_{WC} \times V_{WC}$	46	50	54	V	Note A
A_{WC}	I_{WC} to I_{HEAD} Current Gain	$R_H = 40\Omega$	18.4	20	21.6	mA	Note A
I_{HM}	Write Current Matching	$I_H = 20$ mA, $R_H = 40\Omega$ (Note 2)	−10		+10	%	Note A
V_{WC}	Write Current Pin Voltage	1 mA < I_W < 40 mA	2.3	2.5	2.7	V	Note A
V_H	Differential Head Voltage Swing	Open Head, $I_W = 20$ mA	5	6.5		V_{PP}	Note A
$I_{H(NS)}$	Unselected Head Current	$I_H = 20$ mA			100	μA	Note A
R_{DAMP}	Damping Resistance	Write Only		300		Ω	Note A
I_H	Head Write Current Range		1		40	mA	Note A
V_{CCF}	V_{CC} Shut-Off Voltage	$I_W < 0.2$ mA	3.6		4.2	V	Note A
$V_{OL(WUS)}$	WUS Low Output Voltage	$I_{OL} = 4$ mA			0.5	V	Note A
$I_{LK(WUS)}$	WUS High Level Output Leakage Current	$V_{OH} = V_{CC}$			100	μA	Note A
C_D	Differential Head Load Capacitance				15	pF	Note B
f_W	WDI Transition Frequency	For WUS = low	1			MHz	Note A
$t_{PWH(WD)}$	WDI Pulse Width (High)		5			ns	Note B
$t_{PWL(WD)}$	WDI Pulse Width (Low)		5			ns	Note B

Note 1: Typical values are specified at 25°C and 5V supply.

Note 2: Write curent matching applies between any two heads.

Note A: This parameter is guaranteed by outgoing testing.

Note B: The limit values have been determined by characterization data. No outgoing tests are performed.

AC Electrical Characteristics

Guaranteed over recommended operating conditions (see table) unless otherwise specified. I_W = 20 mA, L_h = 1 μH, R_h = 40Ω and f(data) = 5 MHz unless otherwise specified.

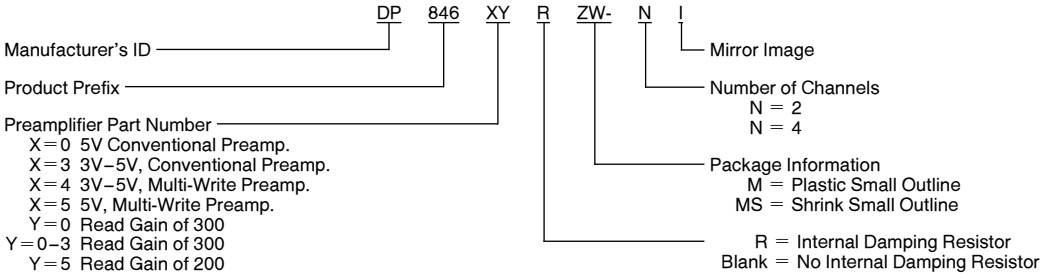
Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units	Test
td_{RW}	Time Delay Switching from Read to Write Modes	R/$\overline{W}$ Transition to 90% of Write Current. $I_W > 5$ mA			0.35	μs	Note A
td_{RWL}	Time Delay Switching from Read to Write Modes	R/$\overline{W}$ Transition to 90% I_{WRITE}. 1 mA $< I_W <$ 5 mA			2	μs	Note A
td_{WR}	Time Delay Switching from Write to Read Modes	R/$\overline{W}$ Transition to 90% of 100 mV Read Signal Envelope			1	μs	Note A
td_{SELECT}	Time Delay Switching from Idle to Either Read or Write Modes	$\overline{CS}$ Negative Transition to 90% I_{WRITE} or 90% of 100 mV, 10 MHz Signal Envelope			0.6	μs	Note A
td_{IDLE}	Time Delay Switching from Either Read or Write to Idle Mode				0.6	μs	Note A
td_{HEAD}	Time Delay Switching from One Head to Another	HS0/HS1 to 90% of 100 mV, 10 MHz Read Signal Envelope			0.6	μs	Note A
td_{UNSAFE}	Time Delay from a Write Safe to a Write Unsafe Condition	WDI Negative Transition to WUS Positive Transition	1		3.6	μs	Note A
td_{SAFE}	Time Delay from Write Unsafe to Write Safe Condition	WDI Negative Transition to WUS Negative Transition			1	μs	Note A
td_{HDI}	Time Delay from WDI to a Current Direction Change in a Head Output	Measurements Made from 50% Points. L_h = 0, R_h = 40		10	20	ns	Note A
ASY_{HD}	Head Current Asymmetry	WDI has 1 ns $t_{r/f}$ Times. L_h = 0, R_h = 40			0.5	ns	Note B
$t_{r/f(HD)}$	Head Current Rise and Fall Times	Measurements Made from 10% to 90% Points. L_h = 0, R_h = 40			6	ns	Note B
$t_{r/f(loaded)}$	Head Current Rise and Fall Times	Measurements Made from 10% to 90% Points. L_h = 1 μH, R_h = 40Ω, I_W = 20 mA		10	16	ns	Note B

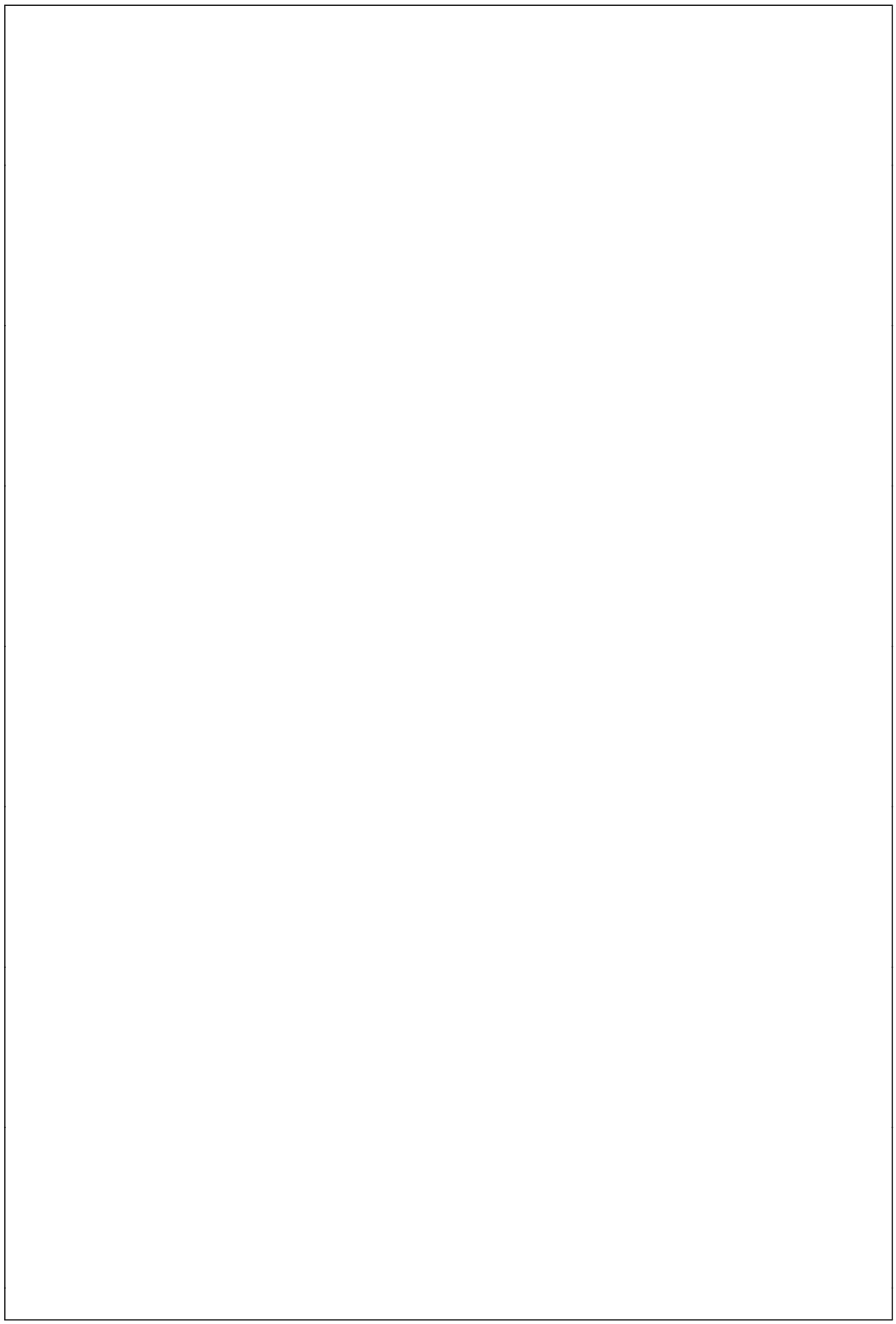
Note 1: Typical values are specified at 25°C and 5V supply.

Note A: This parameter is guaranteed by outgoing testing.

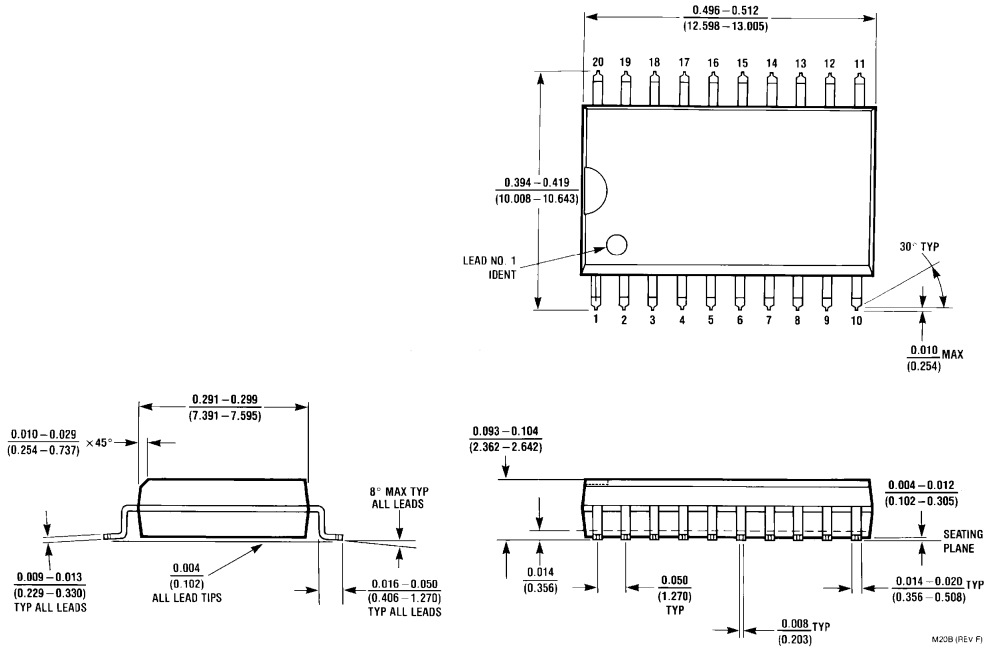
Note B: The limit values have been determined by characterization data. No outgoing tests are performed.

Ordering Information



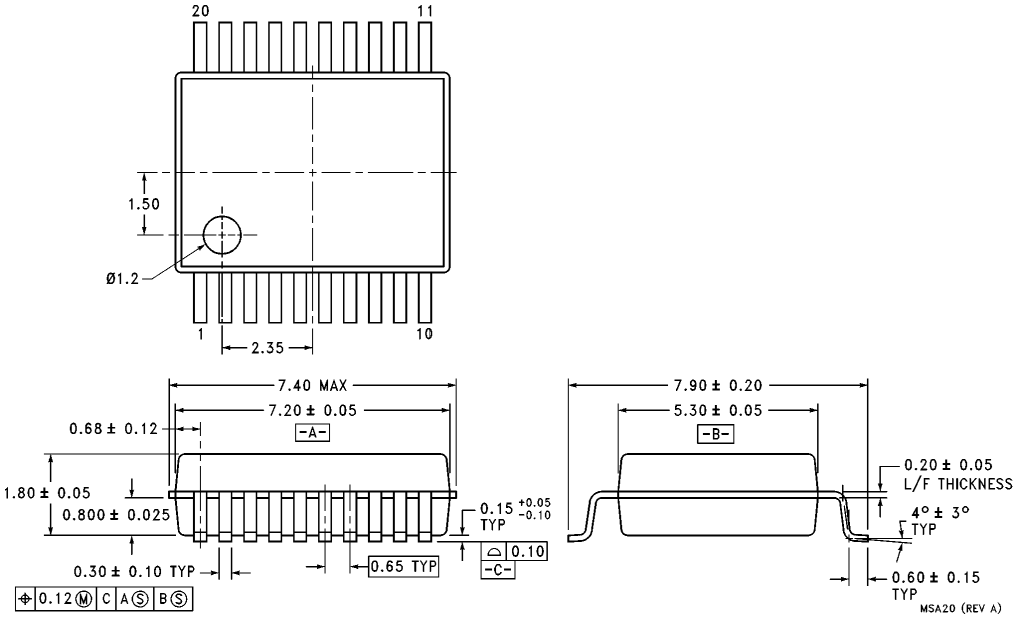


Physical Dimensions inches (millimeters)



Order Number DP84600R or DP84605R
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



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