March 2001

National Semiconductor

# DS90CP22
# 2X2 800 Mbps LVDS Crosspoint Switch

## General Description

DS90CP22 is a 2x2 crosspoint switch utilizing LVDS (Low Voltage Differential Signaling) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The non-blocking design allows connection of any input to any output or outputs. LVDS I/O enable high speed data transmission for point-to-point interconnects. This device can be used as a high speed differential crosspoint, 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter. The mux and demux functions are useful for switching between primary and backup circuits in fault tolerant systems. The 1:2 signal splitter and 2:1 mux functions are useful for distribution of serial bus across several rack-mounted backplanes.

The DS90CP22 accepts LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

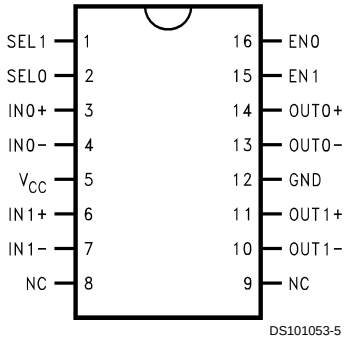
The individual LVDS outputs can be put into TRI-STATE by use of the enable pins.

For more details, please refer to the Application Information section of this datasheet.

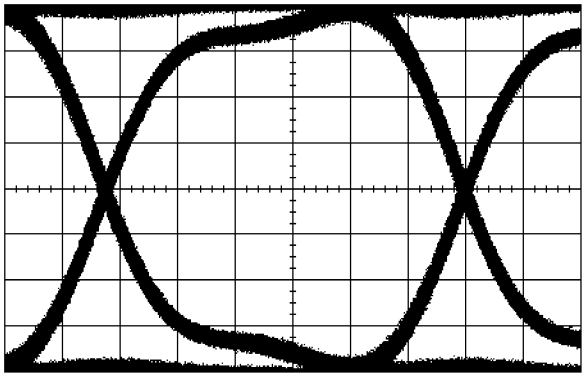
## Features

- Low jitter 800 Mbps fully differential data path
- 75 ps (typ) of pk-pk jitter with PRBS = $2^{23}-1$ data pattern at 800 Mbps
- Single +3.3 V Supply
- Less than 330 mW (typ) total power dissipation
- Non-blocking ''Switch Architecture''
- Balanced output impedance
- Output channel-to-channel skew is 35 ps (typ)
- Configurable as 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter
- LVDS receiver inputs accept LVPECL signals
- Fast switch time of 1.2ns (typ)
- Fast propagation delay of 1.3ns (typ)
- Receiver input threshold < ±100 mV
- 16 lead SOIC package
- Inter-operates with ANSI/TIA/EIA-644-1995 LVDS standard
- Operating Temperature: −40˚C to +85˚C

## Connection Diagram




**Order Number DS90CP22M-8**
**See NS Package Number M16A**



DS101053-10

**Diff. Output Eye-Pattern in 1:2 split mode @ 800 Mbps**
**Conditions: 3.3 V, PRBS = $2^{23}-1$ data pattern,**
**$V_{ID}$ = 300mV, $V_{CM}$ = +1.2 V, 200 ps/div, 100 mV/div**

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.3V to +4V |
| CMOS/TTL Input Voltage (EN0, EN1, SEL0, SEL1) | −0.3V to ($V_{CC}$ + 0.3V) |
| LVDS Receiver Input Voltage (IN+, IN−) | −0.3V to +4V |
| LVDS Driver Output Voltage (OUT+, OUT−) | −0.3V to +4V |
| LVDS Output Short Circuit Current | Continuous |
| Junction Temperature | +150˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Temperature (Soldering, 4 sec.) | +260˚C |
| Maximum Package Power Dissipation at 25˚C | |
| 16L SOIC | 1.435 W |
| 16L SOIC Package Derating | 11.48 mW/˚C above +25˚C |
| ESD Rating: | |
| (HBM, 1.5kΩ, 100pF) | > 5 kV |
| (EIAJ, 0Ω, 200pF) | > 250 V |

## Recommended Operating Conditions

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 3.0 | 3.3 | 3.6 | V |
| Receiver Input Voltage | 0 | | $V_{CC}$ | V |
| Operating Free Air Temperature | -40 | +25 | +85 | ˚C |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS/TTL DC SPECIFICATIONS (EN0,EN1,SEL0,SEL1)** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = 3.6V or 2.0V; $V_{CC}$ = 3.6V | | +7 | +20 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0V or 0.8V; $V_{CC}$ = 3.6V | | ±1 | ±10 | µA |
| $V_{CL}$ | Input Clamp Voltage | $I_{CL}$ = −18 mA | | −0.8 | −1.5 | V |
| **LVDS OUTPUT DC SPECIFICATIONS (OUT0,OUT1)** | | | | | | |
| $V_{OD}$ | Differential Output Voltage | $R_L$ = 75Ω | 270 | 365 | 475 | mV |
| | | $R_L$ = 75Ω, $V_{CC}$ = 3.3V, $T_A$ = 25˚C | 285 | 365 | 440 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between Complimentary Output States | | | | 35 | mV |
| $V_{OS}$ | Offset Voltage (Note 3) | | 1.0 | 1.2 | 1.45 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between Complimentary Output States | | | | 35 | mV |
| $I_{OZ}$ | Output TRI-STATE® Current | TRI-STATE Output, $V_{OUT}$ = $V_{CC}$ or GND | | ±1 | ±10 | µA |
| $I_{OFF}$ | Power-Off Leakage Current | $V_{CC}$ = 0V; $V_{OUT}$ = 3.6V or GND | | ±1 | ±10 | µA |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT+}$ OR $V_{OUT-}$ = 0V | | −15 | −25 | mA |
| $I_{OSB}$ | Both Outputs Short Circuit Current | $V_{OUT+}$ AND $V_{OUT-}$ = 0V | | −30 | −50 | mA |
| **LVDS RECEIVER DC SPECIFICATIONS (IN0,IN1)** | | | | | | |
| $V_{TH}$ | Differential Input High Threshold | $V_{CM}$ = +0.05V or +1.2V or +3.25V, | | 0 | +100 | mV |
| $V_{TL}$ | Differential Input Low Threshold | Vcc = 3.3V | −100 | 0 | | mV |
| $V_{CMR}$ | Common Mode Voltage Range | $V_{ID}$ = 100mV, Vcc = 3.3V | 0.05 | | 3.25 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = +3.0V, $V_{CC}$ = 3.6V or 0V | | ±1 | ±10 | µA |
| | | $V_{IN}$ = 0V, $V_{CC}$ = 3.6V or 0V | | ±1 | ±10 | µA |
| **SUPPLY CURRENT** | | | | | | |
| $I_{CCD}$ | Total Supply Current | $R_L$ = 75Ω, $C_L$ = 5 pF, EN0 = EN1 = High | | 98 | 125 | mA |
| $I_{CCZ}$ | TRI-STATE Supply Current | EN0 = EN1 = Low | | 43 | 55 | mA |

**Note 1:** "Absolute Maximum Ratings" are these beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All typical are given for $V_{CC}$ = +3.3V and $T_A$ = +25˚C, unless otherwise stated.

**Note 3:** $V_{OS}$ is defined and measured on the ATE as ($V_{OH}$ + $V_{OL}$) / 2.

## AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Note 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{SET}$ | Input to SEL Setup Time, *Figures 1, 2* (Note 5) | | 0.7 | 0.5 | | ns |
| $T_{HOLD}$ | Input to SEL Hold Time, *Figures 1, 2* (Note 5) | | 1.0 | 0.5 | | ns |
| $T_{SWITCH}$ | SEL to Switched Output, *Figures 1, 2* | | 0.9 | 1.2 | 1.7 | ns |
| $T_{PHZ}$ | Disable Time (Active to TRI-STATE) High to Z, *Figure 3* | | | 2.1 | 4.0 | ns |
| $T_{PLZ}$ | Disable Time (Active to TRI-STATE) Low to Z, *Figure 3* | | | 3.0 | 4.5 | ns |
| $T_{PZH}$ | Enable Time (TRI-STATE to Active) Z to High, *Figure 3* | | | 25.5 | 55.0 | ns |
| $T_{PZL}$ | Enable Time (TRI-STATE to Active) Z to Low, *Figure 3* | | | 25.5 | 55.0 | ns |
| $T_{LHT}$ | Output Low-to-High Transition Time, 20% to 80%, *Figure 5* | | 290 | 400 | 580 | ps |
| $T_{HLT}$ | Output High-to-Low Transition Time, 80% to 20%, *Figure 5* | | 290 | 400 | 580 | ps |
| $T_{JIT}$ | LVDS Data Path Peak to Peak Jitter, (Note 6) | $V_{ID}$ = 300mV; 50% Duty Cycle; $V_{CM}$ = 1.2V at 800Mbps | | 40 | 90 | ps |
| | | $V_{ID}$ = 300mV; PRBS=$2^{23}$-1 data pattern; $V_{CM}$ = 1.2V at 800Mbps | | 75 | 190 | ps |
| $T_{PLHD}$ | Propagation Low to High Delay, *Figure 6* | | 0.9 | 1.3 | 1.6 | ns |
| | Propagation Low to High Delay, *Figure 6* | $V_{CC}$ = 3.3V, $T_A$ = 25˚C | 1.0 | 1.3 | 1.5 | ns |
| $T_{PHLD}$ | Propagation High to Low Delay, *Figure 6* | | 0.9 | 1.3 | 1.6 | ns |
| | Propagation High to Low Delay, *Figure 6* | $V_{CC}$ = 3.3V, $T_A$ = 25˚C | 1.0 | 1.3 | 1.5 | ns |
| $T_{SKEW}$ | Pulse Skew $\lvert T_{PLHD} - T_{PHLD} \rvert$ | | | 0 | 225 | ps |
| $T_{CCS}$ | Output Channel-to-Channel Skew, *Figure 7* | | | 35 | 80 | ps |

**Note 4:** The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage and temperature) range.

**Note 5:** $T_{SET}$ and $T_{HOLD}$ time specify that data must be in a stable state before and after the SEL transition.

**Note 6:** The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over PVT range with the following equipment test setup: HP70004A (display mainframe) with HP70841B (pattern generator), 5 feet of RG-142 cable with DUT test board and HP83480A (digital scope mainframe) with HP83483A (20GHz scope module).

## AC Timing Diagrams

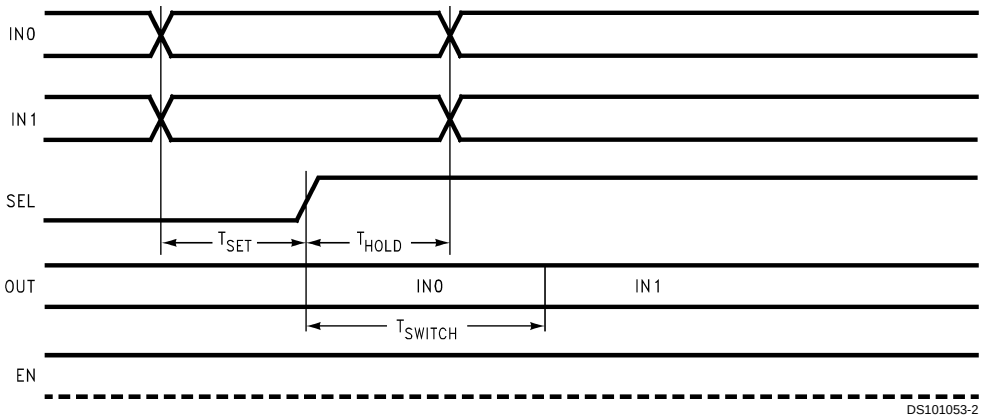



**FIGURE 1. Input-to-Select rising edge setup and hold times and mux switch time**

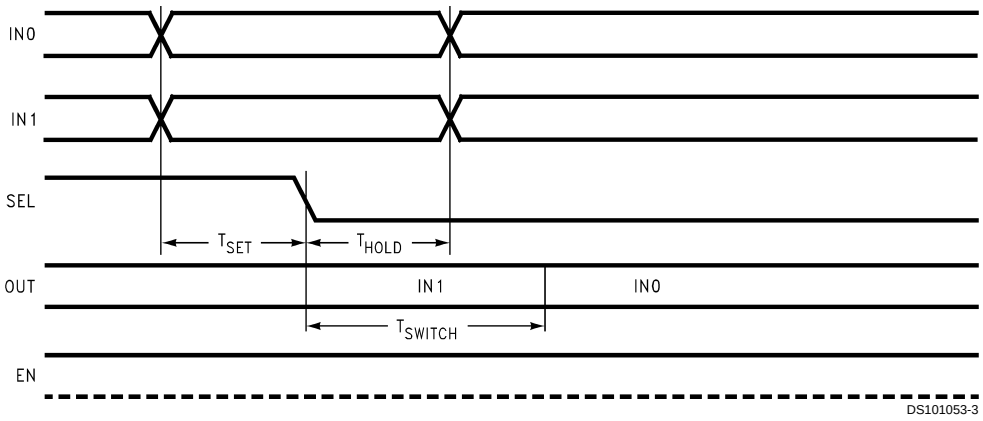



**FIGURE 2. Input-to-Select falling edge setup and hold times and mux switch time**

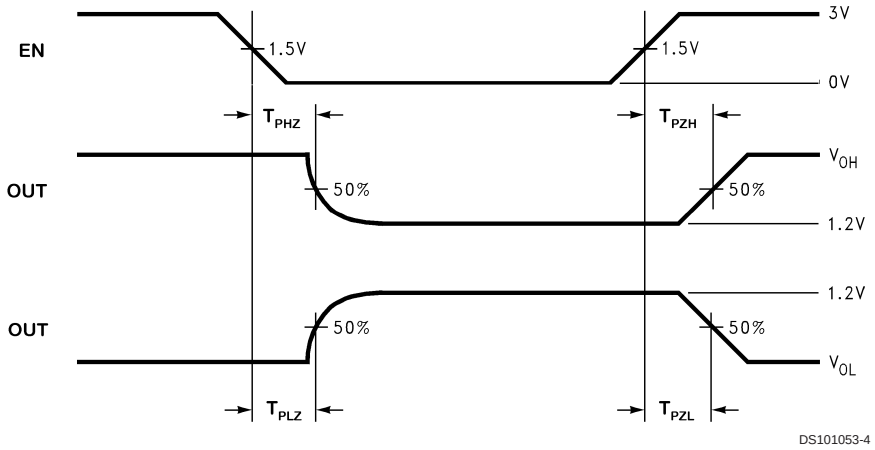



**FIGURE 3. Output active to TRI-STATE and TRI-STATE to active output time**

## AC Timing Diagrams (Continued)

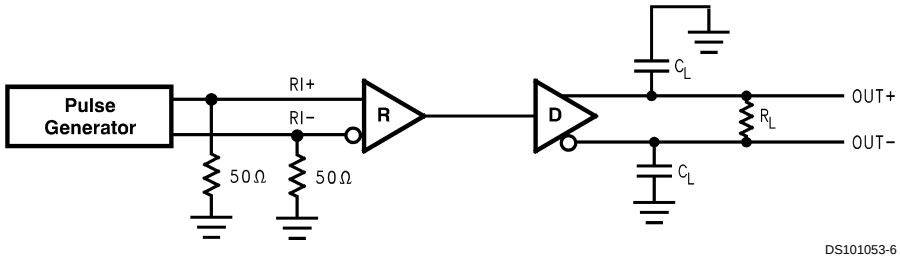



**FIGURE 4. LVDS Output Load**

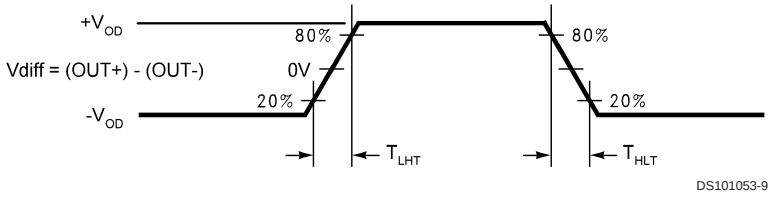



**FIGURE 5. LVDS Output Transition Time**

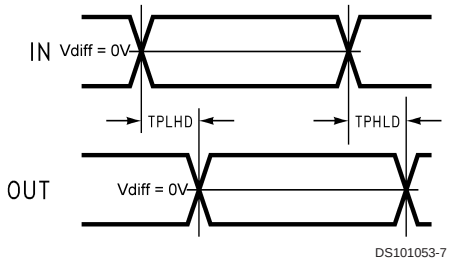



**FIGURE 6. Propagation Delay Low-to-High and High-to-Low**

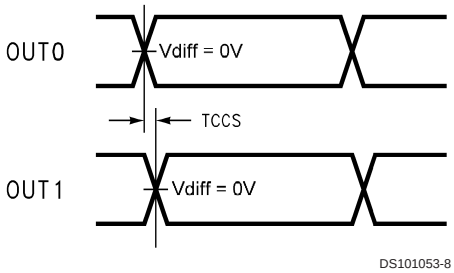



**FIGURE 7. Output Channel-to-Channel Skew in 1:2 splitter mode**

## DS90CP22M-8 Pin Description

| Pin Name | # of Pin | Input/Output | Description |
|---|---|---|---|
| IN+ | 2 | I | Non-inverting LVDS input |
| IN - | 2 | I | Inverting LVDS input |
| OUT+ | 2 | O | Non-inverting LVDS Output |
| OUT - | 2 | O | Inverting LVDS Output |
| EN | 2 | I | A logic low on the Enable puts the LVDS output into TRI-STATE and reduces the supply current |
| SEL | 2 | I | 2:1 mux input select |
| GND | 1 | P | Ground |
| $V_{CC}$ | 1 | P | Power Supply |
| NC | 2 | | No Connect |

## Application Information

**Modes of Operation:**

The DS90CP22M-8 provides three modes of operation. In the 1:2 splitter mode, the two outputs are copies of the same single input. This is useful for distribution / fan-out applications. In the repeater mode, the device operates as a 2 channel LVDS buffer. Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long distance applications. The switch mode provides a crosspoint function. This can be used in a system when primary and redundant paths are supported in fault tolerant applications.

**Input fail-safe:**

The receiver inputs of the DS90CP22M-8 do not have internal fail-safe biasing. For point-to-point and multidrop applications with a single source, fail-safe biasing may not be required. When the driver is off, the link is in-active. If fail-safe biasing is required, this can be accomplished with external high value resistors. The IN+ should be pull to Vcc with 10kΩ and the IN− should be pull to Gnd with 10kΩ. This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.

**Unused LVDS Inputs:**

Unused LVDS Receiver inputs should be tied off to prevent the high-speed sensitive input stage from picking up noise signals. The open input to IN+ should be pull to Vcc with 10kΩ and the open input to IN− should be pull to Gnd with 10kΩ.

**Unused Control Inputs:**

The SEL and EN control input pins have internal pull down devices. Unused pins may be tied off or left as no-connect (if a LOW state is desired).

**Expanding the Number of Output Ports:**

To expand the number of output ports, more than one DS90CP22M-8 can be used. Total propagation delay through the devices should be considered to determine the maximum expansion. For example, if 2 X 4 is desired, than three of the DS90CP22M-8 are required. A minimum of two device propagation delays (2 x 1.3ns = 2.6ns (typ)) can be achieved. For a 2 X 8, a total of 7 devices must be used with propagation delay of 3 x 1.3ns = 3.9ns (typ). The power consumption will increase proportional to the number of devices used.

**PCB Layout and Power System Bypass:**

Circuit board layout and stack-up for the DS90CP22M-8 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. Tantalum capacitors may be in the range 2.2 µF to 10 µF. Voltage rating for tantalum capacitors should be at least 5X the power supply voltage being used. It is recommended practice to use two vias at each power pin of the DS90CP22M-8 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion. The planes should be pulled back from all transmission lines and component mounting pads a distance equal to the width of the widest transmission line or the thickness of the dielectric separating the transmission line from the internal power or ground plane(s) whichever is greater. Doing so minimizes effects on transmission line impedances and reduces unwanted parasitic capacitances at component mounting pads.

There are more common practices which should be followed when designing PCBs for LVDS signaling. Please see Application Note: AN-1108 for additional information.

**Compatibility with LVDS standard:**

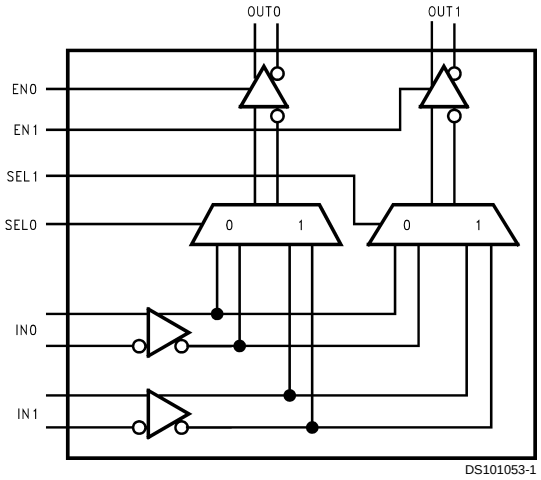
The DS90CP22M-8 is compatible with LVDS and Bus LVDS Interface devices. It is enhanced over standard LVDS drivers in that it is able to driver lower impedance loads with standard LVDS levels. Standard LVDS drivers provide 330mV differential output with a 100Ω load. The DS90CP22M-8 provides 365mV with a 75Ω load or 400mV with 100Ω loads. This extra drive capability is useful in certain multidrop applications.

In backplane multidrop configurations, with closely spaced loads, the effective differential impedance of the line is

## Application Information (Continued)

reduced. If the mainline has been designed for 100Ω differential impedance, the loading effects may reduce this to the 70Ω range depending upon spacing and capacitance load. Terminating the line with a 75Ω load is a better match than with 100Ω and reflections are reduced.

## Block Diagram




DS101053-1

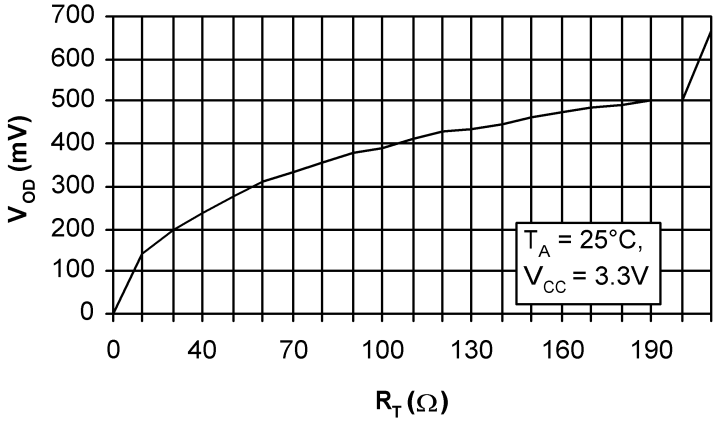
## Function Table

| SEL0 | SEL1 | OUT0 | OUT1 | Mode |
|---|---|---|---|---|
| 0 | 0 | IN0 | IN0 | 1:2 splitter |
| 0 | 1 | IN0 | IN1 | repeater |
| 1 | 0 | IN1 | IN0 | switch |
| 1 | 1 | IN1 | IN1 | 1:2 splitter |

Note: 0 = low, 1 = high
EN0 = EN1 = 1 for enable

## Typical Performance Characteristics

**Diff. Output Voltage ($V_{OD}$) vs. Resistive Load ($R_T$)**

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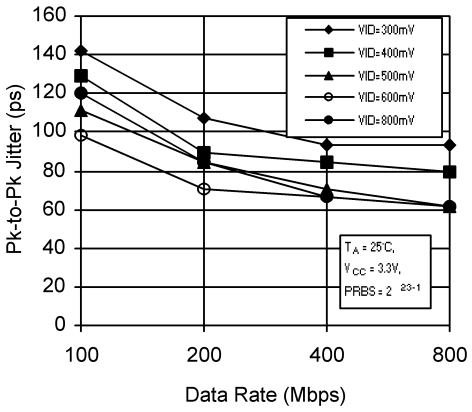
## Typical Performance Characteristics (Continued)

**Peak-to-Peak Output Jitter at $V_{CM}$ = +0.4V vs. VID**

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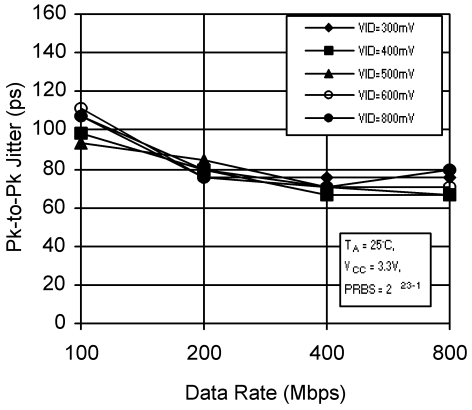
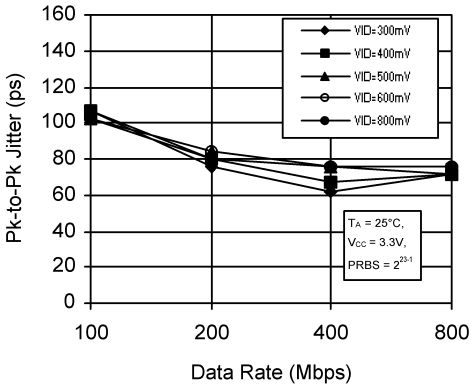
**Peak-to-Peak Output Jitter at $V_{CM}$ = +1.2V vs. VID**



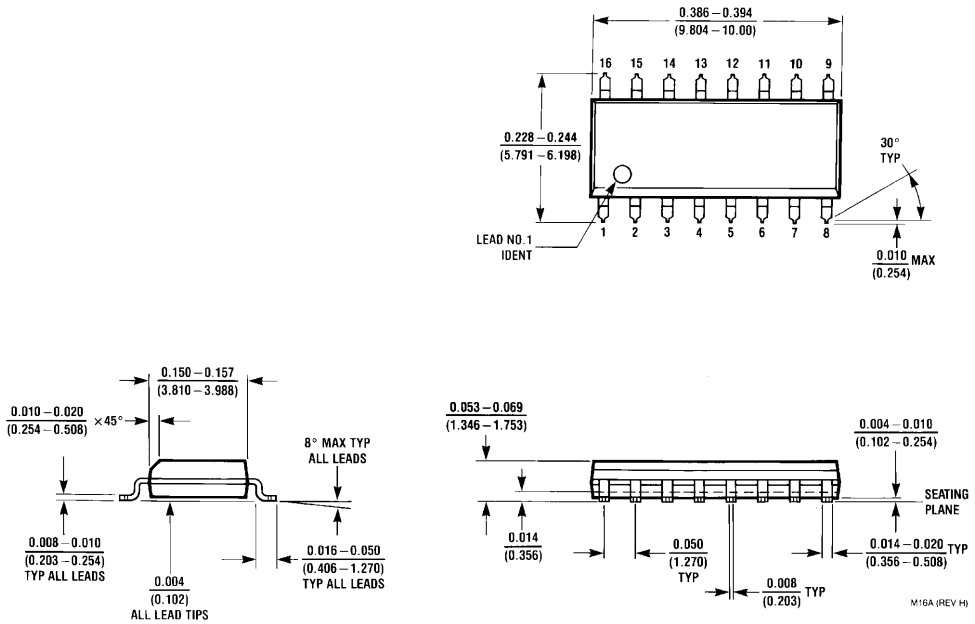

DS101053-13

**Peak-to-Peak Output Jitter at $V_{CM}$ = +1.6V vs. VID**




DS101053-14

## Physical Dimensions inches (millimeters) unless otherwise noted




**Order Number DS90CP22M-8**
**See NS Package Number M16A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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