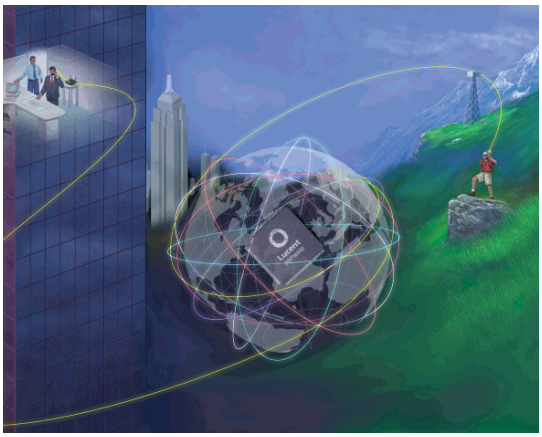
Lucent Technologies
Bell Labs Innovations

DSP16210 Digital Signal Processor



The DSP16210 is the first DSP device based on the DSP16000 digital signal processing core. It is manufactured in a 0.35 µm CMOS technology and offers a 10 ns instruction cycle time at 3 V operation. Designed specifically for applications requiring a large amount of memory, a flexible DMA-based I/O structure, and high cycle efficiency in digital cellular infrastructure systems, the DSP16210 is a signal-coding device that can be programmed to perform a wide variety of fixed-point signal processing functions. The DSP16210 includes a mix of peripherals specifically intended to support processing-intensive but cost-sensitive applications in the area of digital wireless communications.

The large, on-chip RAM (60 Kwords of dual-port RAM) supports downloadable system design—a must for wireless infrastructure—to support field upgrades for evolving digital cellular standards. The DSP16210 can address 60 Kwords of DPRAM and up to 512 Kwords of external storage in both its code/coefficient memory address space and data memory address space. In addition, there are 8 Kwords of internal ROM (IROM) which includes system boot code and hardware development system (HDS) code. The external memory interface (EMI) has both 16- and 32-bit data width capabilities and is designed to support both static RAMs and the new synchronous static RAMs. This device also contains a bit manipulation unit (BMU) and a 3-input, 40-bit arithmetic logic unit (ALU) with add/compare/select (ACS) for enhanced signal coding efficiency and Viterbi acceleration.

To optimize I/O throughput and reduce the I/O service routine burden on the DSP core, the DSP16210 is equipped with two modular I/O units (MIOUs) which manage the simple serial I/O port (SSIO) and the 16-bit parallel host interface (PHIF16) peripherals. The MIOUs optimize I/O throughput and reduce the I/O service routine burden on the core by providing transparent DMA transfers between the peripherals and the on-chip, dual-port RAM.

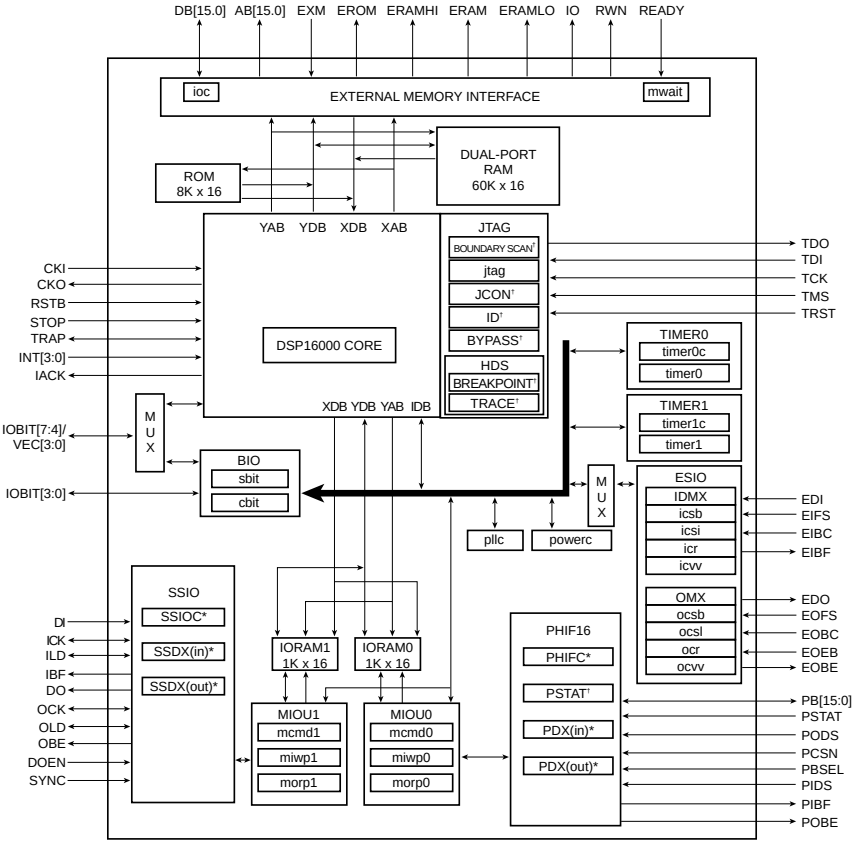
The combination of large on-chip RAM, fast instruction cycle times, and efficient I/O management makes the DSP16210 an ideal solution for supporting multiple channels of voice and data traffic in digital cellular infrastructure equipment.

FEATURES

- Optimized for digital cellular infrastructure applications—speech coding, speech compression, and channel coding
  - — Large, on-chip, dual-port RAM (60 Kwords of DPRAM) eliminates need for fast external SRAM
  - — 3-input, 40-bit arithmetic logic unit (ALU) with add/compare/select (ACS) for Viterbi acceleration
  - — DMA-based I/O—minimizes DSP core overhead for I/O processing
  - — Bit manipulation unit for higher coding efficiency
  - — Flexible power management modes
- 10 ns instruction cycle time at 3 V
- Dual 16 x 16-bit multiplication and 40-bit accumulation in one instruction cycle
- 31 instruction by 32-bit interruptible do-loop cache for high-speed, program-efficient, zero-overhead looping
- Nested interrupts and three interrupt priority levels
- 32-bit sequenced accesses to 512 Kword external instruction/coefficient space (X memory) and 512 Kwords external data space (Y memory)
- 8 Kwords of on-chip ROM with hardware development system and boot code for flexible downloading
- 512 internal and 512 external memory-mapped I/O ports
- On-chip, programmable, PLL clock synthesizer
- Enhanced serial I/O port designed to multiplex/demultiplex 64Kbit/s, 32 Kbits/s, 16 Kbits/s, and 8 Kbits/s channels
- Two dedicated DMA controllers (MIOUs) to off-load I/O processing from DSP core
- 25 Mbits/s simple serial I/O port (SSIO) coupled with MIOU1 to support low overhead DMA-based I/O

- 16-bit parallel host interface (PHIF16) coupled with MIOU0 to support low overhead DMA-based I/O
  - — Supports either 8- or 16-bit external bus configurations (8-bit external configuration supports either 8- or 16-bit logical transfers)
  - — Supports either *Motorola** or *Intel*† protocols
- 8-bit control I/O interface
- *IEEE*‡ P1149.1 test port (JTAG boundary scan)
- Full-speed in-circuit emulation hardware development system on-chip with eight address and two data watchpoint units
- Supported by DSP16210 software and hardware development tools
- Pin and object-code compatible with the DSP1620
- 132-pin BQFP package and 144-pin TQFP package

DSP16210 Block Diagram



*These registers are accessible through the attached MIOU only.
†These registers are accessible through the pins only.

* Motorola *is a registered trademark of Motorola, Inc.*
†Intel *is a registered trademark of Intel Corp.*
‡ IEEE *is a registered trademark of The Institute of Electrical and Electronics Engineers.*

For additional information, contact your Microelectronics Group Account Manager or the following:

❑ Internet
http://www.lucent.com/micro

❑ e-mail
docmaster@micro.lucent.com

❑ Microelectronics Group
Lucent Technologies Inc.
555 Union Boulevard
Room 30L-15P-BA
Allentown, PA 18103
1-800-372-2447
FAX 610-712-4106

In Canada, call:
1-800-553-2448
FAX 610-712-4106

❑ Microelectronics Group Asia/Pacific
Lucent Technologies Singapore Pte. Ltd.
77 Science Park Drive
#03-18 Cintech III
Singapore 118256
Tel. (65) 778 8833
FAX (65) 777 7495

❑ Microelectronics Group
Lucent Technologies Japan Ltd.
7-18, Higashi-Gotanda 2-chome
Shinagawa-ku, Tokyo 141
Japan
Tel. (81) 3 5421 1600
FAX (81) 3 5421 1700

For data requests in Europe:

❑ Microelectronics Group Dataline
Tel. (44) 1189 324 299
FAX (44) 1189 328 148

For technical inquiries in Europe:

❑ Germany:	**(49) 89 95086 0** (Munich)
United Kingdom:	**(44) 1344 865 900** (Bracknell UK)
France:	**(33) 1 41 45 77 00** (Paris)
Sweden:	**(46) 8 600 7070** (Stockholm)
Finland:	**(358) 9 4354 2800** (Helsinki)
Italy:	**(39) 2 6601 1800** (Milan)
Spain:	**(34) 1 807 1441** (Madrid)

September 1997
OT97-347WDSP

microelectronics group

Lucent Technologies
Bell Labs Innovations