Product Note
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microelectronics group

Lucent Technologies
Bell Labs Innovations

DSP1620 Digital Signal Processor

Features

- Optimized for digital cellular infrastructure applications—equalization, channel coding, speech coding
  - — Large, on-chip RAM (32 Kwords) that eliminates need for fast external SRAM
  - — ECCP for equalization and channel coding support
  - — DMA-based I/O that minimizes DSP core overhead for I/O processing
  - — Bit manipulation unit for higher coding efficiency
- On-chip, programmable, PLL clock synthesizer
- 8.3 ns (120 MIPS), 10.0 ns (100 MIPS), 11.1 ns (90 MIPS) instruction cycle times at 3 V and 12.5 ns (80 MIPS) instruction cycle times at 5 V
- Flexible power management modes
- 32 Kwords of on-chip dual-port RAM (DPRAM)
- Support for 128 Kwords external data access
- Four external vectored interrupts
- 25 Mbit/s serial I/O port (SIO) with multiprocessor capability—16-bit data channel, 8-bit protocol channel
- Two dedicated DMA controllers (MIOUs) to off-load I/O processing from DSP core
- 25 Mbit/s simple serial IO port (SSIO) coupled with MIOU0 to support low overhead DMA-based I/O
- 16-bit parallel host interface (PHIF16) coupled with MIOU1 to support low overhead DMA-based I/O
- Supports either 8- or 16-bit external bus configurations
- Supports either 8- or 16-bit logical transfers in 8-bit external configuration
- *Motorola** or *Intel*† compatible
- Sequenced accesses to X and Y external memory
- Single-cycle squaring feature
- 16 x 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Instruction cache for high-speed, program-efficient, zero-overhead looping
- 8-bit control IO interface
- 256 memory-mapped IO ports
- *IEEE*‡ P1149.1 test port (JTAG boundary scan)
- Full-speed in-circuit emulation hardware development system on-chip
- Supported by DSP1620 software and hardware development tools
- On-chip boot routines for flexible downloading
- 132-pin BQFP package and 144-pin TQFP package

* *Motorola* is a registered trademark of Motorola Inc.
† *Intel* is a registered trademark of Intel Corp.
‡ *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Description

The DSP1620 is a DSP1600 core-based fixed-point digital signal processor with a large amount of on-chip RAM and a flexible DMA-based I/O structure that is designed specifically for digital cellular infrastructure applications. This device also contains a bit manipulation unit (BMU) and an error correction coprocessor (ECCP) for enhanced signal coding efficiency. The DSP1620 offers 120, 100, or 90 MIPS performance at 3 V and 80 MIPS performance at 5 V.

The large on-chip RAM (32 Kwords of dual-port RAM) supports downloadable system design—a must for wireless infrastructure to support field upgrades for evolving digital cellular standards. The DSP1620 can address 30 Kwords of DPRAM and up to 64 Kwords of external storage in its code and coefficient memory address space. In addition, the DSP1620 can address 32 Kwords of on-chip DPRAM and up to 128 Kwords of external storage in its data memory address space.

To optimize I/O throughput and reduce the I/O service routine burden on the DSP core, the DSP1620 is equipped with two modular I/O units (MIOU) which manage one of the serial ports (SSIO) and the 16-bit parallel host interface (PHIF16) peripherals. The MIOUs provide transparent DMA transfers between the peripherals and the on-chip, dual-port RAM.

The error correction coprocessor is a powerful hardware engine for Viterbi decoding with instructions for maximum likelihood sequence estimation (MLSE) equalization and convolutional decoding.

The combination of a large, on-chip RAM, 120 MIPS performance, and efficient I/O management makes the DSP1620 an ideal solution for supporting multiple channels of voice and data traffic in digital cellular infrastructure equipment.

The device is packaged in a 132-pin BQFP and a 144-pin TQFP and is available with 12.5 ns and 8.3 ns, 10.0 ns, 11.1 ns instruction cycle speeds at 5 V and 3 V, respectively.

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