Microelectronics
Product Note
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Lucent Technologies
Bell Labs Innovations

DSP1618x16 Digital Signal Processor
DSP1618x24 Digital Signal Processor

Features

- Optimized for digital cellular applications with a bit manipulation unit and an error correction coprocessor for higher signal coding efficiency
- 20 ns, 25 ns, and 30 ns instruction cycle times at 5 V; 33 ns and 38 ns instruction cycle times at 3 V and 2.7 V, respectively
- Mask-programmable clock options: 1X at 25 ns, 2X at 20 ns, crystal oscillator, small signal, CMOS, and TTL
- Low power consumption:
  — Error correction coprocessor (ECCP) for power-efficient hardware acceleration
  — Non-ECCP mode power consumption:
    <10.5 mW/MIPS typical at 5 V
    < 3.8 mW/MIPS typical at 3 V
    < 3.1 mW/MIPS typical at 2.7 V
- Flexible power management modes:
  — Standard sleep:
    <1.2 mW/MIPS at 5 V
    <0.5 mW/MIPS at 3 V
  — Sleep with slow internal clock:
    <3.0 mW at 5 V
    <1.2 mW at 3 V
  — Hardware STOP (pin halts DSP):<50 μA
- Low-profile TQFP package (1.5 mm) available
- Sequenced accesses to X and Y external memory spaces
- Pin compatible with the DSP1616/1617
- Single-cycle squaring
- 16 x 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Instruction cache for high-speed, program-efficient, zero-overhead looping
- Two external vectored interrupts and trap
- 8-bit parallel host interface
- 8-bit control I/O interface
- 256 memory-mapped I/O ports, one internally decoded for glueless device interfacing
- Mask-programmable memory map option: The DSP1618x24 features 24 Kwords of on-chip ROM and access to 16 Kwords of external ROM in the same map. The DSP1618x16 features 16 Kwords of on-chip ROM and access to 32 Kwords of external ROM in the same map. Both feature 4 Kwords of dual-port RAM and a secure option for on-chip ROM
- Dual 25 Mbit/s serial I/O ports with multiprocessor capability—16-bit data channel, 8-bit protocol channel
- *IEEE** P1149.1 test port (JTAG with boundary scan)
- Full-speed in-circuit emulation hardware development system on-chip
- Supported by DSP1618 software and hardware development tools

Description

Designed specifically for low-power applications in digital cellular systems, the DSP1618 is a signal coding device that can be programmed to perform a wide variety of fixed-point signal processing functions. The device is based on the DSP1600 core with a bit manipulation unit and error correction coprocessor for enhanced signal coding efficiency. The DSP1618 includes a mix of peripherals specifically intended to support processing-intensive but cost-sensitive applications in the area of digital mobile communications. In addition to 16 or 24 Kwords of ROM, the device contains 4 Kwords of dual-port RAM (DPRAM) which allow simultaneous access to two RAM locations in a single instruction cycle.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers.

Description (continued)

The DSP1618 is pin-for-pin compatible with the DSP1616-x30, while providing more memory and architectural enhancements including an external memory sequencer, an error correction coprocessor for more efficient Viterbi decoding, and an 8-bit parallel host interface for hardware flexibility. These features make the DSP1618 an ideal solution for the baseband signal processing requirements in GSM terminal and base station applications.

The error correction coprocessor (ECCP) is a powerful hardware engine for Viterbi decoding with instructions for a wide range of maximum likelihood sequence estimation (MLSE) equalization and convolutional decoding.

The DSP1618 supports 5 V, 3 V, and 2.7 V operation and flexible power management modes required for portable cellular terminals. Several control mechanisms achieve low-power operation, including a STOP pin for placing the DSP into a fully static, halted state and a programmable power control register used to power down unused on-chip I/O units. These power management modes allow for trade-offs between power reduction and wake-up latency requirements. During system standby, power consumption is reduced to less than 50 μA.

The device is packaged in a 100-pin PQFP or a 100-pin TQFP and is available with 20 ns, 25 ns, 30 ns, 33 ns, and 38 ns instruction cycle speeds.

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