Microelectronics
Product Note
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Lucent Technologies
Bell Labs Innovations

DSP1628 Digital Signal Processor

Features

- Optimized for digital cellular applications such as half-rate and enhanced full-rate GSM, with a bit manipulation unit and an error correction co-processor for higher signal coding efficiency
- 19 ns instruction cycle time at 2.7 V
- Low power consumption
  — <0.7 mW/MIP typical at 2.7 V
- Low profile TQFP package (1.6 mm)
- Sequenced accesses to X and Y external memory spaces
- Pin compatible with DSP1627
- Single cycle squaring
- 16 x 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Instruction cache for high-speed, program-efficient, zero-overhead looping
- Two external vectored interrupts and trap
- 48 Kwords on-chip ROM (with secure option), 7 Kwords on-chip dual-port RAM
- Dual 25 Mbit/s serial I/O ports with multiprocessor capability – 16-bit data channel, 8-bit protocol channel
- 8-bit parallel host interface
- 8-bit control I/O interface
- 256 memory mapped I/O ports, one internally decoded for glueless device interfacing
- *IEEE** P1149.1 test port (JTAG with boundary scan)
- Full-speed in-circuit emulation hardware development system on-chip
- Supported by DSP1628 software and hardware development tools

* IEEE is a registered trademark of The Institute of Electrical and Electronics Engineers.

Description

Designed specifically for low-power applications in digital cellular systems, the DSP1628 is a signal coding device that can be programmed to perform a wide variety of fixed-point signal processing functions. The device is based on the DSP1600 core with a bit manipulation unit and error correction coprocessor for enhanced signal coding efficiency. The DSP1628 includes a mix of peripherals specifically intended to support processing-intensive but cost-sensitive application in the area of digital mobile communications. In addition to 48 Kwords of ROM, the device contains 7 Kwords of dual-port RAM (DPRAM) which allow simultaneous access to two RAM locations in a single instruction cycle.

The DSP1628 is instruction set-compatible with the DSP1618, while providing more memory and higher performance. This makes the DSP1628 an ideal solution for the baseband signal processing requirements in GSM terminals, especially those implementing half-rate and enhanced full-rate speech coding.

The error correction coprocessor (ECCP) is a powerful hardware engine for Viterbi decoding with instructions for a wide range of maximum likelihood sequence estimation (MLSE) and convolutional decoding.

The DSP1628 supports 2.7 V operation and flexible power management modes required for portable cellular terminals. Several control mechanisms achieve low-power operation, including a STOP pin for placing the DSP into a fully static, halted state and a programmable power control register used to power down unused chip I/O units. These power management modes allow for tradeoffs between power reduction and wake-up latency requirements. During system standby, power consumption is reduced to less than 50 μA.

The device is packaged in a 100-pin TQFP.

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