**Advance Information**
**January 1997**

microelectronics group

Lucent Technologies
Bell Labs Innovations

# DSP1628x16 Digital Signal Processor
# DSP1628x08 Digital Signal Processor

## Features

- Optimized for digital cellular applications with a bit manipulation unit and an error correction coprocessor (ECCP) for higher signal coding efficiency
- On-chip, programmable, PLL clock synthesizer
- 12.5 ns and 19.2 ns instruction cycle times at 2.7 V
- Mask-programmable memory map option: The DSP1628 features 48 Kwords on-chip ROM and 16 Kwords or 8 Kwords on-chip dual-port RAM and a secure option for on-chip ROM
- Low power consumption:
  — Error correction coprocessor (ECCP) for power efficient hardware acceleration
  — Non-ECCP mode power consumption: <1.9 mW/MIPS typical at 2.7 V
- Flexible power management modes:
  — Standard sleep: 0.2 mW/MIPS typical at 2.7 V
  — Sleep with slow internal clock: 0.7 mW typical at 2.7 V
  — Hardware STOP (pin halts DSP): <50 µA
- Mask-programmable clock options: small signal and CMOS
- Low-profile TQFP package (1.6 mm) available
- Sequenced accesses to X and Y external memory
- Object code compatible with the DSP1618
- Single-cycle squaring
- 16 x 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Instruction cache for high-speed, program-efficient, zero-overhead looping
- Dual 25 Mbit/s serial I/O ports with multiprocessor capability—16-bit data channel, 8-bit protocol channel
- 8-bit parallel host interface
  —Supports 8- or 16-bit transfers
  —*Motorola** or *Intel*† compatible
- 8-bit control I/O interface
- 256 memory mapped I/O ports
- *IEEE*‡ P1149.1 test port (JTAG boundary scan)
- Full-speed in-circuit emulation hardware development system on-chip
- Supported by DSP1628 software and hardware development tools
- Pin compatible with the 1627; note that TRST replaces a $V_{DD}$ pin

* *Motorola* is a registered trademark of Motorola Inc.
† *Intel* is a registered trademark of Intel Corporation.
‡ *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers.

## Description

The DSP1628 digital signal processor offers 80 MIPS and 52 MIPS operation at 2.7 V. Designed specifically for applications requiring low power dissipation in digital cellular systems, the DSP1628 is a signal-coding device that can be programmed to perform a wide variety of fixed-point signal processing functions. The device is based on the DSP1600 core with a bit manipulation unit for enhanced signal coding efficiency, an external memory sequencer, an error correction coprocessor (ECCP) for more efficient Viterbi decoding, and an 8-bit parallel host interface for hardware flexibility. The DSP1628 includes a mix of peripherals specifically intended to support processing-intensive but cost-sensitive applications in the area of digital wireless communications.

The DSP1628 contains 48 Kwords of internal ROM, and either 8 or 16 Kwords of dual-port RAM (DPRAM), which allows simultaneous access to two RAM locations in a single instruction cycle. When the ECCP is active, the core cannot access the fourth 1 Kword bank of dual-port RAM. This bank is used by the ECCP for storing traceback information. Locations of ECCP memory are at addresses 0x0C00—0x0FFF

While providing more memory, the DSP1628 is object code compatible with the DSP1618 with the following exceptions:

— ECCP Busy Flag which indicates error correction coprocessor activity has changed its condition field.

| CON | Condition |
|---|---|
| 11100 | lock |
| 11101 | ebusy |

— The SIO interrupts (IBF and OBE) are cleared one instruction cycle AFTER reading or writing the serial data registers, (**sdx**[in] or **sdx**[out]). To account for this added latency, the user must insure that a single instruction (NOP or any other valid DSP16XX instruction) follows the **sdx** register read or write instruction prior to exiting an interrupt service routine (via an ireturn or goto pi instruction) or before checking the **ins** register for the SIO flag status. Adding this instruction insures that interrupts are not reported incorrectly following an ireturn or that stale flags are not read from the **ins** register. Refer to TECHNICAL ADVISORY #23.

The DSP1628 is pin compatible with the DSP1627. Note that TRST, JTAG test reset, replaces a $V_{DD}$ pin. When asserted low, TRST asynchronously resets the JTAG TAP controller. In an application environment, even if the JTAG TAP controller is not used, this pin must be asserted prior to or concurrent with RSTB. At initial powerup, or if the supply voltage falls below $V_{DD}$ MIN and a device reset is required, both TRST and RSTB must be asserted to initialize the device.

The DSP1628 supports 2.7 V operation and flexible power management modes required for portable cellular terminals. Several control mechanisms achieve low-power operation, including a STOP pin for placing the DSP into a fully static, halted state and a programmable power control register used to power down unused on-chip I/O units. These power management modes allow for tradeoffs between power reduction and wake-up latency requirements. During system standby, power consumption is reduced to less than 50 µA.

The on-chip programmable clock synthesizer can be driven by an external clock whose frequency is a fraction of the instruction rate.

The device is packaged in a 100-pin BQFP or a 100-pin TQFP and is available with 12.5 ns, and 19.2 ns instruction cycle speeds at 2.7 V.

## Pin Information

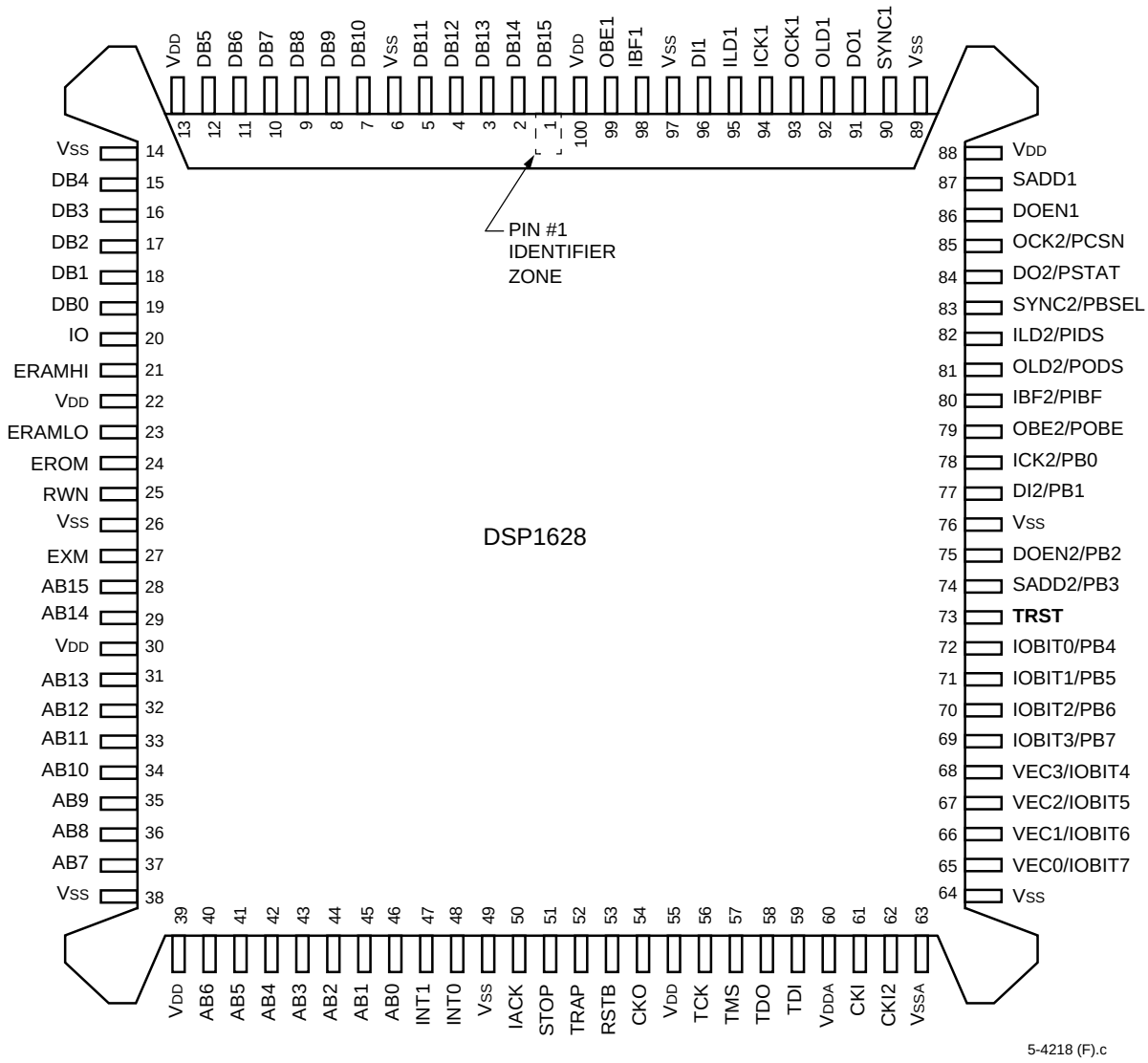


**Figure 1. DSP1628 100-Pin BQFP**

## Pin Information (continued)

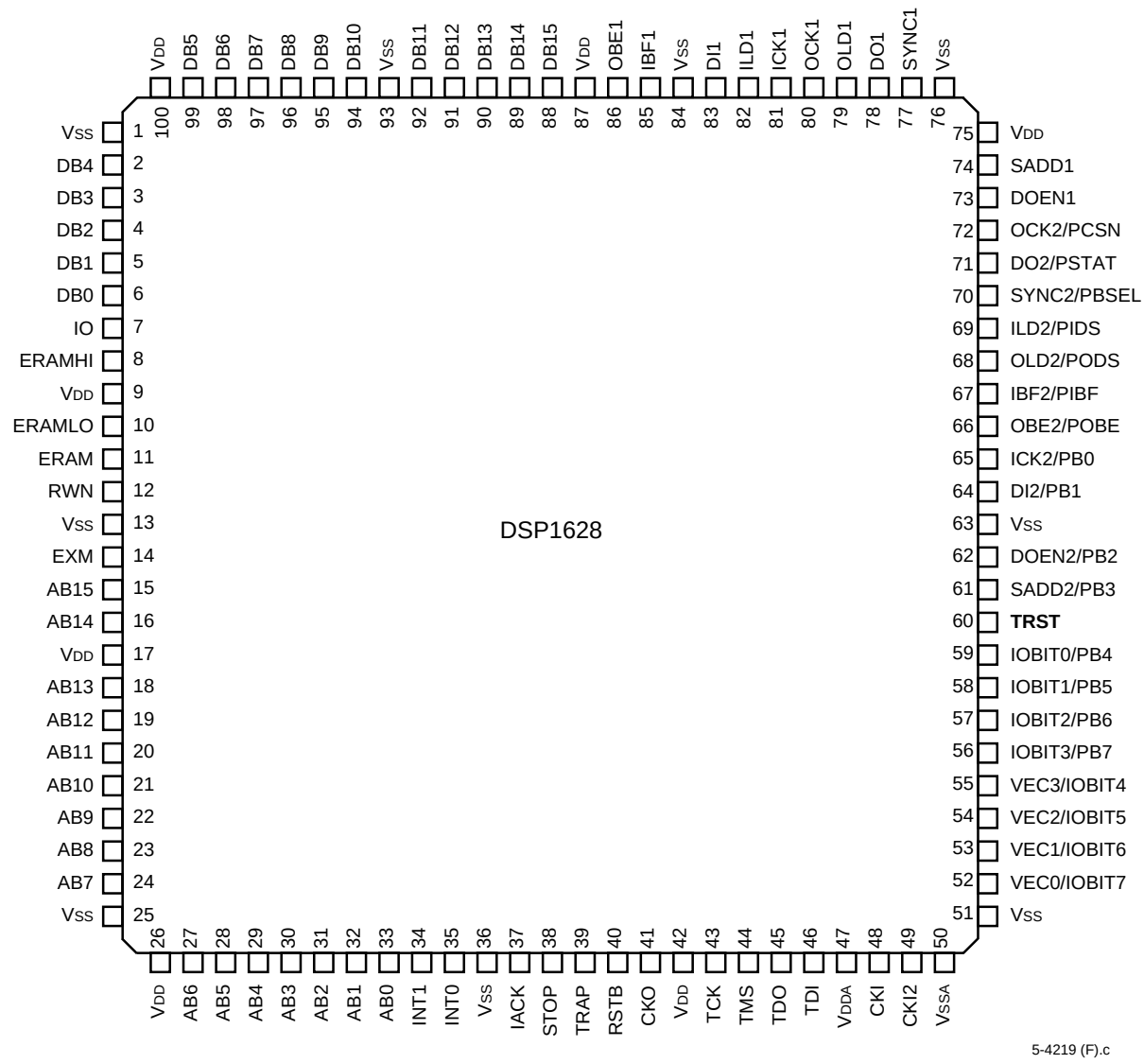


**Figure 2. DSP1628 100-Pin TQFP**

## Pin Information (continued)

The functionality of pins 61 and 62 (TQFP pins 48 and 49) are mask-programmable. Input levels on all I and I/O type pins are designed to remain at full CMOS levels when not driven by the DSP.

**Table 1. Pin Descriptions**

| BQFP Pin | TQFP Pin | Symbol | Type | Name/Function | | |
|---|---|---|---|---|---|---|
| 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 15, 16, 17, 18, 19 | 88, 89, 90, 91, 92, 94, 95, 96, 97, 98, 99, 2, 3, 4, 5, 6 | DB[15:0] | I/O* | External Memory Data Bus 15—0. | | |
| 20 | 7 | IO | O† | Data Address 0x4000 to 0x40FF I/O Enable. | | |
| 21 | 8 | ERAMHI | O† | Data Address 0x8000 to 0xFFFF External RAM Enable. | | |
| 23 | 10 | ERAMLO | O† | Data Address 0x4100 to 0x7FFF External RAM Enable. | | |
| 24 | 11 | EROM | O† | Program Address External ROM Enable. | | |
| 25 | 12 | RWN | O† | Read/Write Not. | | |
| 27 | 14 | EXM | I | External ROM Enable. | | |
| 28, 29, 31, 32, 33, 34, 35, 36, 37, 40, 41, 42, 43, 44, 45, 46 | 15, 16, 18, 19, 20, 21, 22, 23, 24, 27, 28, 29, 30, 31, 32, 33 | AB[15:0] | O* | External Memory Address Bus 15—0. | | |
| 47 | 34 | INT1 | I | Vectored Interrupt 1. | | |
| 48 | 35 | INT0 | I | Vectored Interrupt 0. | | |
| 50 | 37 | IACK | O* | Interrupt Acknowledge. | | |
| 51 | 38 | STOP | I | STOP Input Clock. | | |
| 52 | 39 | TRAP | I/O* | Nonmaskable Program Trap/Breakpoint Indication. | | |
| 53 | 40 | RSTB | I | Reset Bar. | | |
| 54 | 41 | CKO | O† | Processor Clock Output. | | |
| 56 | 43 | TCK | I | JTAG Test Clock. | | |
| 57 | 44 | TMS | I‡ | JTAG Test Mode Select. | | |
| 58 | 45 | TDO | O§ | JTAG Test Data Output. | | |
| 59 | 46 | TDI | I‡ | JTAG Test Data Input. | | |
| | | | | **Mask-Programmable Input Clock Option** | | |
| | | | | **CMOS** | **Small Signal** | **CMOS** |
| 61 | 48 | CKI** | I | CKI | VAC | CKI |
| 62 | 49 | CKI2** | I | VSSA | VCM | Open |
| 65 | 52 | VEC0/IOBIT7 | I/O* | Vectored Interrupt Indication 0/Status/Control Bit 7. | | |
| 66 | 53 | VEC1/IOBIT6 | I/O* | Vectored Interrupt Indication 1/Status/Control Bit 6. | | |
| 67 | 54 | VEC2/IOBIT5 | I/O* | Vectored Interrupt Indication 2/Status/Control Bit 5. | | |
| 68 | 55 | VEC3/IOBIT4 | I/O* | Vectored Interrupt Indication 3/Status/Control Bit 4. | | |

* 3-states when RSTB = 0, or by JTAG control.
† 3-states when RSTB = 0 and INT0 = 1. Output = 1 when RSTB = 0 and INT0 = 0, except CKO which is free-running.
§ Pull-up devices on input.
‡ 3-states by JTAG control.
** Mask-programmable.
†† For SIO multiprocessor applications, add 5 kΩ external pull-up resistors to SADD1 and/or SADD2 for proper initialization.

## Pin Information (continued)

**Table 1. Pin Descriptions** (continued)

| BQFP Pin | TQFP Pin | Symbol | Type | Name/Function |
|---|---|---|---|---|
| 69 | 56 | IOBIT3/PB7 | I/O* | Status/Control Bit 3/PHIF Data Bus Bit 7. |
| 70 | 57 | IOBIT2/PB6 | I/O* | Status/Control Bit 2/PHIF Data Bus Bit 6. |
| 71 | 58 | IOBIT1/PB5 | I/O* | Status/Control Bit 1/PHIF Data Bus Bit 5. |
| 72 | 59 | IOBIT0/PB4 | I/O* | Status/Control Bit 0/PHIF Data Bus Bit 4. |
| 73 | 60 | TRST | I | JTAG Test Reset (new pin, active-low). |
| 74 | 61 | SADD2/PB3†† | I/O* | SIO2 Multiprocessor Address/PHIF Data Bus Bit 3. |
| 75 | 62 | DOEN2/PB2 | I/O* | SIO2 Data Output Enable/PHIF Data Bus Bit 2. |
| 77 | 64 | DI2/PB1 | I/O* | SIO2 Data Input/PHIF Data Bus Bit 1. |
| 78 | 65 | ICK2/PB0 | I/O* | SIO2 Input Clock/PHIF Data Bus Bit 0. |
| 79 | 66 | OBE2/POBE | O* | SIO2 Output Buffer Empty/PHIF Output Buffer Empty. |
| 80 | 67 | IBF2/PIBF | O* | SIO2 Input Buffer Full/PHIF Input Buffer Full. |
| 81 | 68 | OLD2/PODS | I/O* | SIO2 Output Load/PHIF Output Data Strobe. |
| 82 | 69 | ILD2/PIDS | I/O* | SIO2 Input Load/PHIF Input Data Strobe. |
| 83 | 70 | SYNC2/PBSEL | I/O* | SIO2 Multiprocessor Synchronization/PHIF Byte Select. |
| 84 | 71 | DO2/PSTAT | I/O* | SIO2 Data Output/PHIF Status Register Select. |
| 85 | 72 | OCK2/PCSN | I/O* | SIO2 Output Clock/PHIF Chip Select Not. |
| 86 | 73 | DOEN1 | I/O* | SIO1 Data Output Enable. |
| 87 | 74 | SADD1†† | I/O* | SIO1 Multiprocessor Address. |
| 90 | 77 | SYNC1 | I/O* | SIO1 Multiprocessor Synchronization. |
| 91 | 78 | DO1 | O* | SIO1 Data Output. |
| 92 | 79 | OLD1 | I/O* | SIO1 Output Load. |
| 93 | 80 | OCK1 | I/O* | SIO1 Output Clock. |
| 94 | 81 | ICK1 | I/O* | SIO1 Input Clock. |
| 95 | 82 | ILD1 | I/O* | SIO1 Input Load. |
| 96 | 83 | DI1 | I | SIO1 Data Input. |
| 98 | 85 | IBF1 | O* | SIO1 Input Buffer Full. |
| 99 | 86 | OBE1 | O* | SIO1 Output Buffer Empty. |
| 6, 14, 26, 38, 49, 64, 76, 89, 97 | 93, 1, 13, 25, 36, 51, 63, 76, 84 | $V_{SS}$ | P | Ground. |
| 13, 22, 30, 39, 55, 88, 100 | 100, 9, 17, 26, 42, 60, 75, 87 | $V_{DD}$ | P | Power Supply. |
| 60 | 47 | $V_{DDA}$ | P | Analog Power Supply. |
| 63 | 50 | $V_{SSA}$ | P | Analog Ground. |

* 3-states when RSTB = 0, or by JTAG control.
† 3-states when RSTB = 0 and INT0 = 1. Output = 1 when RSTB = 0 and INT0 = 0, except CKO which is free-running.
§ Pull-up devices on input.
‡ 3-states by JTAG control.
** Mask-programmable.
†† For SIO multiprocessor applications, add 5 kΩ external pull-up resistors to SADD1 and/or SADD2 for proper initialization.

# Hardware Architecture

## DSP1628 Memory Maps

**Table 2. Instruction/Coefficient Memory Maps**

**DSP1628x16**

| X Address | AB[0:15] | MAP 1* EXM = 0 LOWPR = 0† | MAP 2 EXM = 1 LOWPR = 0 | MAP 3‡ EXM = 0 LOWPR = 1 | MAP 4 EXM = 1 LOWPR = 1 |
|---|---|---|---|---|---|
| 0 | 0x0000 | IROM (48K) | EROM (48K) | DPRAM (16K) | DPRAM (16K) |
| 4K | 0x1000 | | | | |
| 8K | 0x2000 | | | | |
| 12K | 0x3000 | | | | |
| 16K | 0x4000 | | | IROM (48K) | EROM (48K) |
| 20K | 0x5000 | | | | |
| 24K | 0x6000 | | | | |
| 28K | 0x7000 | | | | |
| 32K | 0x8000 | | | | |
| 36K | 0x9000 | | | | |
| 40K | 0xA000 | | | | |
| 44K | 0xB000 | | | | |
| 48K | 0xC000 | DPRAM (16K) | DPRAM (16K) | | |
| 52K | 0xD000 | | | | |
| 54K | 0xD800 | | | | |
| 56K | 0xE000 | | | | |
| 60K—64K | 0xFFFF | | | | |

**DSP1628x08**

| X Address | AB[0:15] | MAP 1* EXM = 0 LOWPR = 0† | MAP 2 EXM = 1 LOWPR = 0 | MAP 3‡ EXM = 0 LOWPR = 1 | MAP 4 EXM = 1 LOWPR = 1 |
|---|---|---|---|---|---|
| 0 | 0x0000 | IROM (48K) | EROM (48K) | DPRAM (8K) | DPRAM (8K) |
| 4K | 0x1000 | | | | |
| 8K | 0x2000 | | | Reserved | Reserved |
| 12K | 0x3000 | | | | |
| 16K | 0x4000 | | | IROM (48K) | EROM (48K) |
| 20K | 0x5000 | | | | |
| 24K | 0x6000 | | | | |
| 28K | 0x7000 | | | | |
| 32K | 0x8000 | | | | |
| 36K | 0x9000 | | | | |
| 40K | 0xA000 | | | | |
| 44K | 0xB000 | | | | |
| 48K | 0xC000 | DPRAM (8K) | DPRAM (8K) | | |
| 52K | 0xD000 | | | | |
| 54K | 0xD800 | | | | |
| 56K | 0xE000 | Reserved | Reserved | | |
| 60K—64K | 0xFFFF | | | | |

* MAP1 is set automatically during an HDS trap. The user-selected map is restored at the end of the HDS trap service routine.
† LOWPR is an **alf** register bit. The Lucent Technologies Microelectronics Group development system tools can independently set the memory map.
‡ MAP3 is not available if the secure mask-programmable option is selected.

## Hardware Architecture (continued)

### Table 3. Data Memory Maps

**DSP1628x16 Data Memory Map (not to scale)**

| Decimal Address | Address in r0, r1, r2, r3 | Segment |
|---|---|---|
| 0 | 0x0000 | DPRAM[1:16] |
| 16K | 0x4000 | IO |
| 16,640 | 0x4100 | ERAMLO |
| 32K | 0x8000 | ERAMHI |
| 64K – 1 | 0xFFFF | |

**DSP1628x08 Data Memory Map (not to scale)**

| Decimal Address | Address in r0, r1, r2, r3 | Segment |
|---|---|---|
| 0 | 0x0000 | DPRAM[1:8] |
| 8K | 0x2000 | Reserved |
| 16K | 0x4000 | IO |
| 16,640 | 0x4100 | ERAMLO |
| 32K | 0x8000 | ERAMHI |
| 64K – 1 | 0xFFFF | |

For additional information, contact your Microelectronics Group Account Manager or the following:
INTERNET: **http://www.lucent.com/micro**
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103,
**1-800-372-2447**, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106), e-mail **docmaster@micro.lucent.com**
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
**Tel. (65) 778 8833**, FAX (65) 777 7495
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
**Tel. (81) 3 5421 1600**, FAX (81) 3 5421 1700
For data requests in Europe:
MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148
For technical inquiries in Europe:
CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 1344 865 900** (Bracknell UK),
FRANCE: **(33) 1 47 67 47 67** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)



January 1997
OT97-129WDSP