QUAD, 16-BIT, LOW-POWER, VOLTAGE OUTPUT W/I^{2}C INTERFACE DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **MicroPower Operation: 950 µA at 5 V V_{DD}**
- **Power-On Reset to Zero**
- **+2.7 V to +5.5 V Analog Power Supply**
- **Specified Monotonic by Design**
- **Settling Time: 10µs to ±0.003% FSR**
- **I^{2}C™ Interface Up to 3.4 Mbps**
- **Data Transmit Capability**
- **On-Chip Output Buffer Amplifier, Rail-to-Rail Operation**
- **Double-Buffered Input Register**
- **Address Support for up to Sixteen DAC8574's**
- **Synchronous Update Support for up to 64 Channels**
- **Operation From -40°C to 105°C**
- **Small 16 Lead TSSOP Package**

APPLICATIONS

- **Process Control**
- **Data Acquistion Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Portable Instrumentation**

DESCRIPTION

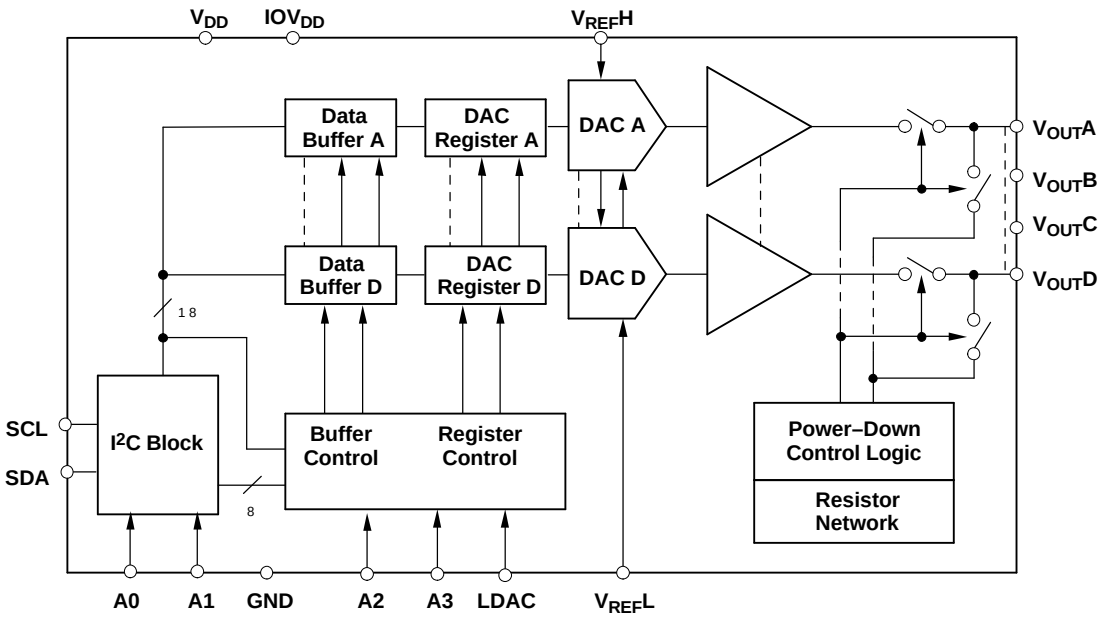
The DAC8574 is a low-power, quad channel, 16-bit buffered voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC8574 utilizes an I^{2}C compatible two wire serial interface supporting high-speed interface mode with address support of up to sixteen DAC8574's for a total of 64 channels on the bus.

The DAC8574 requires an external reference voltage to set the output range of the DAC. The DAC8574 incorporates a power-on-reset circuit that ensures that the DAC output powers up at zero volts and remains there until a valid write takes place to the device. The DAC8574 contains a power-down feature, accessed via the internal control register, that reduces the current consumption of the device to 200nA at 5V.

The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The power consumption is less than 5mW at V_{DD}=5V reducing to 1µW in power-down mode.

The DAC8574 is available in an 16-lead TSSOP package.

I²C is a trademark of Philips Corporation.


VDD
IOVDD
VREFH
Data Buffer A
DAC Register A
DAC A
Data Buffer D
DAC Register D
DAC D
VOUTA
VOUTB
VOUTC
VOUTD
18
SCL
SDA
I2C Block
8
Buffer Control
Register Control
Power–Down Control Logic
Resistor Network
A0
A1
GND
A2
A3
LDAC
VREFL

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC8574	16-TSSOP	PW	-40°C to +105°C	D8574I	DAC8574IPW	90 Piece Tube
					DAC8574PWR	2000 Piece Tape and Reel

ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to GND	-0.3V to +6V
Digital input voltage to GND	-0.3V to V_{DD} + 0.3V
V_{OUT} to GND	0.3V to V_{DD} + 0.3V
Operating temperature range	40°C to +105°C
Storage temperature range	65°C to +150°C
Junction temperature range (T_J max)	+150°C
Power dissipation:	
Thermal impedance (ΘJA)	118°C/W
Thermal impedance (ΘJC)	29°C/W
Lead temperature, soldering:	
Vapor phase (60s)	215°C
Infrared (15s)	220°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, R_L = 2kΩ to GND; C_L = 200pF to GND; all specifications -40°C to +105°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (1)					
Resolution		16			Bits
Relative accuracy				± 0.0987	% of FSR
Differential nonlinearity	Assured monotonic by design			± 1	LSB
Zero-code error	All zeroes loaded to DAC register		5	20	mV
Full-scale error	All ones loaded to DAC register		-0.15	-1.0	% of FSR
Gain error				± 1.0	% of FSR
Zero code error erift			±7		µV/°C
Gain temperature coefficient			± 3		ppm of FSR/°C
PSRR	V_{DD}=5V		0.75		mV/V
OUTPUT CHARACTERISTICS (2)					
Output voltage range		0		V_{REF}H	V
Output voltage settling time (full scale)	R_L=2 kΩ; 0 pF < C_L < 200 pF		8	10	µs
	R_L=2kΩ ; C_L=500 pF		12		µs

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7V to 5.5V, R_L = 2kΩ to GND; C_L = 200pF to GND; all specifications -40°C to +105°C, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Slew rate			1		V/µs
DC crosstalk			0.25		LSB
AC drosstalk	1 kHz Sine Wave		-100	-96	dB
Capacitive load stability	R_L=∞		470		pF
	R_L=2kΩ		1000		pF
Digital-to-analog glitch impulse	1 LSB change around major carry		20		nV-s
Digital feedthrough			0.5		nV-s
DC output impedance			1		Ω
Short-circuit current	V_{DD}=5V		50		mA
	V_{DD}=3V		20		mA
Power-up time	Coming out of power-down mode, V_{DD}=+5V		2.5		µs
	Coming out of power-down mode, V_{DD}=+3V		5		µs
REFERENCE INPUT					
V_{REFH} Input range		0		V_{DD}	V
V_{REFL}Iput range	V_{REFL} < V_{REFH}	0	GND	V_{DD}	V
Reference input impedance			35		kΩ
Reference current	V_{REF}=V_{DD}=+5V		135	180	µA
	V_{REF}=V_{DD}=+3V		80	120	
LOGIC INPUTS (3)					
Input current				± 1	µA
V_{IN_L}, Input low voltage				0.3xIOV_{DD}	V
V_{IN_H}, Input high voltage	V_{DD}=3V	0.7xIOV_{D} D			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}IOV_{DD}		2.7		5.5	V
I_{DD}(normal operation)	DAC active and excluding load current				
AI_{DD}@ V_{DD}=+3.6V to +5.5V	V_{IH}=IO$V_{DD}$and V_{IL}=GND		950	1600	µA
AI_{DD}@ V_{DD}=+2.7V to +3.6V	V_{IH}=IO$V_{DD}$and V_{IL}=GND		900	1500	µA
I_{DD} (all power-down modes)					
V_{DD}=+3.6V to +5.5V	V_{IH}=IO$V_{DD}$and IOV_{IL}=GND		0.2	1	µA
AI_{DD}=+2.7V to +3.6V	V_{IH}=$V_{DD}$and V_{IL}=GND		0.05	1	µA
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD}=2mA, V_{DD}=+5V		93%		
TEMPERATURE RANGE					
Specified performance		-40		+105	°C

(3) Ensured by design and characterization, not production tested.

TIMING CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, R_L = 2kΩ to GND; all specifications -40°C to +105°C, unless otherwise specified.

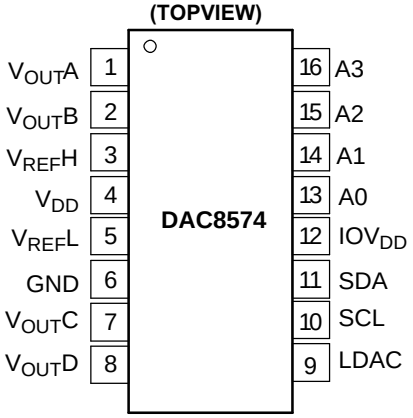
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCL}	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High-Speed Mode, C_B=100pF max			3.4	MHz
		High-speed mode, C_B=400pF max			1.7	MHz
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HD}; t_{STA}	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode	160			ns
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			µs
		High-speed mode, C_B=100pF max	160			ns
		High-speed mode, C_B=400pF max	320			ns
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	600			ns
		High-Speed Mode, C_B=100pF max	60			ns
		High-speed mode, C_B=400pF max	120			ns
t_{SU}; t_{STA}	Setup time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	600			ns
		High-speed mode	160			ns
t_{SU}; t_{DAT}	Data setup time	Standard mode	250			ns
		Fast mode	100			ns
		High-speed mode	10			ns
t_{HD}; t_{DAT}	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		High-speed mode, C_B=100pF max	0		70	ns
		High-speed mode, C_B=400pF max	0		150	ns
t_{RCL}	Rise time of SCL signal	Standard mode	$20 \times 0.1C_B$		1000	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B=100pF max	10		40	ns
		High-speed mode, C_B=400pF max	20		80	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	Standard mode	$20 \times 0.1C_B$		1000	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B=100pF max	10		80	ns
		High-speed mode, C_B=400pF max	20		160	ns
t_{FCL}	Fall time of SCL signal	Standard mode	$20 \times 0.1C_B$		300	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B=100pF max	10		40	ns
		High-speed mode, C_B=400pF max	20		80	ns
t_{RDA}	Rise time of SDA signal	Standard mode	$20 \times 0.1C_B$		1000	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B=100pF max	10		80	ns
		High-speed mode, C_B=400pF max	20		160	ns

TIMING CHARACTERISTICS (continued)

V_{DD} = 2.7V to 5.5V, R_L = 2kΩ to GND; all specifications -40°C to +105°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{FDA}	Fall time of SDA signal	Standard mode	$20 \times 0.1C_B$		300	ns
		Fast mode	$20 \times 0.1C_B$		300	ns
		High-speed mode, C_B=100pF max	10		80	ns
		High-speed mode, C_B=400pF max	20		160	ns
t_{SU}; t_{STO}	Setup time for STOP condition	Standard mode	4.0			µs
		Fast mode	600			ns
		High-speed mode	160			ns
C_B	Capacitive load for SDA and SCL				400	pF
t_{SP}	Pulse width of spike suppressed	Fast mode			50	ns
		High-speed mode			10	ns
V_{NH}	Noise margin at the HIGH level for each connected device (including hysteresis)	Standard mode	$0.2V_{DD}$			V
		Fast mode				
		High-speed mode				
V_{NL}	Noise margin at the LOW level for each connected device (including hysteresis)	Standard mode	$0.1V_{DD}$			V
		Fast mode				
		High-speed mode				

PW PACKAGE
(TOPVIEW)



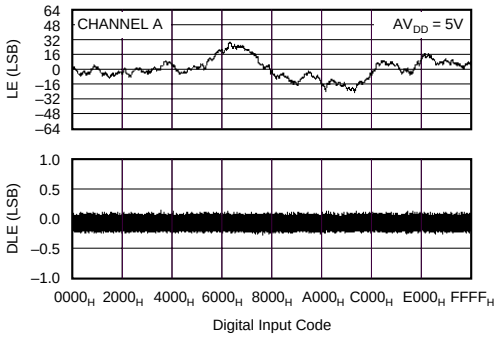
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$V_{OUT}A$	Analog output voltage from DAC A
2	$V_{OUT}B$	Analog output voltage from DAC B
3	$V_{REF}H$	Positive reference voltage input
4	V_{DD}	Analog voltage supply input
5	$V_{REF}L$	Negative reference voltage input
6	GND	Ground reference point for all circuitry on the part
7	$V_{OUT}C$	Analog output voltage from DAC C
8	$V_{OUT}D$	Analog output voltage from DAC D
9	LDAC	H/W synchronous V_{OUT} update
10	SCL	Serial clock input
11	SDA	Serial data input
12	IOV_{DD}	I/O voltage supply input
13	A0	Device address select - I^2C
14	A1	Device address select - I^2
15	A2	Device address select - Extended
16	A3	Device address select - Extended

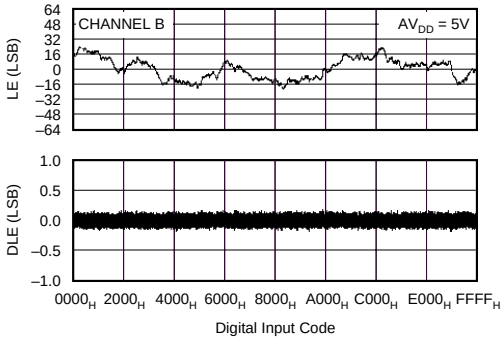
TYPICAL CHARACTERISTICS

At TA = +25°C, unless otherwise noted.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



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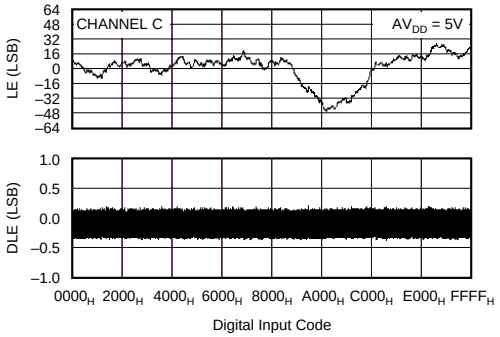
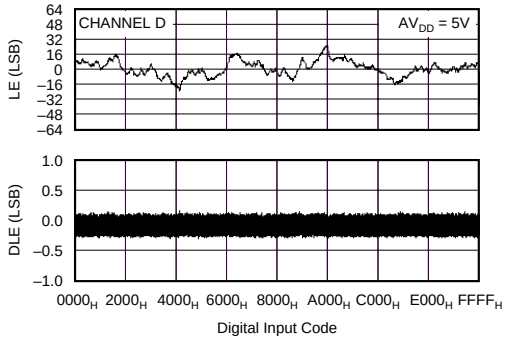
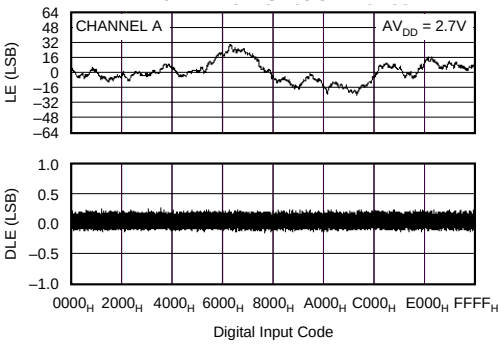


LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



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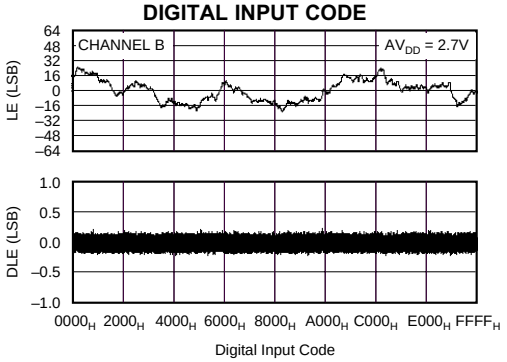

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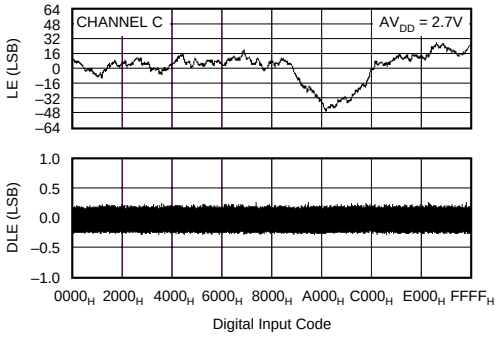
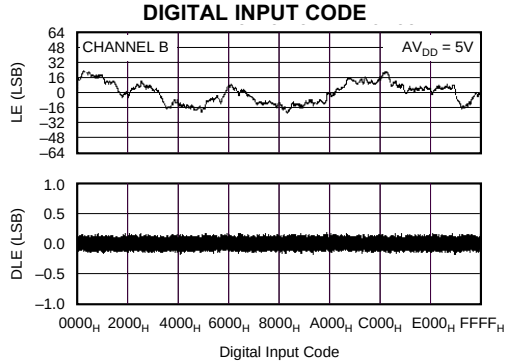
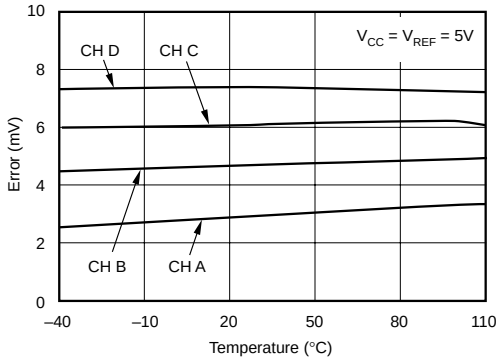


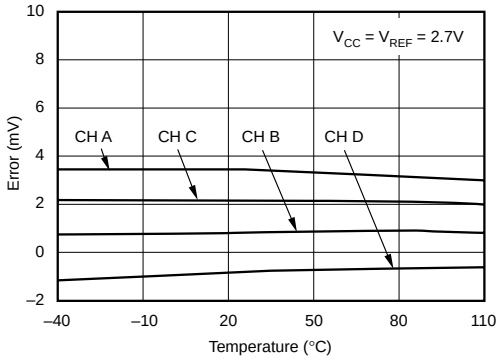
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



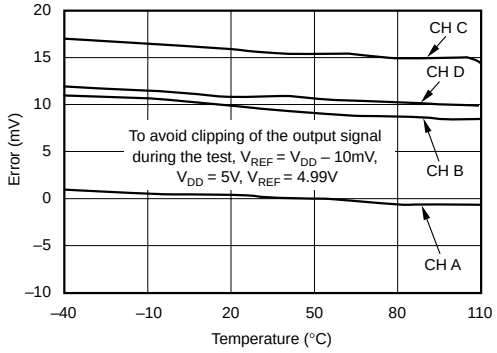
ZERO-SCALE ERROR vs TEMPERATURE



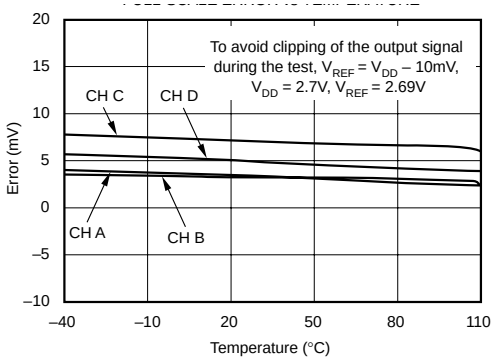
ZERO-SCALE ERROR vs TEMPERATURE



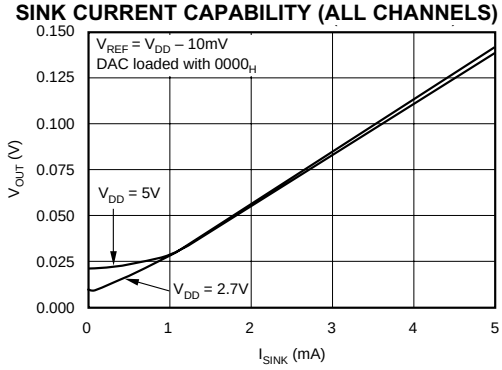
FULL-SCALE ERROR vs TEMPERATURE



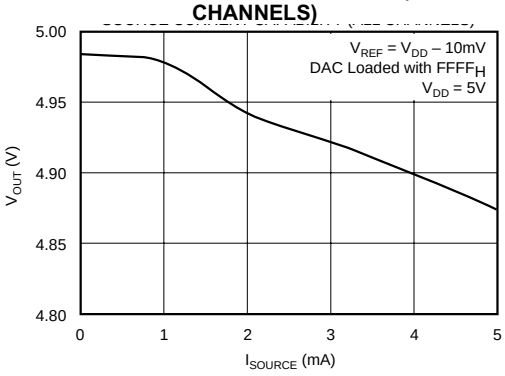
FULL-SCALE ERROR vs TEMPERATURE



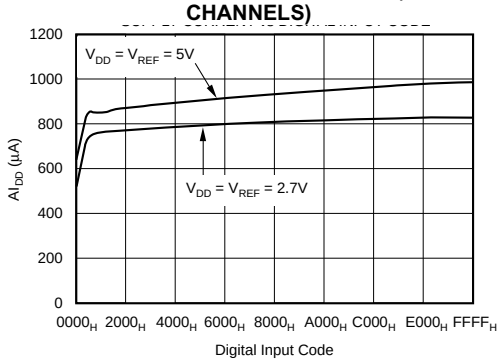
SINK CURRENT CAPABILITY (ALL CHANNELS)



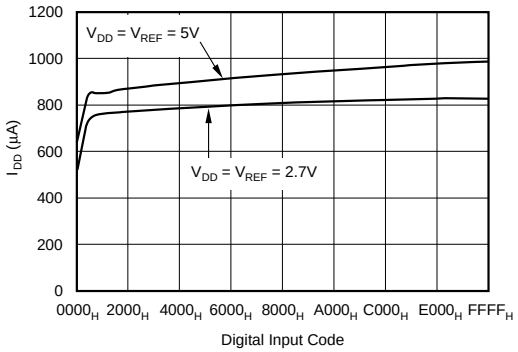
SOURCE CURRENT CAPABILITY (ALL CHANNELS)



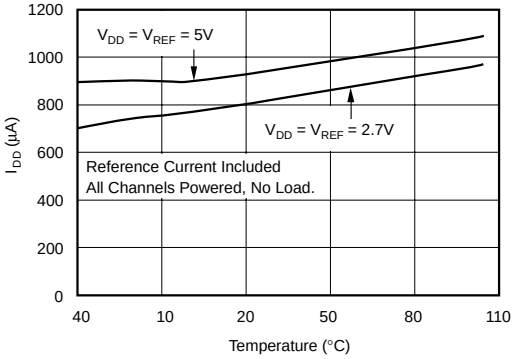
SOURCE CURRENT CAPABILITY (ALL CHANNELS)



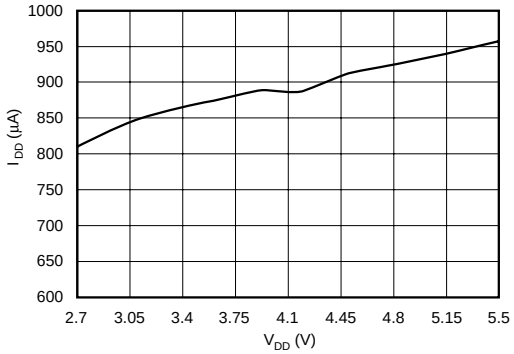
SUPPLY CURRENT vs DIGITAL INPUT CODE



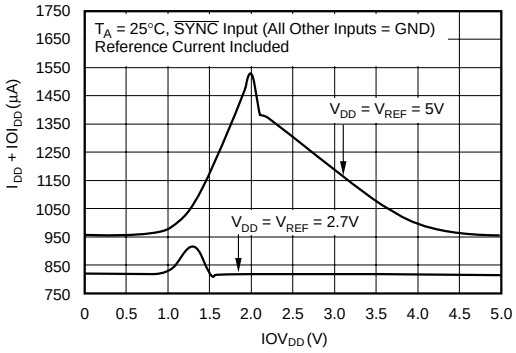
SUPPLY CURRENT vs TEMPERATURE



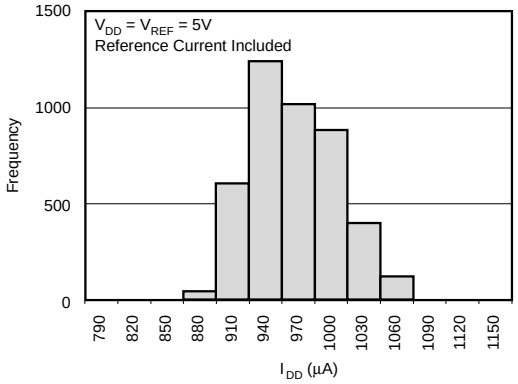
SUPPLY CURRENT vs SUPPLY VOLTAGE



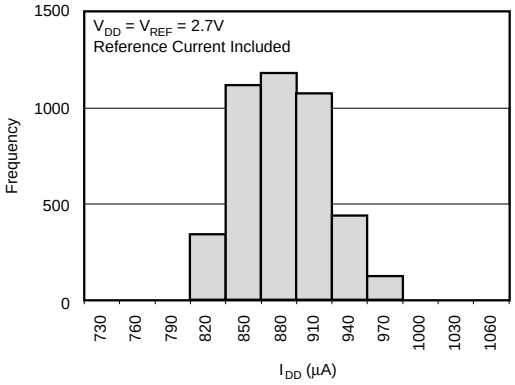
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



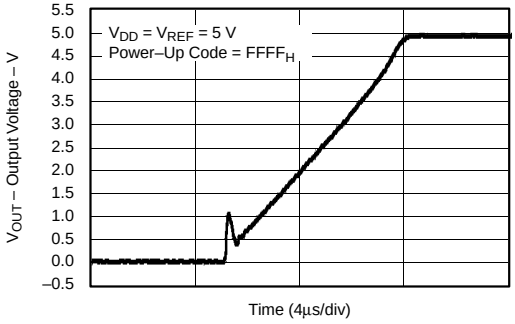
HISTOGRAM OF CURRENT CONSUMPTION



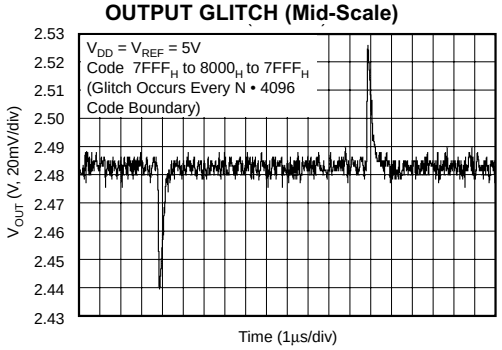
HISTOGRAM OF CURRENT CONSUMPTION



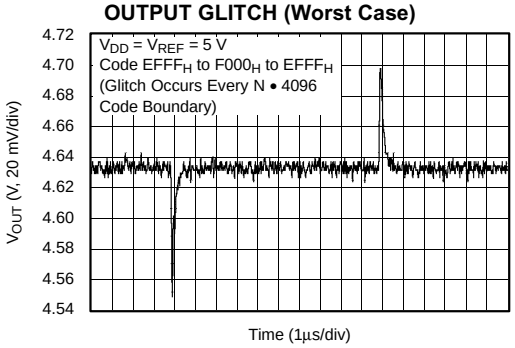
EXITING POWER-DOWN MODE



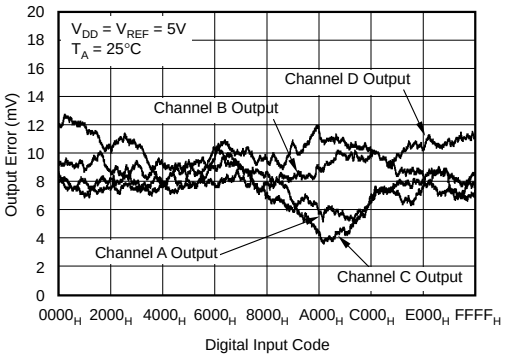
OUTPUT GLITCH (Mid-Scale)



OUTPUT GLITCH (Worst Case)



ABSOLUTE ERROR



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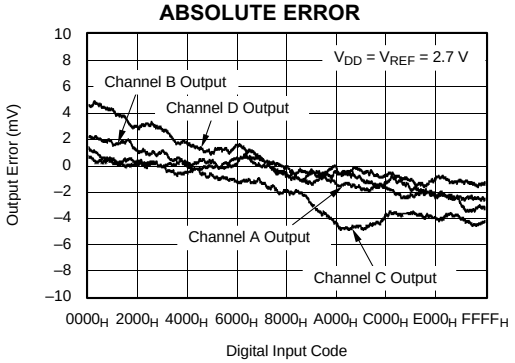
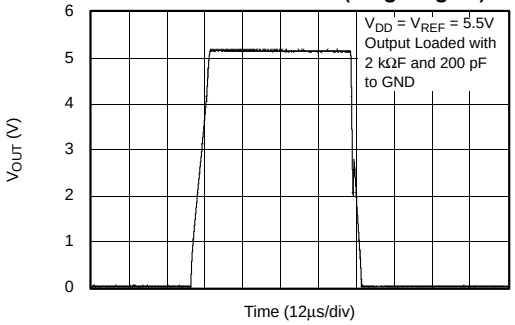
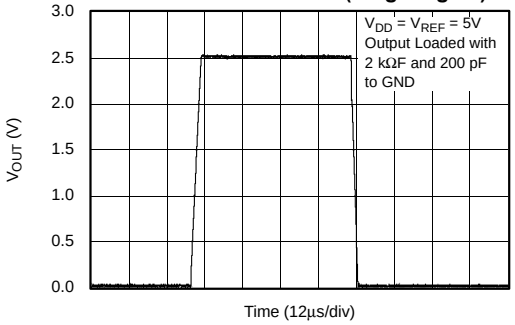


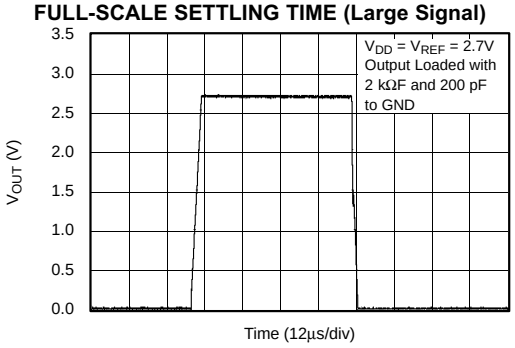
FULL-SCALE SETTLING TIME (Large Signal)



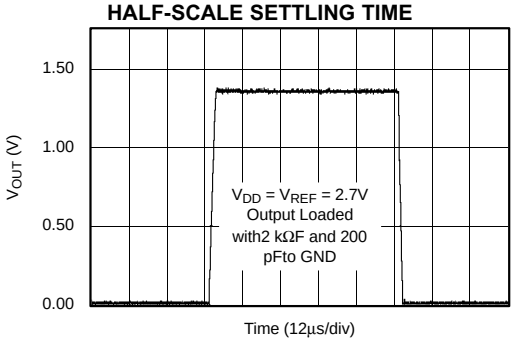
HALF-SCALE SETTLING TIME (Large Signal)



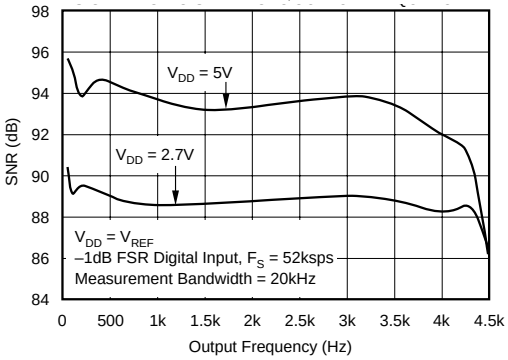
FULL-SCALE SETTLING TIME (Large Signal)



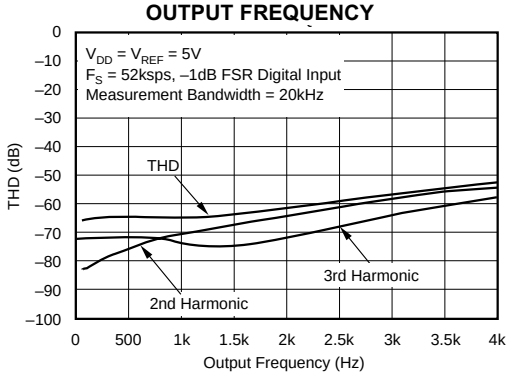
HALF-SCALE SETTLING TIME



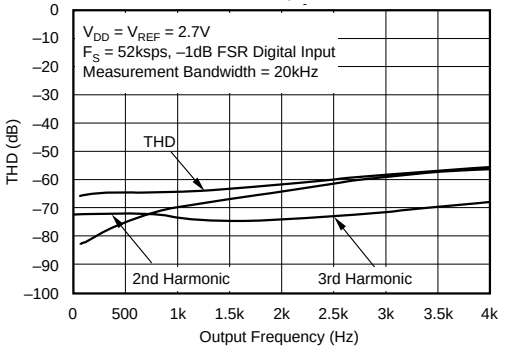
SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY



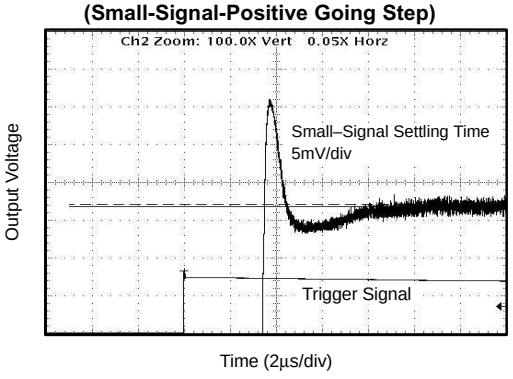
TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY



TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY



FULL-SCALE SETTLING TIME (Small-Signal-Positive Going Step)



FULL-SCALE SETTLING TIME (Small-Signal-Negative Going Step)

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC8574 consists of a string DAC followed by an output buffer amplifier. Figure 1 shows a generalized block diagram of the DAC architecture.

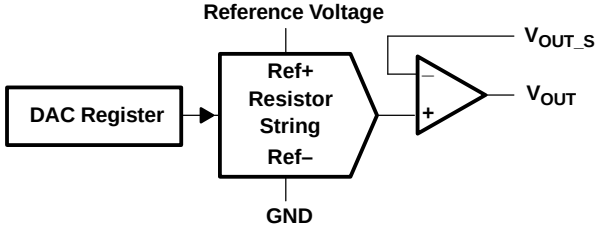


Figure 1. R-String DAC Architecture

The input coding to the DAC8574 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = V_{REF}L + (V_{REF} - V_{REF}L) \times \frac{D}{65536}$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 2. It is basically a divide-by-2 resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Because the architecture consists of a string of resistors, it is specified monotonic.

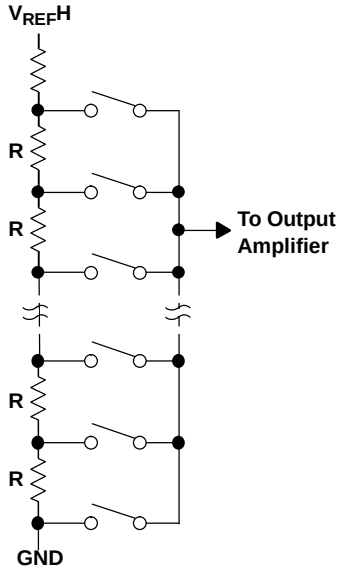


Figure 2. Typical Resistor String

OUTPUT AMPLIFIER

The output buffer is a gain-of-2 noninverting amplifiers, capable of generating rail-to-rail voltages on its output, which gives an output range of 0V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/μs with a half-scale settling time of 8 μs with the output unloaded.

I²C INTERFACE

The DAC8574 supports the I²C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed 10-bit addressing, and general call address are not supported. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DAC8574 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The bus should include pullup devices.

The following bus protocol has been defined (as shown in Figure 5):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

- Bus Not Busy: Both data and clock lines remain HIGH.
- Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- Data Valid: The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit. Within the I²C bus specifications a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are defined. The DAC8574 works in all three modes.
- Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition. Figure 2 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/W bit (see Figure 5), two types of data transfer are possible:
  - Data transfer from a master transmitter to a slave receiver. DAC8574 supports 7-bit I²C addressing. The first byte transmitted by the master is the 7-bit slave address followed by the R/$\overline{W}$ bit=0. Next follows a number of data bytes. The slave returns an acknowledge, if addressed after the slave address and each received byte.
  - Data transfer from a slave transmitter to a master receiver. The first byte, the 7-bit slave address and R/$\overline{W}$ bit=1, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. The DAC8574 may operate in the following two modes:
    - Slave Receiver Mode: Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (R/$\overline{W}$=0).
    - Slave Transmitter Mode: The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit (R/$\overline{W}$=1) indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the DAC8574 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

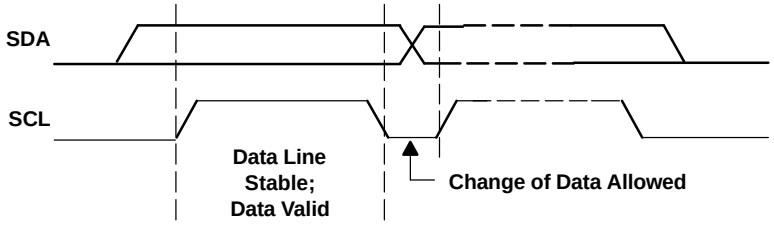


Figure 3. Bit Transfer on the I^2C Bus

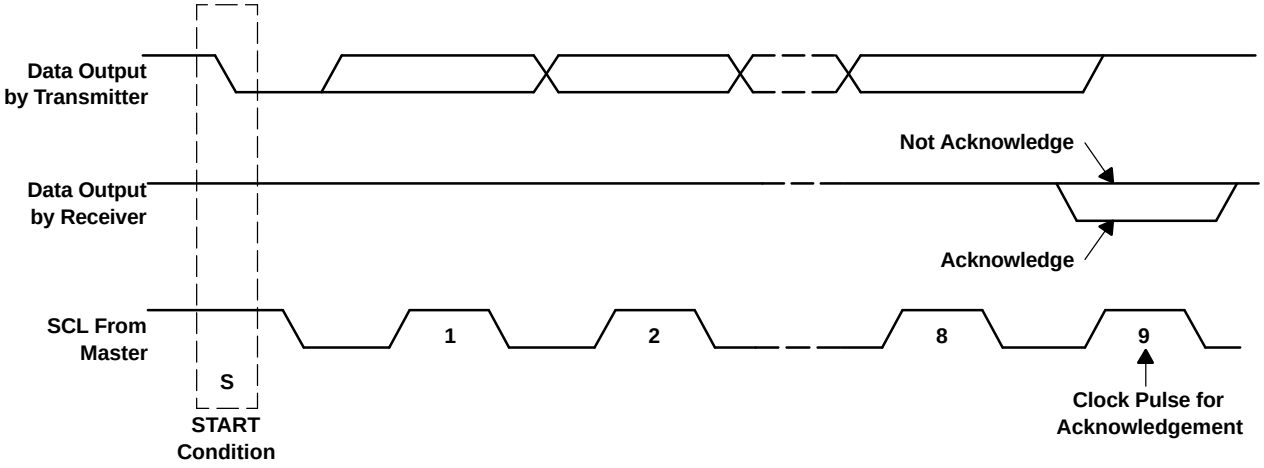


Figure 4. Acknowledge on the I^2C Bus

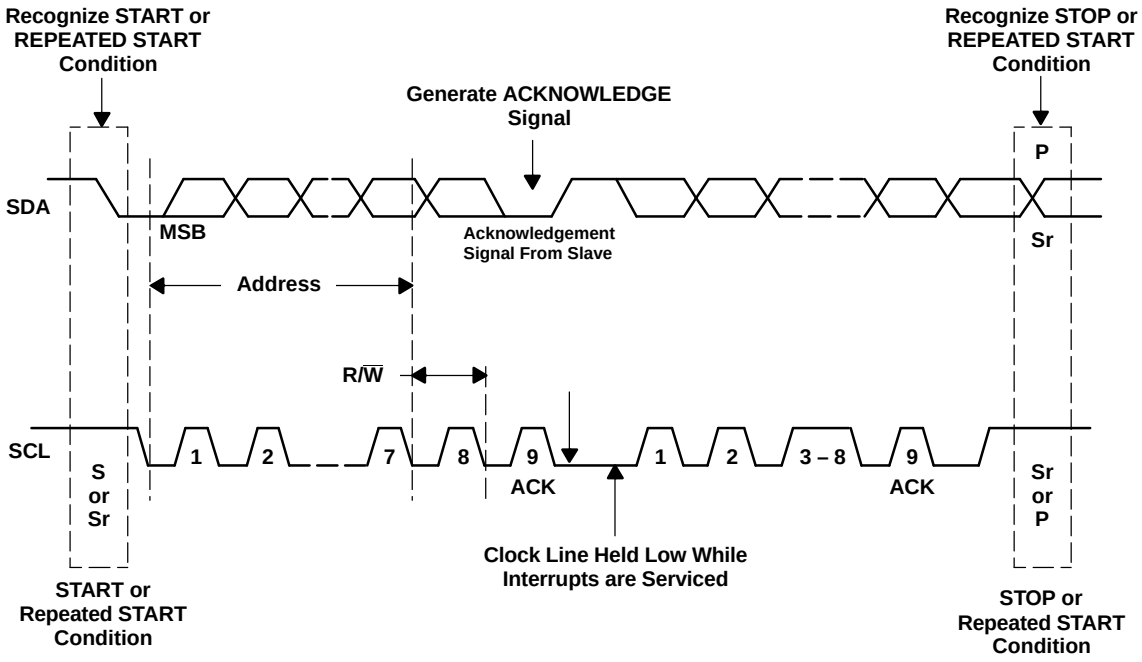
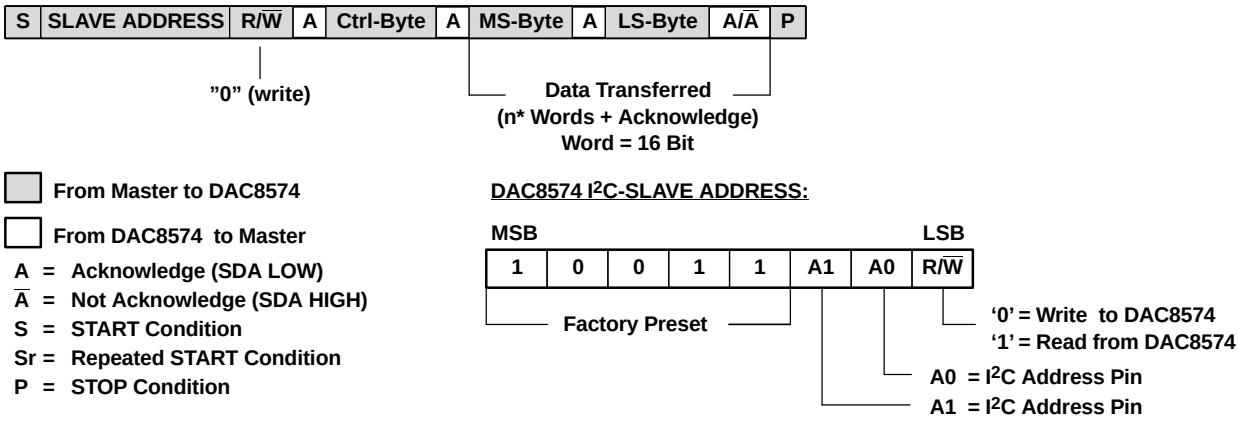
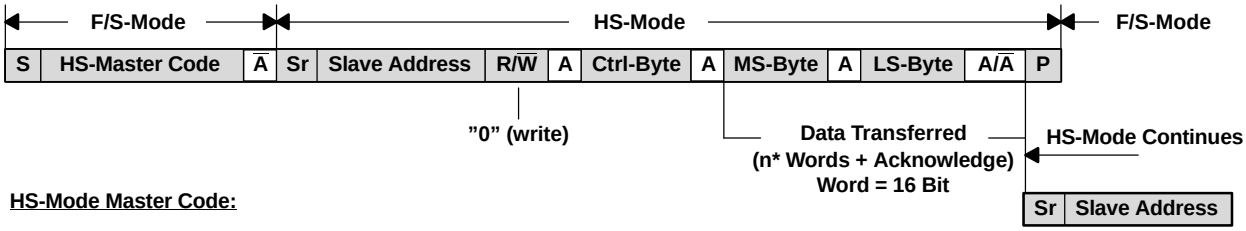


Figure 5. Bus Protocol

Standard-and Fast-Mode:



High-Speed-Mode (HS-Mode):



HS-Mode Master Code:

MSB							LSB
0	0	0	0	1	X	X	R/W

MS-Byte:

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

LS-Byte:

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

D15 – D0 = Data Bits

Control Byte:

MSB							LSB
A3	A2	L1	L0	X	Sel1	Sel2	PD0

A3 = Extended Address Bit
A2 = Extended Address Bit
L1 = Load1 (Mode Select) Bit
L0 = Load0 (Mode Select) Bit
Sel1 = Buff Sel1 (Channel) Select Bit
Sel0 = Buff Sel0 (Channel) Select Bit
PD0 = Power Down Flag

Figure 6. Master Transmitter Addressing DAC8574 as a Salve Receiver with a 7-Bit Address

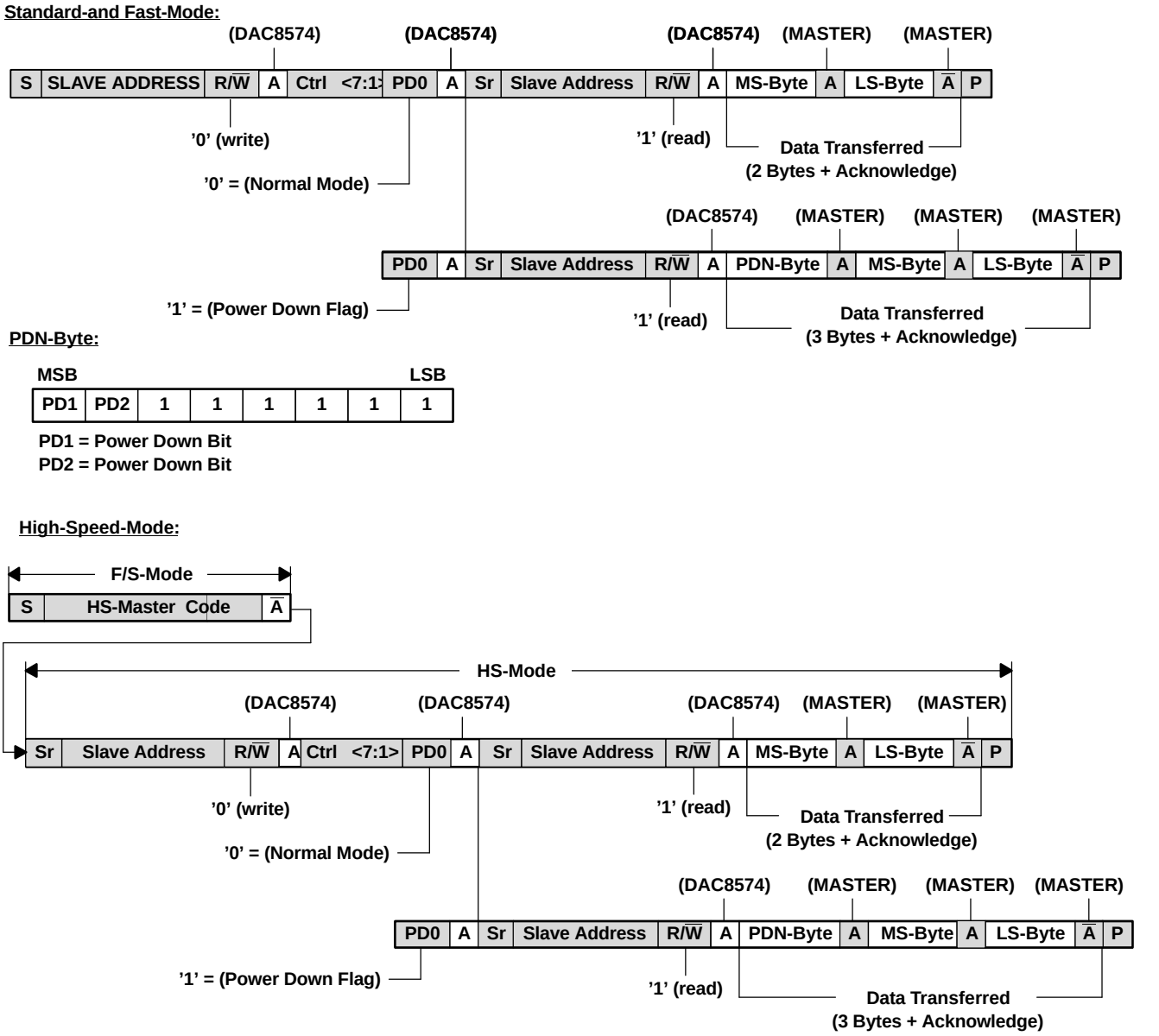


Figure 7. Master Addressing DAC8574 as a Slave Transmitter with a 7-Bit Address

Write Sequence - Data Input (continued)

WRITE SEQUENCE - DATA INPUT

Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master	Start								Begin sequence (1)
Master	1	0	0	1	1	A1	A0	R/$\overline{W}$	Write addressing (R/$\overline{W}$=0)
DAC8574	DAC8574 Acknowledges								
Master	A3	A2	Load 1	Load 0	x	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=0)
DAC8574	DAC8574 Acknowledges								
Master	D15	D14	D13	D12	D11	D10	D9	D8	Writing data word, high byte
DAC8574	DAC8574 Acknowledges								
Master	D7	D6	D5	D4	D3	D2	D1	D0	Writing data word, low byte
DAC8574	DAC8574 Acknowledges								
Master	Stop or Repeated Start (2)								Done

(1) Once DAC8574 is properly addresed and control byte is sent, high-byte-low-byte sequences can repeat until a stop condition is recieved.
(2) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

WRITE SEQUENCE - POWER DOWN MODE

Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master	Start								Begin sequence
Master	1	0	0	1	1	A1	A0	R/$\overline{W}$	Write addressing (R/$\overline{W}$=0)
DAC8574	DAC8574 Acknowledges								
Master	A3	A2	Load 1	Load 0	x	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=1)
DAC8574	DAC8574 Acknowledges								
Master	PD1	PD2	0	0	0	0	0	0	Writing data word, high byte
DAC8574	DAC8574 Acknowledges								
Master	0	0	0	0	0	0	0	0	Writing data word, low byte
DAC8574	DAC8574 Acknowledges								
Master	Stop or Repeated Start (2)								Done

Read Sequence - Data Registers (continued)

READ SEQUENCE - DATA REGISTERS

Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master	Start								Begin sequence
Master	1	0	0	1	1	A1	A0	0	Write addressing (R/$\overline{W}$=0)
DAC8574	DAC8574 Acknowledges								
Master	A3	A2	Load 1	Load 0	x	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=0)
DAC8574	DAC8574 Acknowledges								
Master	Repeated Start								
Master	1	0	0	1	1	A1	A0	1	Read addressing (R/$\overline{W}$=1)
DAC8574	DAC8574 Acknowledges								
DAC8574	D15	D14	D13	D12	D11	D10	D9	D8	Reading data word, high byte
Master	Master Acknowledges								
DAC8574	D7	D6	D5	D4	D3	D2	D1	D0	Reading data word, low byte
Master	Master Not Acknowledges								Master signal end of read
Master	Stop or Repeated Start (1)								Done

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for next Write.

READ SEQUENCE - POWER DOWN REGISTERS

Transmitter	MSB	6	5	4	3	2	1	LSB	Comment
Master	Start								Begin sequence
Master	1	0	0	1	1	A1	A0	0	Write addressing (R/$\overline{W}$=0)
DAC8574	DAC8574 Acknowledges								
Master	A3	A2	Load 1	Load 0	x	Buff Sel 1	Buff Sel 0	PD0	Control byte (PD0=1)
DAC8574	DAC8574 Acknowledges								
Master	Repeated Start								
Master	1	0	0	1	1	A1	A0	1	Read addressing (R/$\overline{W}$=1)
DAC8574	DAC8574 Acknowledges								
DAC8574	PD1	PD2	1	1	1	1	1	1	Read power down byte
Master	Master Acknowledges								
DAC8574	D15	D14	D13	D12	D11	D10	D9	D8	Reading data word, high byte
Master	Master Acknowledges								
DAC8574	D7	D6	D5	D4	D3	D2	D1	D0	Feading data word, low byte
Master	Master Not Acknowledges								Master sgnal end of read
Master	Stop or Repeated Start (1)								Done

(1) Use repeated start to secure bus operation and loop back to the stage of write addressing for nextWrite.

I^2C UPDATE SEQUENCE

DAC8574 requires a start condition, a valid I^2C address, a control byte, an MSB byte and an LSB byte for a single update. After the receipt of each byte, DAC8574 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^2C address selects the DAC8574. The control byte sets the operational mode of the selected DAC8574. Once the operational mode is selected by the control byte, DAC8574 expects an MSB byte followed by an LSB byte for data update to occur. DAC8574 performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

Control byte needs not to be resent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, DAC8574 requires a start condition, a valid I^2C address, a control byte, an MSB byte and an LSB byte. For all consecutive updates, DAC8574 needs an MSB byte and an LSB byte as long as the control command remains the same.

Using the I^2C high-speed mode (f_{scl}= 3.4 MHz), the clock running at 3.4MHz, each 16-bit DAC update other than the first update can be done within 18 clock cycles (MSB byte, acknowledge signal, LSB byte, acknowledge signal), at 188.88 KSPS. Using the fast mode (f_{scl}= 400 kHz), clock running at 400KHz, maximum DAC update rate is limited to 22.22 KSPS.

Once a stop condition is received DAC8574 releases the I^2C bus and awaits a new start condition.

Address Byte

MSB							LSB	
1	0	0	1	1	A1	A0	R/$\overline{W}$	

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory preset to 10011. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the DAC8574 determine these two bits of the device address for a particular DAC8574. A maximum of four devices with the same preset code can therefore be connected on the same bus at one time with different I^2C addresses (up to 16 DAC8574 devices can still be connected to the same I^2C bus as is explained). The A1-A0 Address Inputs can be connected to VDD or digital ground, or can be actively driven by TTL or CMOS logic levels. The device address is set by the state of these pins upon power-up of the DAC8574.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a 1 a read operation is selected (master device reads from DAC8574); when set to a 0 a write operation is selected (master device writes to DAC8574). Following the START condition the DAC8574 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10011 code, the appropriate device select bits (A1–A0), and the R/$\overline{W}$ bit, the DAC8574 outputs an acknowledge signal on the SDA line.

Broadcast addressing is also supported by DAC8574. Broadcast addressing can be used for synchronously updating or powering down multiple DAC8574 devices. DAC8574 is designed to work with other members of DAC857X DAC757X families to support multichannel synchronous update. When the broadcast address is used, DAC8574 responds regardless of the states of the A0 and A1 pins. Broadcast address is as follows. Broadcast is only supported in Write Mode (Master writes to DAC8574).

MSB							LSB	
1	0	0	1	0	0	0	0	

Control Byte

After transmitting an acknowledge pulse following a valid address, DAC8574 expects a control byte C<7:0>.

The first two MSBs C<7> and C<6> are extended address matching bits. The state of these bits must match the state of pins A3 and A2 in order the DAC8574 to update.

Broadcast modes override extended address matching requirement.

C<5> and C<4> are used for setting the update mode.

C<5>=0, C<4>=0: Store I^2C data. The contents of MSB byte and LSB byte data (or power-down information) are stored in the temporary register of a selected channel. This mode does not change the DAC output of the selected channel.

C<5>=0, C<4>=1: Update selected DAC with I^2C data. Most commonly utilized mode. The contents of MSB byte and LSB byte data (or power-down information) are stored in the temporary data register and into the DAC register of the selected channel. This mode changes the DAC output of the selected channel with the contents of I^2C MSB byte and LSB byte data.

C<5>=1, C<4>=0: 4-channel synchronous update. The contents of MSB byte and LSB byte data (or powerdown information) update the temporary register and the DAC register of the selected channel. Simultaneously, the other three DACs get updated with previously stored temporary register data. This mode updates all four DACs together.

C<5>=1, C<4>=1: Broadcast update. This mode has two functions. If C<2> = 0, all four DACs are updated with the contents of their temporary register data, I^2C MSB and LSB bytes are ignored. If C<2> = 1, all four DACs are updated with I^2C MSB byte and LSB byte data. In broadcast modes, DAC8574 responds regardless of local address matching and channel selection becomes irrelevant as all channels update. This mode is intended to enable up to 64 channel simultaneous update, if used with the I^2C broadcast address (10010000).

C<3> should always be zero.

C<2> and C<1>: Channel select bits. They select one out of 4 channels. C<2,1> = 00…11 select DAC channels A … D respectively. (In broadcast mode channel selection becomes irrelevant, so C<2> is assigned a different purpose as explained above).

C<0> should be zero during normal DAC operation. C<0> = 1 is a power-down flag. If C<0> = 1, MSB<7>, MSB<6> indicate a power-down operation as shown in (Temp TBL5)Table 1.

Table 1. (Temp Tbl5) Control Byte.

C7	C6	C5	C4	C3	C2	C1	C0	MSB7	MSB6	MSB5..	DESCRIPTION
A3	A2	Load1	Load0	Don't Care	Ch Sel 1	Ch Sel 0	PD0	MSB (PD1)	MSB-1 (PD2)	MSB-2 ...LSB	
(Address Select)											
(A3 and A2 should correspond to the package address set via pins A3 and A2.)		0	0	X	0	0	0	Data			Write to temporary register A (TRA) with data
		0	0	X	0	1	0	Data			Write to temporary register B (TRB) with data
		0	0	X	1	0	0	Data			Write to temporary register C (TRC) with data
		0	0	X	1	1	0	Data			Write to temporary register D (TRD) with data
		0	0	X	(00, 01, 10, or 11)		1	see (Temp Tbl 7)		0	Write to TRx (selected C<2> &C<1> w/Powerdown Command
		0	1	X	(00, 01, 10, or 11)		0	Data			Write to TRx (selected C<2> &C<1> and load DACx w/ data
		0	1	X	(00, 01, 10, or 11)		1	see (Temp Tbl 7)		0	Powerdown DACx (selected by C<2> and C<1>)
		1	0	X	(00, 01, 10, or 11)		0	Data			Write to TRx (selected C<2> &C<1> w/ data and load all DACs
		1	0	X	(00, 01, 10, or 11)		1	see (Temp Tbl 7)		0	Powerdown DACx (selected by C<2> and C<1>) & load all DACs
BROADCAST MODES (CONTROLS UP TO 4 DEVICES ON A SINGLE SERIAL BUS)											
X	X	1	1	X	0	X	X	X			Update all DACs, all devices with previously stored TRx data
X	X	1	1	X	1	X	0	Data			Update all DACs, all devices with MSB<7:0> and LSB<7:0> data
X	X	1	1	X	1	X	1	see (Temp Tbl 7)		0	Powerdown all DACs, all devices

Most Significant Byte

Most Significant Byte MSB<7:0> consists of eight most significant bits of 16-bit unsigned binary D/A conversion data. When C<0>=1, MSB<7>, MSB<6> indicate a powerdown operation as shown in Table TBD.

Least Significant Byte

Least Significant Byte LSB<7:0> consists of the 8 least significant bits of the 16bit unsigned binary D/A conversion data. DAC8574 updates at the falling edge of the acknowledge signal that follows the LSB<0> bit.

DATA TRANSMIT AND READBACK

The I^2C bus can be noisy and data integrity can be a problem in a system of many I^2C devices, especially in high-speed mode. To enable I^2C system verification, DAC8574 provides read back capability to the user. During read back operation, a particular channel can be selected and the power-down data, MSB byte and the LSB byte could be transmitted back to the master device using the I^2C bus. This read-back function can also be useful if a device on the I^2C bus inquires the status of a DAC8574 channel.

For read-back operation, the master device sends the I^2C address with R/$\overline{W}$=0. DAC8574 acknowledges. The master then sends a control byte with the sole purpose of channel selection. DAC8574 acknowledges. Master sends a repeated start condition followed by the address byte with R/$\overline{W}$=1. DAC8574 acknowledges. Then, upon the receipt of further clock pulses from the master, DAC8574 sends the powerdown data for the selected channel. If the master acknowledges, DAC8574 sends the MSB byte for the selected channel. If the master acknowledges, DAC8574 sends the LSB byte. This read-back sequence can be terminated by the master sending a not acknowledge signal.

LDAC FUNCTIONALITY

The LDAC pin is required only when an external timing signal is used to update the DACs. LDAC is a positive edge triggered asynchronous input that allows four DAC output voltages to be updated simultaneously with temporary register data. The LDAC trigger should only be used after the buffers temporary registers are properly updated through software.

DAC8574 REGISTERS

Following registers are utilized in the DAC8574 architecture:

ADDRESS<7:0>
Stores 8 bit I^2C address sent by the master

C<7:0>
Stores 8 bit control command sent by the master

MSB<7:0>
Stores the 8 most significant bits of unsigned binary data sent by the master. Can also store 2-bit power-down data.

LSB<7:0>
Stores the 8 least significant bits of unsigned binary data sent by the master.

TRA<17:0>, TRB<17:0>, TRC<17:0>, TRD<17:0>
18-bit temporary storage registers assigned to each channel. Two MSBs store power-down information, 16 LSB store data.

DRA<17:0>, DRB<17:0>, DRC<17:0>, DRD<17:0>
18-bit DAC registers for each channel. Two MSBs store power-down information, 16 LSB store DAC data. An update of this register means a DAC update with data or power-down.

64 CHANNEL OPERATION

DAC8574 is designed to facilitate high channel count operation. DAC8574 supports multichannel simultaneous synchronous update up to 16 DAC8574 devices for up to 64 channels on a single I^2C bus. Working with multiple DAC8574s, single channel DAC8571s can be used on the same bus to obtain odd channel counts, or quad channel DAC7574s can be used if some channels only need 12 bits of resolution.

Data or power down can be loaded to temporary registers of each channel serially and a single broadcast operation can be used to update all channels of all devices simultaneously with previously stored data or power-down condition. Another feature useful for system start-up or system shut-down is to broadcast the same data (or power-down condition) to all channels with a single broadcast command.

All multichannel system updates are performed at the falling edge of the acknowledge signal that follows the least significant byte.

The 64-channel operation requires 6-bit address decoding. 4-bit address decoding is used to support 16 DAC8574 devices on the same bus and 2-bit address decoding is used to select one out of four channels of a DAC8574. 4-bit address decoding that selects one out of 16 DAC8574 devices is done as follows: To save I^2C address space, 2-bits (A0 and A1) are used for I^2C address decoding, and two additional bits (A2 and A3) are used for local address decoding. Up to 4 DAC8574 devices using the same I^2C address can be connected on the same I^2C bus. These four devices with the same I^2C address can be locally decoded using A2 and A3 pins. If multiple devices use the same I^2C address, multiple devices acknowledge at the same time. However, in order for a particular device to respond to a command, the states of the first two bits of the control word C<7> and C<6> must match the states of A3 and A2 pins. Four devices per I^2C address and four distinct I^2C addresses enable 16 devices on the same bus.

The four address pins should be set at power-up, and address bits must be set to match a particular device's address pins. To decode up to 16 DAC8574 devices, the logic states of A3, A2, A1, A0 address pins and C<7>, C<6>, A1, A0 address bits should be set as shown in (Temp Table 6)

Table 2. (Temp Table 6) 64 Channel Address Decoding

DEV #	A3 PIN	C7 BIT	A2 PIN	C6 BIT	A1 PIN	A1 BIT	A0 PIN	A0 BIT
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	1	1
3	0	0	0	0	1	1	0	0
4	0	0	0	0	1	1	1	1
5	0	0	1	1	0	0	0	0
6	0	0	1	1	0	0	1	1
7	0	0	1	1	1	1	0	0
8	0	0	1	1	1	1	1	1
9	1	1	0	0	0	0	0	0
10	1	1	0	0	0	0	1	1
11	1	1	0	0	1	1	0	0
12	1	1	0	0	1	1	1	1
13	1	1	1	1	0	0	0	0
14	1	1	1	1	0	0	1	1
15	1	1	1	1	1	1	0	0
16	1	1	1	1	1	1	1	1

Once a DAC8574 device is selected, channel select bits C <2> and C <1> can select a particular channel. Overall, I^2C address bits A1, A0, control bits C<7>, C<6>, C<2> and C<1> form the 6-bit address required to select one channel out of 64 possibilities.

Broadcast operation is supported for both I^2C addressing and for extended addressing. A broadcast address (10010000) makes all DAC8574 devices listen, regardless of the states of A0 and A1 pins. Also, a broadcast command (C<5>=C<4>=1) makes all devices listen, regardless of the states of A2 and A3 pins. The same broadcast command (C<5>=C<4>=1) also selects all channels for a given device, regardless of the states of channel select bits. Thus, a global broadcast message that simultaneously updates up to 64 channels uses 10010000 as I^2C address and has C<5>=C<4>=1 in the control word.

POWER-ON RESET

The DAC8574 contains a power-on-reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The DAC8574 contains four separate power-down modes of operation. These modes are programmable via two most significant bits of the MSB byte of the I^2C interface, while C<0>=1. (Temp Table 7)Table 3 shows how the state of the bits correspond to the mode of operation of the device.

Table 3. (Temp Table 7) Power-Down Modes of Operation for the DAC8574

(Temp Table 7) Power-Down Modes of Operation for the DAC8574 (continued)

C<0>	MSB<7>	MSB<6>	Operating Mode
1	0	0	High Impedance Output
1	0	1	1 kΩ to AGND
1	1	0	100 kΩ to AGND
1	1	1	High Impedance

When C<0>=0, the device works normally with its normal power consumption of 250 µA at 5 V per channel. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (50 nA at 3 V). Not only does the supply current fall but also the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while in power-down mode. There are three different options: The output is connected internally to AGND through a 1kΩ resistor, a 100kΩ resistor or it is left open-circuited (high impedance). The output stage is illustrated in .

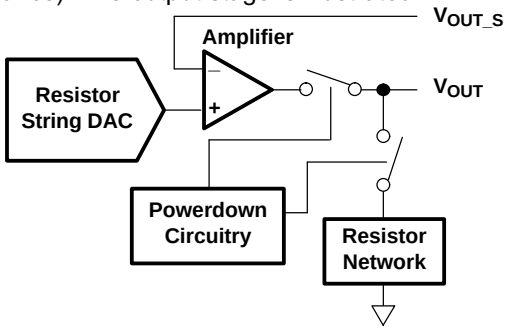


Figure 8. Output Stage During Power-Down

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for AV_{DD} = 5 V and 5 µs for AV_{DD} = 3 V. (See the Typical Curves section for additional information.)

The DAC8574 offers a flexible power-down interface based on channel register operation. A channel consists of a single 16 bit DAC with power-down circuitry, a temporary storage register (TR) and a DAC register (DR). TR and DR are both 18 bits wide. Two MSBs represent the power-down condition and the 16 LSBs represent data for TR and DR. By using bits 17 and 18 of TR and DR, a power-down condition can be temporarily stored and used just like data. Internal circuits ensure that MSB<7> and MSB<6> get transferred to TR<17> and TR<16> (DR<17> and DR<16>) when the power-down flag C<0> is set. Therefore, DAC8574 treats power-down conditions like data and all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DAC8574s in the system, or it is possible to simultaneously power down a channel while updating data on other channels.

CURRENT CONSUMPTION

The DAC8574 typically consumes 225 µA at V_{DD} = 5 V and 200 µA at V_{DD} = 3 V for each active channel, including reference current consumption. Additional current consumption can occur at the digital inputs if V_{IH} << V_{DD}. For most efficient power operation, CMOS logic levels are recommended at the digital inputs to the DAC. In power-down mode, typical current consumption is 200 nA. A delay time of 10 to 20 ms after a power-down command is issued to the DAC is typically sufficient for the power-down current to drop below 10 µA.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The DAC8574 output stage is capable of driving loads of up to 1000pF while remaining stable. Within the offset and gain error margins, the DAC8574 can operate rail-to-rail when driving a capacitive load. Resistive loads of 2 mW can be driven by the DAC8574 while achieving a typical load regulation of 1%. As the load resistance drops below 2 mW, the load regulation error increases. When the outputs of the DAC are driven to the positive rail under resistive loading, the PMOS transistor of each Class-AB output stage can enter into the linear region. When this occurs, the added IR voltage drop deteriorates the linearity performance of the DAC. This only occurs within approximately the top 20 mV of the DAC's digital input-to-voltage output transfer characteristic. The reference voltage applied to the DAC8574 may be reduced below the supply voltage applied to V_{DD} in order to eliminate this condition if good linearity is a requirement at full scale (under resistive loading conditions).

CROSSTALK AND AC PERFORMANCE

The DAC8574 architecture uses separate resistor strings for each DAC channel in order to achieve ultra-low crosstalk performance. DC crosstalk seen at one channel during a full-scale change on the neighboring channel is typically less than 0.5 LSBs. The ac crosstalk measured (for a full-scale, 1kHz sine wave output generated at one channel, and measured at the remaining output channel) is typically under -100dB. In addition, the DAC8574 can achieve typical ac performance of 96 dB signal-to-noise ratio (SNR) and 65 dB total harmonic distortion (THD), making the DAC8574 a solid choice for applications requiring low SNR at output frequencies at or below 4 kHz.

OUTPUT VOLTAGE STABILITY

The DAC8574 exhibits excellent temperature stability of ±3 ppm/°C typical output voltage drift over the specified temperature range of the device. This enables the output voltage of each channel to stay within a ±25 μV window for a ±1°C ambient temperature change. Good power-supply rejection ratio (PSRR) performance reduces supply noise present on V_{DD} from appearing at the outputs to well below 10 μV-s. Combined with good dc noise performance and true 16-bit differential linearity, the DAC8574 becomes a perfect choice for closed-loop control applications.

SETTLING TIME AND OUTPUT GLITCH PERFORMANCE

Settling time to within the 16-bit accurate range of the DAC8574 is achievable within 10 μs for a full-scale code change at the input. Worst case settling times between consecutive code changes is typically less than 2 μs, enabling update rates up to 500 ksps for digital input signals changing code-to-code. The high-speed serial interface of the DAC8574 is designed in order to support up to 200 ksps update rate. For full-scale output swings, the output stage of each DAC8574 channel typically exhibits less than 100 mV of overshoot and undershoot when driving a 200 pF capacitive load. Code-to-code change glitches are extremely low (~10 μV) given that the code-to-code transition does not cross an Nx4096 code boundary. Due to internal segmentation of the DAC8574, code-to-code glitches occur at each crossing of an Nx4096 code boundary. These glitches can approach 100mVs for N = 15, but settle out within ~2 μs.

USING REF02 AS A POWER SUPPLY FOR DAC8574

Due to the extremely low supply current required by the DAC8574, a possible configuration is to use a REF02 +5V precision voltage reference to supply the required voltage to the DAC8574's supply input as well as the reference input, as shown in Figure 10. This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V. The REF02 outputs a steady supply voltage for the DAC8574. If the REF02 is used, the current it needs to supply to the DAC8574 is 800 μA typical and 1200 μA max for V_{DD} = 5 V. When a DAC output is loaded, the REF02 also needs to supply the current to the load. The total typical current required (with a 5 μW load on a given DAC output) is:

800 μA (5V/ 5μW = 1.8 mA

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 392 mV for a 1.5-mA current draw from it. This corresponds to a 5.13 LSB error for a 0 V to 5 V output range.

LAYOUT

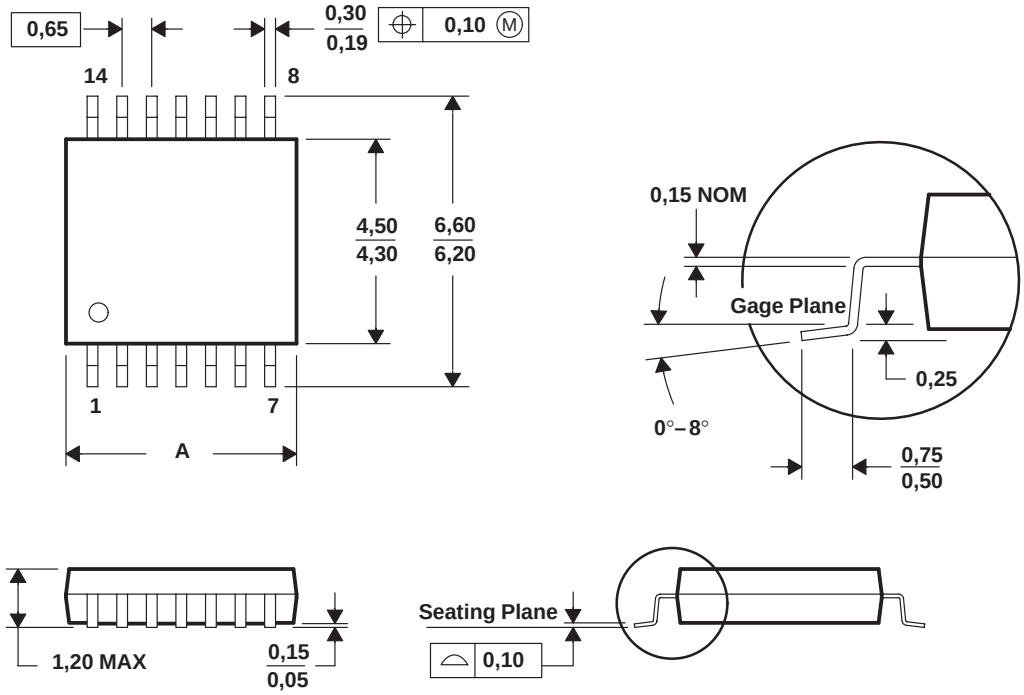
A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The power applied to AV_{DD} should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the AGND connection, AV_{DD} should be connected to a positive power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1 µF to 10 µF capacitor in parallel with a 0.1 µF bypass capacitor is strongly recommended. In some situations, additional bypassing may be required, such as a 100 µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the -5 V supply, removing the high-frequency noise.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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