National Semiconductor

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Enhanced Diversity Receiver Chipset CLC5526, CLC5957, and CLC5903

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General Description

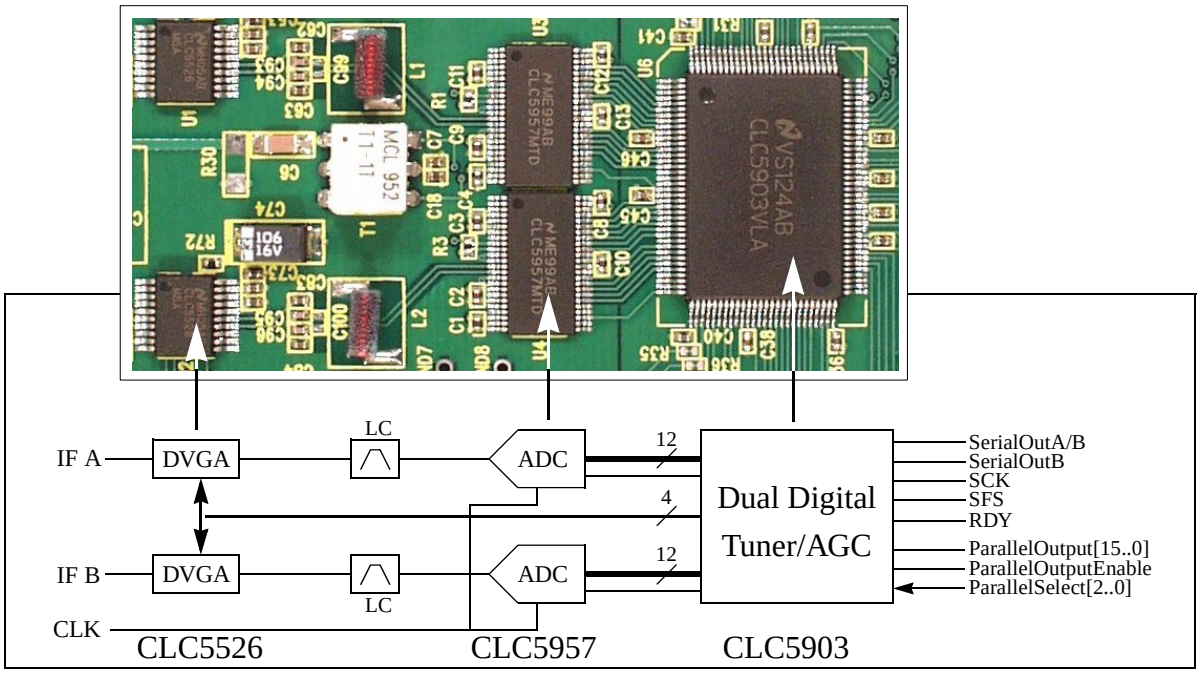
The Diversity Receiver Chipset (DRCS) is a five-chip narrowband receiver solution requiring less than 2.8 square inches of PC board area. The DRCS consists of five chips, including two CLC5526 Digitally-Controlled Variable Gain Amplifiers (DVGAs), two CLC5957 12-bit 70MSPS Analog-to-Digital Converters (ADCs), and one CLC5903 Dual Digital Tuner/AGC. IF inputs up to 300MHz produce digital quadrature symbols at baseband. Either two channel diversity or independent two channel operation can be supported by the DRCS.

The DRCS has been enhanced by replacing the CLC5902 with the CLC5903. In the Enhanced Diversity Receiver Chipset (EDRCS), the CLC5903 provides higher speed operation (78MHz vs. 52MHz) and lower power dissipation (290mW vs. 760mW). The CLC5903 also supports independent channel filter coefficients. Existing software is 100% forward compatible to ease the transition from the CLC5902 to the CLC5903.

This Diversity Receiver Chipset has been designed to support software configurable narrowband receivers. Direct IF-sampling removes the need for a second LO, mixer, and associated channel filters. All subsequent tuning and channel filtering is performed digitally by the CLC5903. Tuning is accomplished by quadrature mixing the digital input signal with a programmable digital LO signal. The quadrature mixer outputs are then channel-filtered by two sets of programmable FIR filters.

Features

- 70MSPS Operation
- Two Independent Channels
- Wide Dynamic Range: >120dB
- User Programmable AGC
- Direct IF Sampling to 300MHz
- Channel Filters include a Fourth Order CIC followed by 21-tap and 63-tap Symmetric FIRs
- Flexible output formats include 12 bit Floating Point and 8, 16, 24, or 32 bit Fixed Point
- Serial and Parallel output ports
- JTAG Boundary Scan
- Shutdown/Stand-by Capability
- Meets GSM, EDGE, PCS, DCS, AMPS, DAMPS, and PHS requirements
- Small Footprint
- Low Cost



AGC Operation

The AGC can operate in two modes, either *Inhibit* or *Free Run*.

AGC operation is based on envelope detection by an absolute value circuit followed by a digital lowpass filter. The filtered signal is applied to a programmable RAM look-up table to allow complete flexibility in setting the AGC threshold (attack point) and deadband (hysteresis). The RAM output is integrated and the resulting error signal drives the DVGAs. Integrator gain is programmable so that the loop time constant can be adjusted.

Dynamic Range

The ADC's 62dB SINAD (in Nyquist bandwidth, 150MHz input) is enhanced by the DVGA and digital processing to provide 120dB dynamic range in a 216kHz bandwidth. The DVGA compresses the input dynamic range prior to the ADC under the control of the AGC processor. Gain adjustment from -12dB to +30dB allows 42dB of compression. The compressed signal is optionally expanded in the digital domain to provide an extended linear output range. System noise sets the realizable dynamic range to 120dBFS in 200kHz.

The Diversity Receiver Chipset dynamic range is determined by the following component contributions:

Component	Input Dynamic Range (GSM)
CLC5526 DVGA	42dB Gain Range
CLC5526 DVGA	-7.2dB Noise Contribution
CLC5957 ADC	62dBFS SINAD (IF = 150MHz, F_S = 52MHz)
CLC5903 Processing Gain	23.7dB (10*log(52MHz/216kHz))
Total	120dBFS

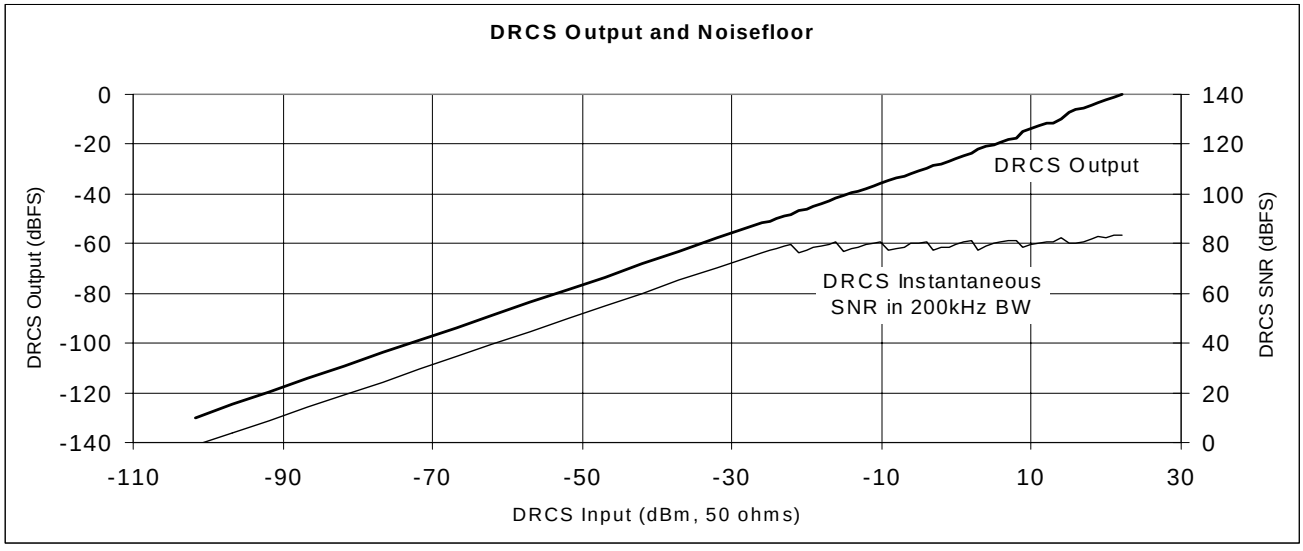
Processing gain comes from the reduction in output bandwidth provided by the channel filters. The channel filter bandwidth and output symbol rate are controlled by the division of the ADC sample rate (decimation ratio). In a GSM system the desired output symbol rate is 270.83kHz. The FIR channel filter coefficients should be set for a bandwidth of approximately 0.8 times the symbol rate or 216kHz. In this case, the noise will be reduced by a factor of 52MHz/216kHz or 23.7dB. The greater the ratio of ADC sample rate to channel filter bandwidth the better the system noise performance.

The CLC5903 accepts inputs up to 14-bits. AGC operation generates a 3-bit exponent which can scale the 14-bit input words into the 21-bit internal word width. The output of the final FIR filter is 32 bits and either 8, 16, 24, or 32 bits of this data can be selected for output. The output words are available in standard DSP serial formats or 16-bit parallel words. The DVGAs and the CLC5903 can be configured to provide compressed dynamic range or the full linear dynamic range of more than 120dBFS.

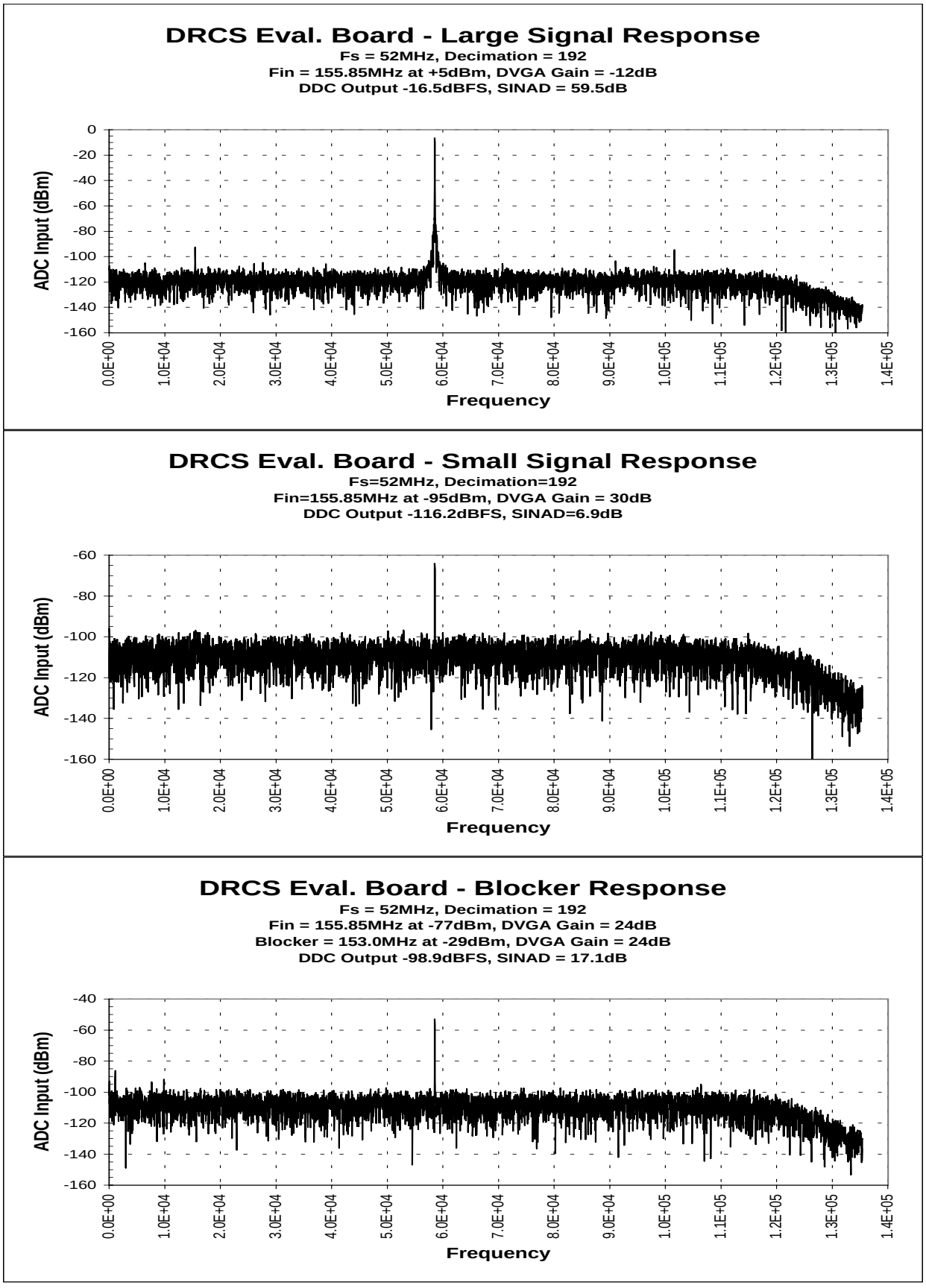
As the input signal increases, the DVGA will attenuate the ADC input signal in 6dB steps. The ADC output is scaled up in 6dB steps to maintain a linear input to output relationship. A representative example of the expanded dynamic range of the Diversity Receiver Chipset is shown in the figure below. The 42dB gain range of the DVGA can be clearly seen in the difference between the ADC output and the CLC5903 output. The zero SINAD point can be seen where Pin = -120dBFS.

System operation

The CLC5957 has a flexible clock input circuit which can accept sine, TTL, or PECL. It also provides a TTL data valid output clock designed to drive the CLC5903. This clock is divided by the CLC5903 to generate the desired output sample rate and to set the channel filter bandwidth. Typical system power requirements include 1.76W at +5V, 0.142W at +3.3V, and 0.144W at 1.8V for 52MSPS operation. Shutdown/stand-by modes are available for the DVGAs and the ADCs. The CLC5903 power requirements are reduced when the input clock is stopped.

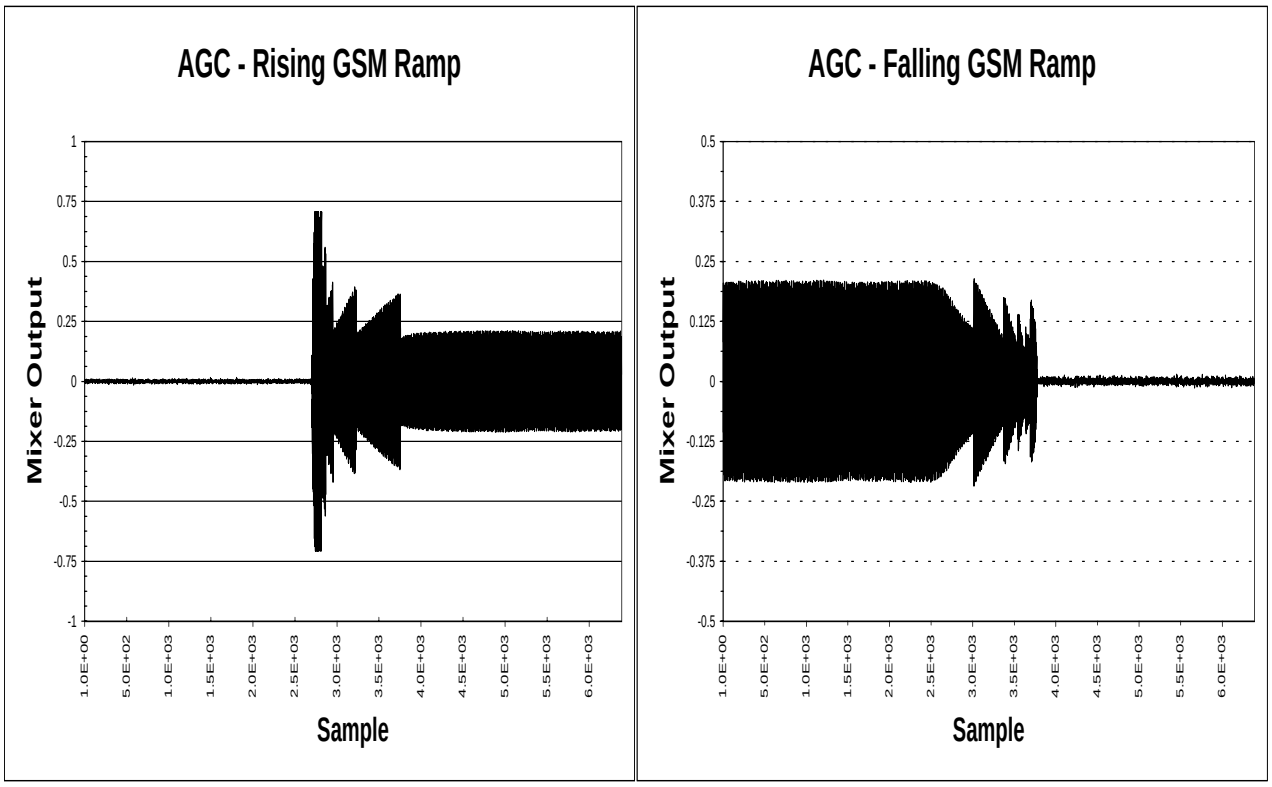


Diversity Receiver Chipset Measured Data:

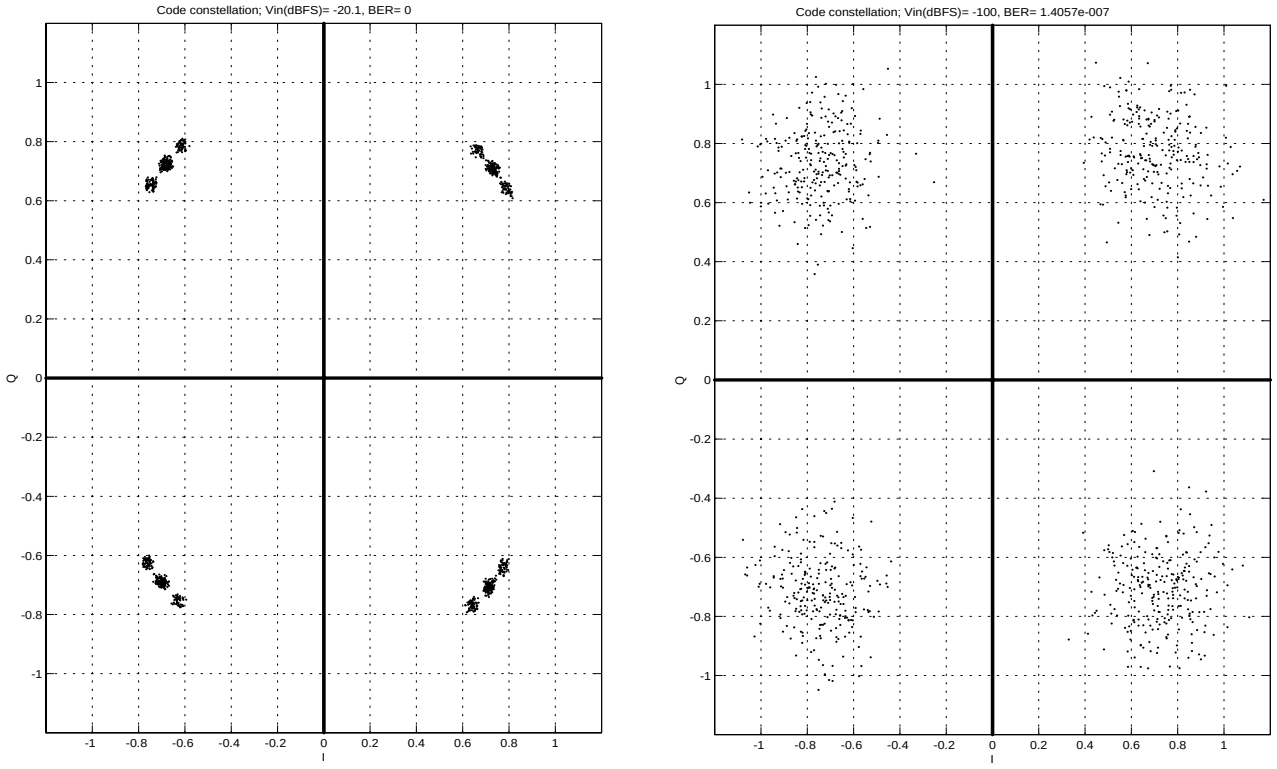


Dynamic AGC Performance (GSM Burst):

30µsec 70dB power ramp at ADC output, Fs = 52MSPS, Fin = 150MHz
AGC operation during a burst does not impair equalizer/demodulator operation.



Diversity Receiver Chipset GSM Constellation:



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