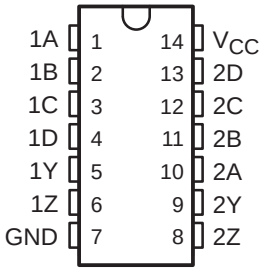
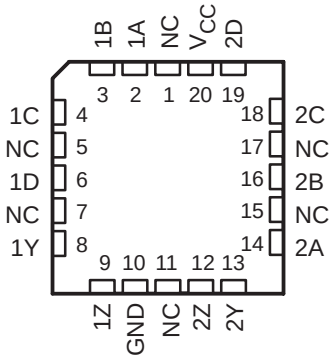
SLLS093D – OCTOBER 1972 – REVISED APRIL 1998

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **Short-Circuit Protection of Outputs**
- **Output Clamp Diodes to Terminate Line Transients**
- **High-Current Outputs**
- **Quad Inputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Designed for Use With Dual Differential Drivers SN55182 and SN75182**
- **Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830**

SN55183 . . . J OR W PACKAGE
SN75183 . . . D OR N PACKAGE
DS8830 . . . N PACKAGE
(TOP VIEW)



SN55183 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE DS8830 AND SN55183 ARE NOT RECOMMENDED FOR NEW DESIGNS

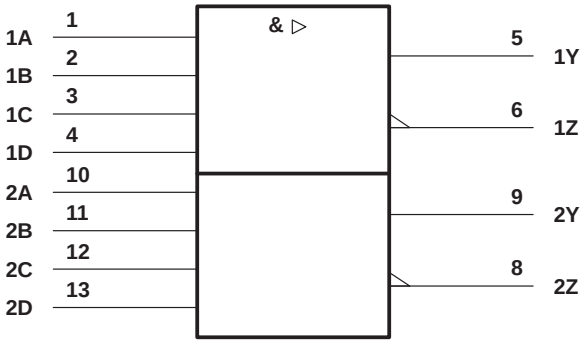
description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices can be used as TTL expander/phase splitters, because the output stages are similar to TTL totem-pole outputs.

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

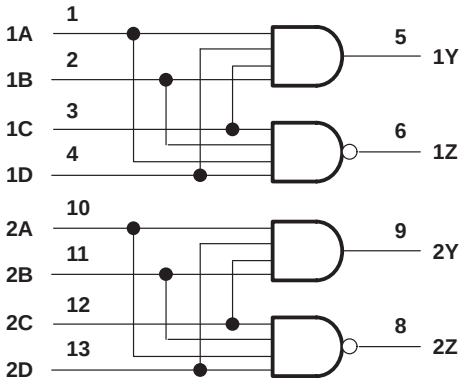
The SN55183 is characterized for operation over the full military temperature range of –55°C to 125°C. The DS8830 and SN75183 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

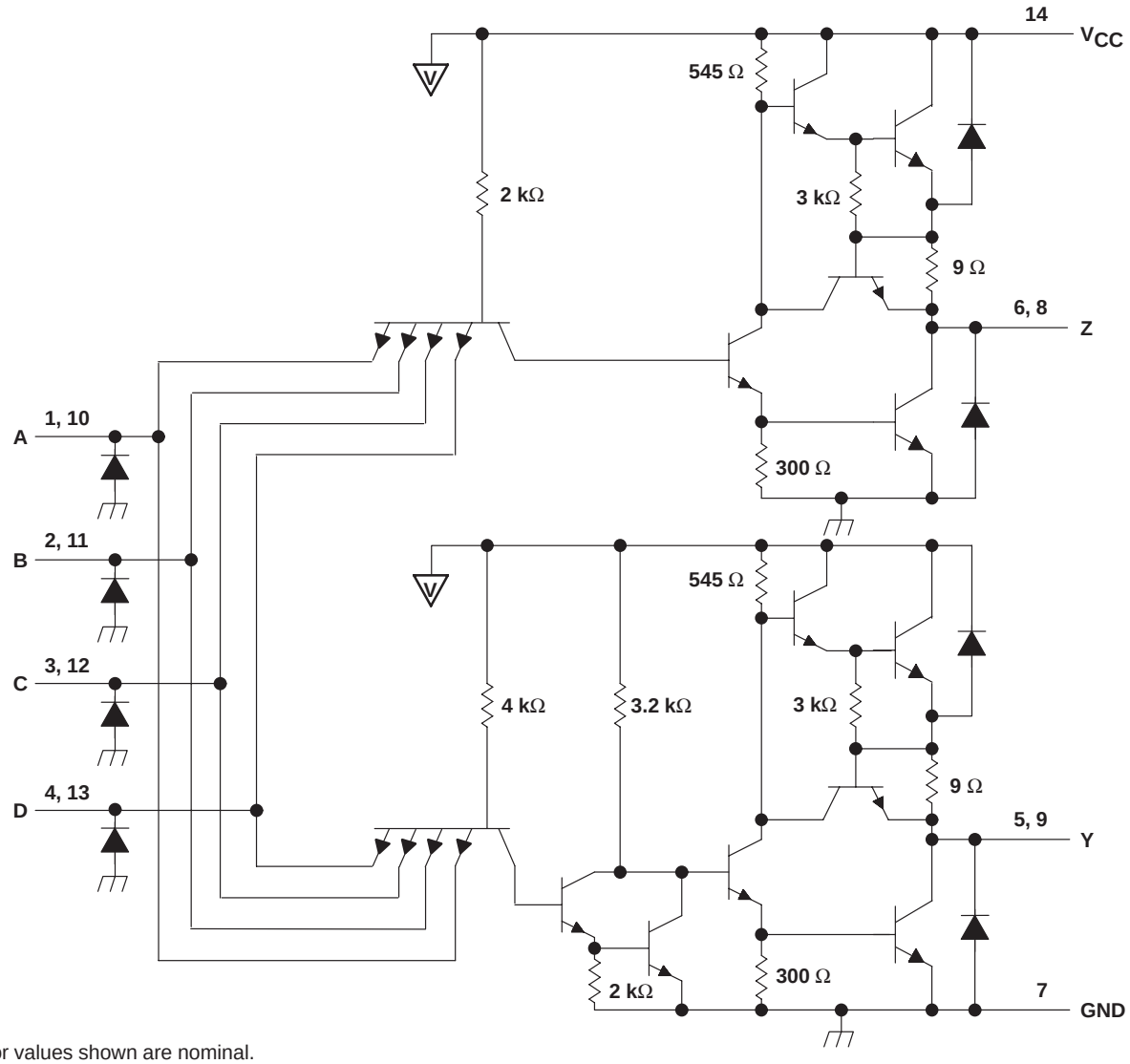
logic diagram (positive logic)



Positive logic: $y = ABCD$, $Z = \overline{ABCD}$

Pin numbers shown are for the D, J, N, and W packages.

schematic (each driver)



Resistor values shown are nominal.
Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Duration of output short circuit (see Note 2) . . . . . 1 s
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Case temperature for 60 seconds, T_c: FK package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at any one time.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W‡	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK, J, and W packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

recommended operating conditions

	SN55183			DS8830, SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			–40			–40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

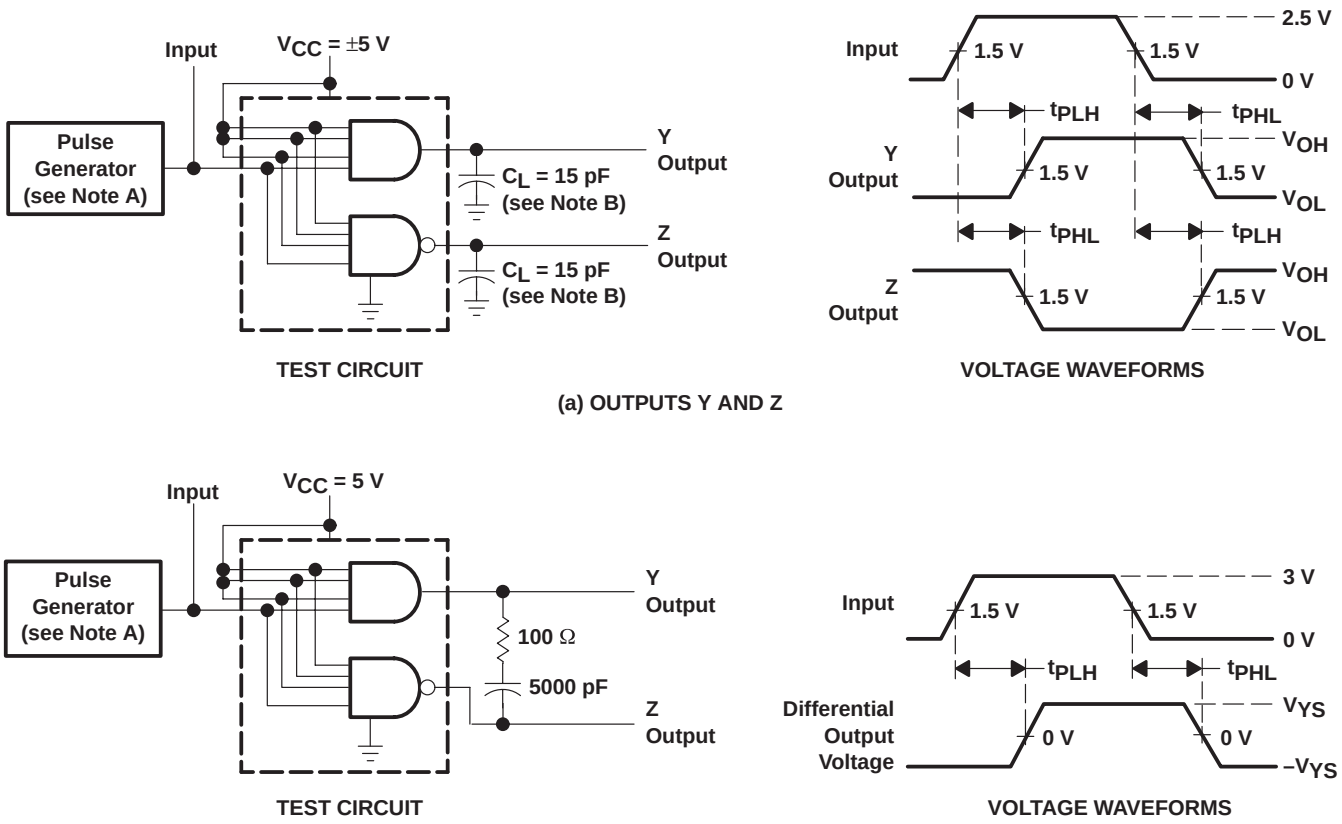
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Y (AND) outputs	V_{IH} = 2 V	I_{OH} = –0.8 mA	2.4			V
				I_{OH} = –40 mA	1.8	3.3		
V_{OL}	Low-level output voltage	Y (AND) outputs	V_{IL} = 0.8 V	I_{OL} = 32 mA		0.2		V
				I_{OL} = 40 mA		0.22	0.4	
V_{OH}	High-level output voltage	Z (NAND) outputs	V_{IL} = 0.8 V	I_{OH} = –0.8 mA	2.4			V
				I_{OH} = –40 mA	1.8	3.3		
V_{OL}	Low-level output voltage	Z (NAND) outputs	V_{IH} = 2 V	I_{OL} = 32 mA		0.2		V
				I_{OL} = 40 mA		0.22	0.4	
I_{IH}	High-level input current		V_{IH} = 2.4 V				120	μA
I_I	Input current at maximum input voltage		V_{IH} = 5.5 V				2	mA
I_{IL}	Low-level input current		V_{IL} = 0.4 V				–4.8	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V,	T_A =125°C§	–40	–100	–120	mA
I_{CC}	Supply current (average per driver)		V_{CC} = 5 V,	All inputs at 5 V, No load		10	18	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.
§ T_A = 125°C is applicable to SN55183 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level Y output	AND gates	C_L = 15 pF, See FIgure 1(a)		8	12	ns
t_{PHL}	Propagation delay time, high- to low-level Y output	AND gates	C_L = 15 pF, See FIgure 1(a)		12	18	ns
t_{PLH}	Propagation delay time, low- to high-level Z output	NAND gates	C_L = 15 pF, See FIgure 1(a)		6	12	ns
t_{PHL}	Propagation delay time, high- to low-level Z output	NAND gates	C_L = 15 pF, See FIgure 1(a)		6	8	ns
t_{PLH}	Propagation delay time, low- to high-level differential output	Y output with respect to Z output, R_L = 100 Ω in series with 5000 pF, See Figure 1(b)			9	16	ns
t_{PHL}	Propagation delay time, high- to low-level differential output	Y output with respect to Z output, R_L = 100 Ω in series with 5000 pF, See Figure 1(b)			8	16	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \le 10$ ns, $t_f \le 10$ ns, t_W = 0.5 µs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with $r_i \ge 1$ MΩ.

Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

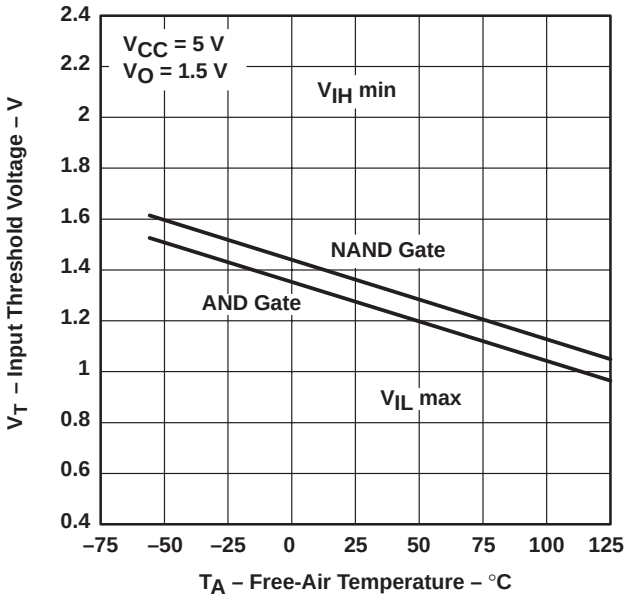


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

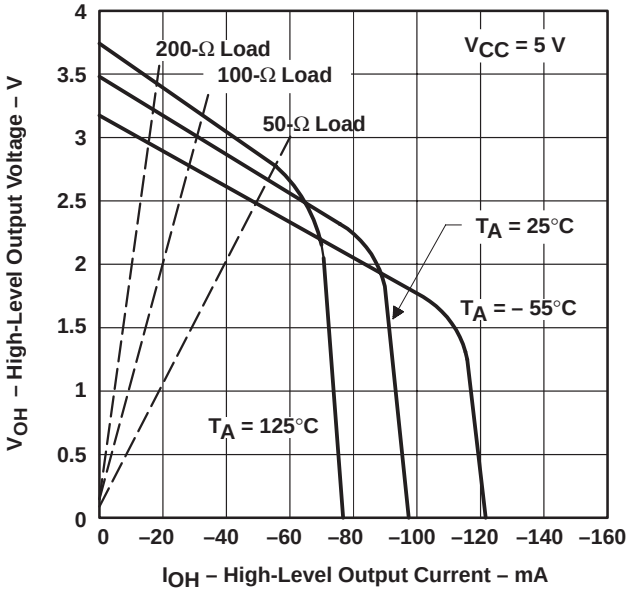


Figure 3

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL OUTPUT CURRENT

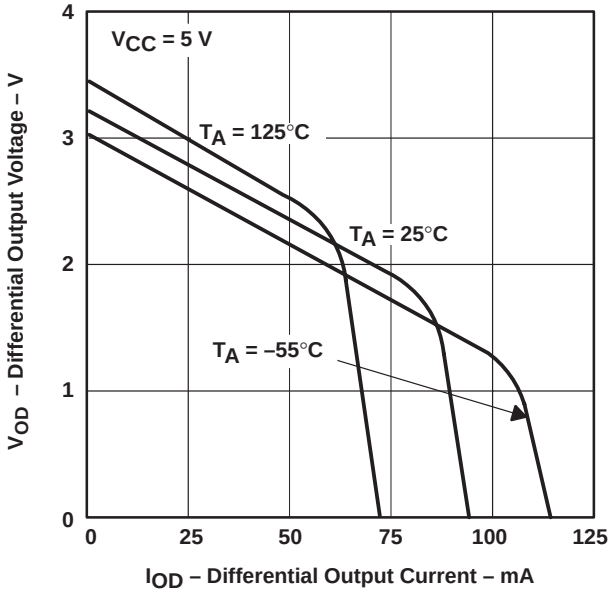


Figure 4

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

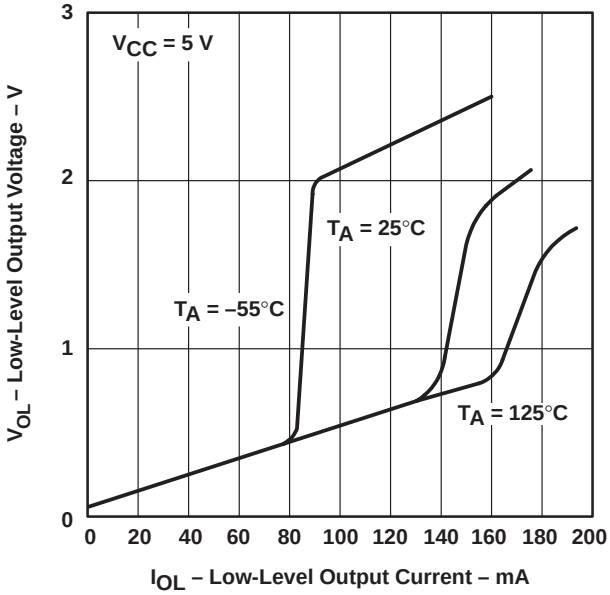


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME (DIFFERENTIAL OUTPUT) vs FREE-AIR TEMPERATURE

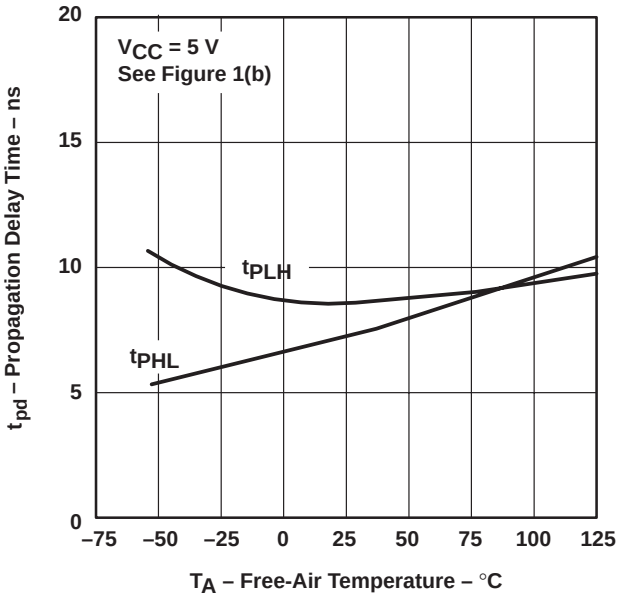


Figure 6

TOTAL POWER DISSIPATION (BOTH DRIVERS) vs FREQUENCY

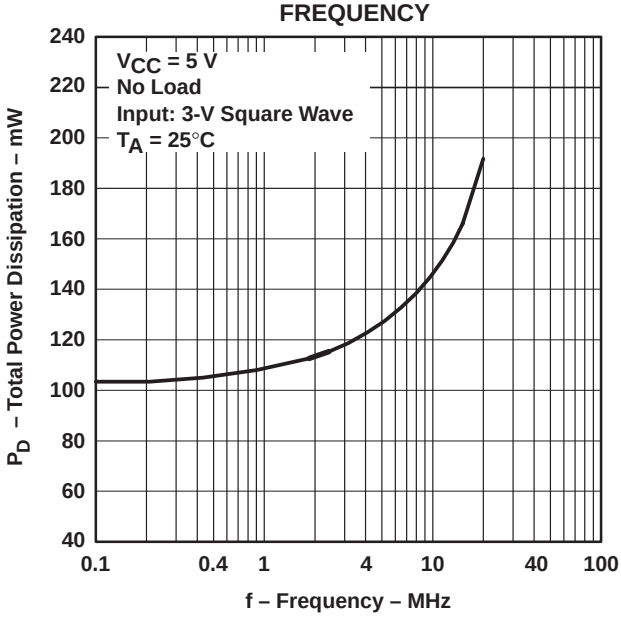
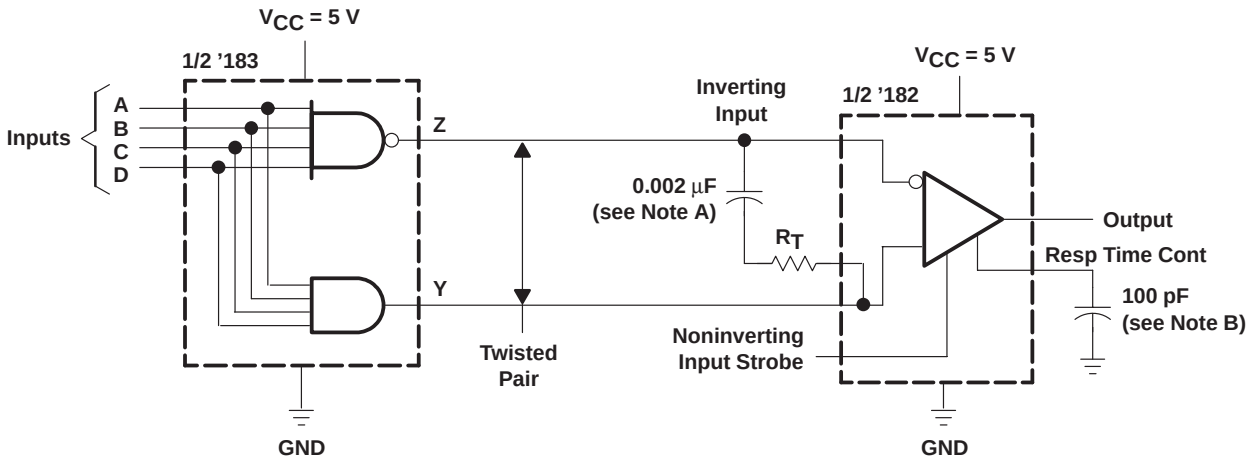


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let f = 5 MHz
C = 0.002 μF

$$Z_{(circuit)} = \frac{1}{2\pi fC} = \frac{1}{2\pi\left(5 \times 10^{6}\right)\left(0.002 \times 10^{-6}\right)}$$

$$Z_{(circuit)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 8. Transmission of Digital Data Over Twisted-Pair Line

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