PWM LOW-SIDE DRIVER (1.5A and 3A)
for Solenoids, Coils, Valves, Heaters, and Lamps

FEATURES

● **HIGH OUTPUT DRIVE: 1.5A and 3A Versions**
● **WIDE SUPPLY RANGE: +8V to +32V**
● **COMPLETE FUNCTION**
  Digitally Controlled Input
  PWM Output
  Adjustable Internal Oscillator: 500Hz to 100kHz
  Adjustable Delay and Duty Cycle
● **FULLY PROTECTED**
  **Thermal and Current Limit Shutdown with
  Status OK Indicator Flag**
● **PACKAGES: SO-8 and PowerPAD™ SO-8**

APPLICATIONS

● **ELECTROMECHANICAL DRIVER:**
  **Solenoids, Valves, Positioners, Actuators,
  Relays, Power Contactor Coils, Heaters, Lamps**
● **HYDRAULIC AND PNEUMATICS SYSTEMS**
● **PART HANDLERS AND SORTERS**
● **CHEMICAL PROCESSING**
● **ENVIRONMENTAL MONITORING AND HVAC**
● **THERMOELECTRIC COOLERS**
● **DC MOTOR SPEED CONTROLS**
● **MEDICAL AND SCIENTIFIC ANALYZERS**
● **FUEL INJECTOR DRIVERS**

PowerPAD is a trademark of Texas Instruments.

DESCRIPTION

The DRV103 is a low-side DMOS power switch employing a pulse-width modulated (PWM) output. Its rugged design is optimized for driving electromechanical devices such as valves, solenoids, relays, actuators, motors, and positioners. The DRV103 is also ideal for driving thermal devices such as heaters, coolers, and lamps. PWM operation conserves power and reduces heat rise, resulting in higher reliability. In addition, adjustable PWM allows fine control of the power delivered to the load. DC-to-PWM output delay time and oscillator frequency are also externally adjustable.

The DRV103 can be set to provide a strong initial closure, automatically switching to a "soft" hold mode for power savings. A resistor, analog voltage, or Digital-to-Analog (D/A) converter can control the duty cycle. An output OK flag indicates when thermal shutdown or over current occurs.

Two packages provide a choice of output current: 1.5A (SO-8) or 3A (PowerPAD™ SO-8 with exposed metal heat sink).

The DRV103 is specified for –40°C to +85°C.
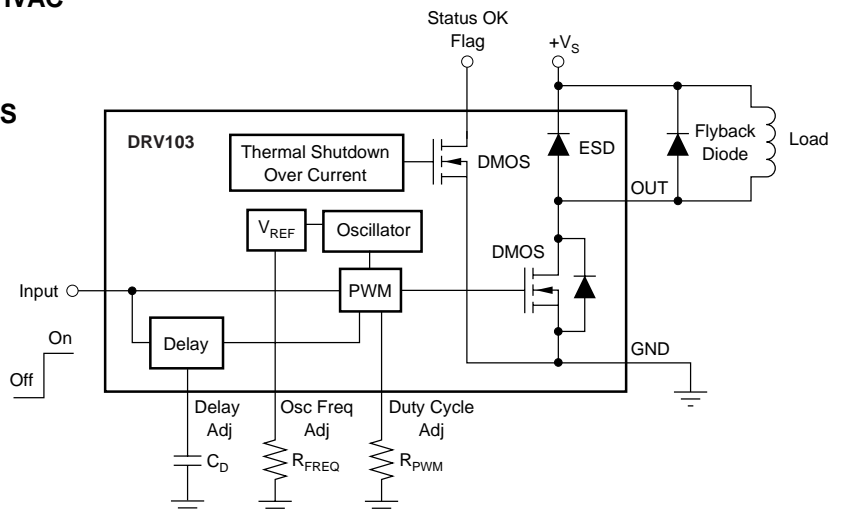
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
DRV103U	SO-8	182	–40°C to +85°C	DRV103U	DRV103U DRV103U/2K5	Rails Tape and Reel
"	"	"	"	"		
DRV103H	PowerPAD™ SO-8	DDA	–40°C to +85°C	DRV103H	DRV103H DRV103H/2K5	Rails Tape and Reel
"	"	"	"	"		

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DRV103U/2K5" will get a single 2500-piece Tape and Reel.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V_S[2] .... +40V
Input Voltage .... –0.2V to +5.5V[3]
PWM Adjust Input .... –0.2V to +5.5V[3]
Delay Adjust Input .... –0.2V to +5.5V[3]
Frequency Adjust Input .... –0.2V to +5.5V[3]
Status OK Flag and OUT .... –0.2V to V_S[4]
Operating Temperature Range ....–55°C to +125°C
Storage Temperature Range ....–65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) .... +300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) See Bypassing section for discussion about operating near maximum supply voltage. (3) Higher voltage may be applied if current is limited to 2mA. (4) The Status OK Flag will internally current limit at about 10mA.

⚠ ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
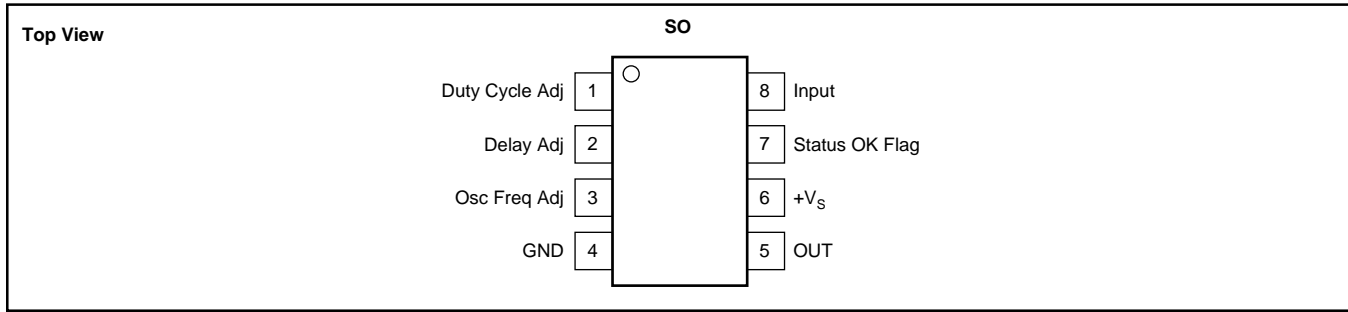
TEXAS INSTRUMENTS

ELECTRICAL CHARACTERISTICS

At T_C = +25°C, V_S = +24V, Load = 100Ω, and 4.99kΩ "OK Flag" pullup to +5V, Delay Adj Capacitor = 100pF to Ground, Freq Adj Resistor = 205kΩ to Ground, Duty Cycle Adj Resistor = 137kΩ to Ground, unless otherwise noted.

PARAMETER	CONDITIONS	DRV103U, H			UNITS
		MIN	TYP	MAX	
OUTPUT					
Output Current[1]	SO-8 Package (U)		1.5		A
	PowerPAD™ SO-8 Package (H)		3		A
Output Saturation Voltage, Source	I_O = 1A		+0.4	+0.6	V
	I_O = 0.1A		+0.05	+0.07	V
Current Limit[2], [10]		3	3.5	4.2	A
Leakage Current	DMOS Output Off, V_O = +32V		±1	±10	µA
DIGITAL CONTROL INPUT[3]					
V_{CTR} Low (output disabled)		0		+1.2	V
V_{CTR} High (output enabled)		+2.2		+5.5	V
I_{CTR} Low (output disabled)	V_{CTR} = 0V		0.01	1	µA
I_{CTR} High (output enabled)	V_{CTR} = +5.5V		120	150	µA
Propagation Delay	On-to-Off and Off-to-On		1		µs
DELAY TO PWM[4]	DC to PWM Mode				
Delay Equation[5]			See Note (6)		s
Delay Time	C_D = 0.1µF	90	110	140	ms
Minimum Delay Time[7]	C_D = 0		18		µs
DUTY CYCLE ADJUST					
Duty Cycle Range			10 to 90		%
Duty Cycle Accuracy	50% Duty Cycle, 25kHz		±2		%
vs Supply Voltage	50% Duty Cycle, V_S = V_O = +8V to +32V		±2		%
Nonlinearity[8]	10% to 90% Duty Cycle		1		% FSR
DYNAMIC RESPONSE					
Output Voltage Rise Time	V_O = 10% to 90% of V_S		0.2	2	µs
Output Voltage Fall Time	V_O = 90% to 10% of V_S		0.2	2	µs
Oscillator Frequency Range	External Adjust		0.5 to 100		kHz
Oscillator Frequency	R_{OSC} = 205kΩ	20	25	30	kHz
OK FLAG					
Normal Operation	20kΩ Pull-Up to +5V	+4.5	5.0		V
Fault[90]	Sinking 1mA		+0.22	+0.4	V
Sink Current	V_{OKFLAG} = 0.4V		2		mA
Over-Current Flag: Set			5		µs
THERMAL SHUTDOWN					
Junction Temperature					
Shutdown			+160		°C
Reset from Shutdown			+140		°C
POWER SUPPLY					
Specified Operating Voltage			+24		V
Operating Voltage Range		+8		+32	V
Quiescent Current	I_O = 0		0.4	0.8	mA
TEMPERATURE RANGE					
Specified Range		−40		+85	°C
Operating Range		−55		+125	°C
Storage Range		−65		+150	°C
Thermal Resistance, θ_{JA}					
SO-8 (U)	1in² 0.5oz. Copper on PCB		150		°C/W
PowerPAD™ SO-8 (H)[10]	1in² 0.5oz. Copper on PCB		68		°C/W

NOTES: (1) Output current is limited by internal current limit and by DRV103 power dissipation. (2) Output current resets to zero when current limit is reached. (3) Logic High enables output (normal operation). (4) Constant DC output to PWM (Pulse-Width Modulated) time. (5) Maximum delay is determined by an external capacitor. Pulling the Delay Adjust Pin LOW corresponds to an infinite (continuous) delay. (6) Delay to PWM $\approx C_D \bullet 10^6$ (C_D in F • 1.1). (7) Connecting the Delay Adjust Pin to +5V reduces delay time to less than 1µs. (8) V_{IN} at pin 3 to percent of duty cycle at pin 6. (9) OK Flag LOW indicates fault from over-temperature or over-current conditions. (10) PowerPAD™ SO-8 (H) package has highest continuous current (2A) because the chip operates at a lower junction temperature when underside metal tab is connected to a heat sink or heat spreader. θ_{JA} = 68°C/W measured on DRV103 demo board; θ_{JA} = 58°C/W measured on JEDEC standard test board. H package θ_{JC} = 16.7°C/W.

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PIN CONFIGURATION

Top View

SO

Duty Cycle Adj	1		8	Input
Delay Adj	2		7	Status OK Flag
Osc Freq Adj	3		6	+V_S
GND	4		5	OUT

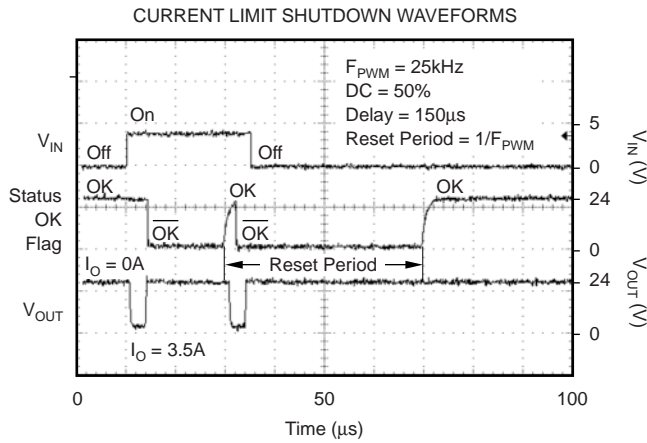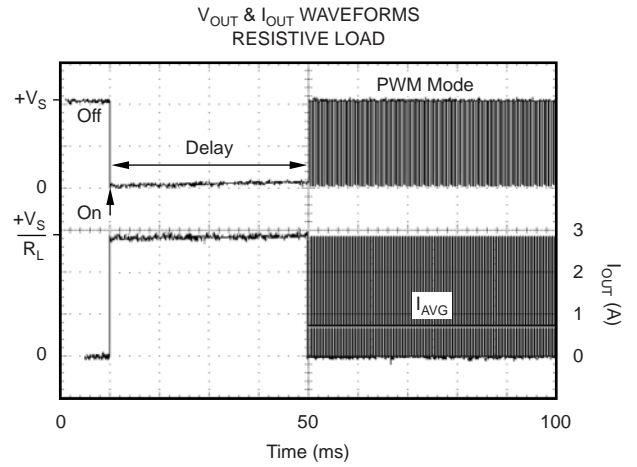## PIN DESCRIPTIONS

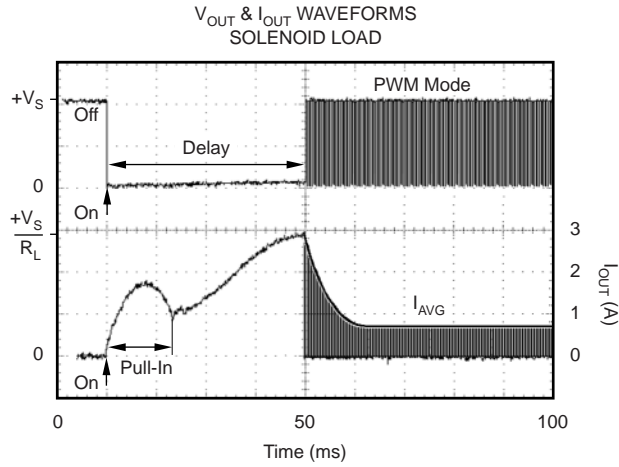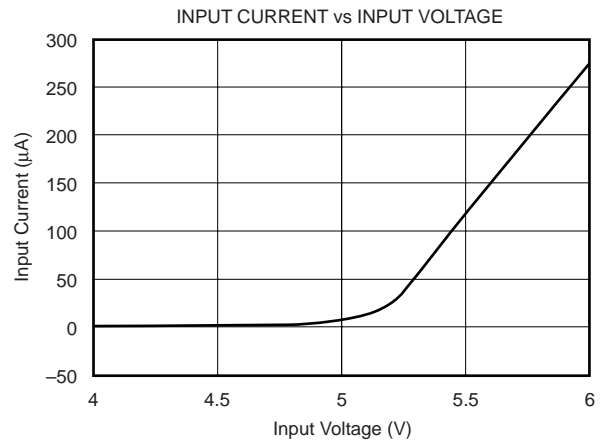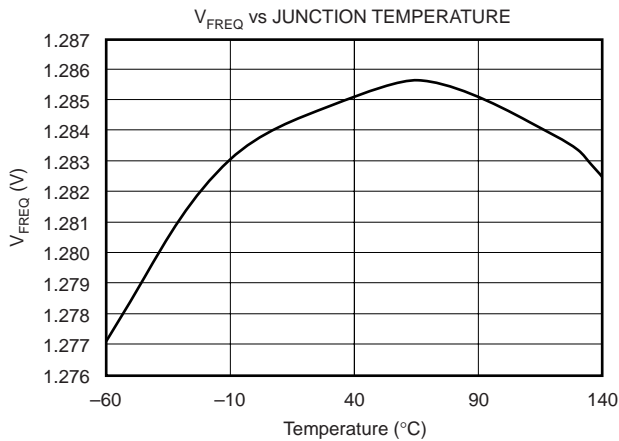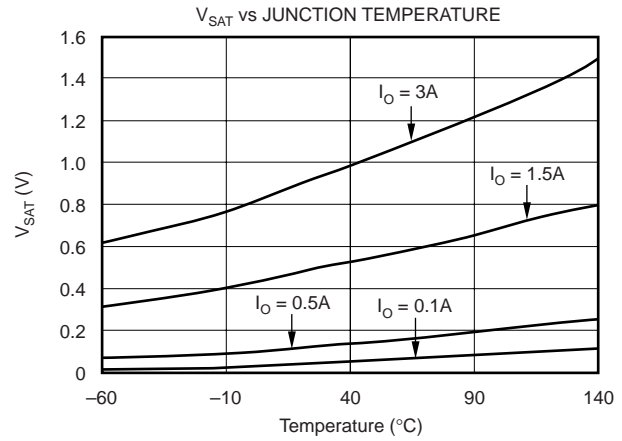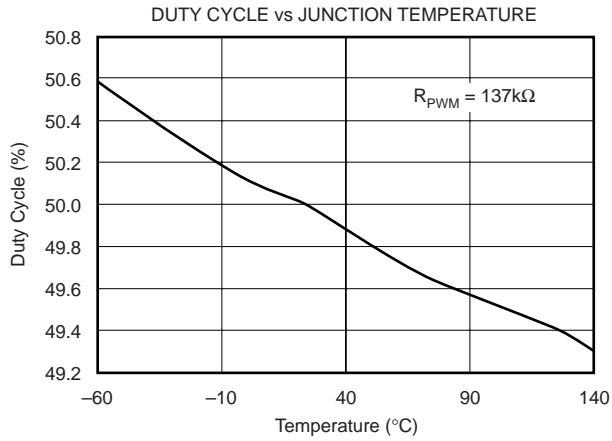| PIN #	NAME	DESCRIPTION
Pin 1	Duty Cycle Adjust	Internally, this pin connects to the input of a comparator and a (2.75 x I_{REF}) current source from V_S. The voltage at this node linearly sets the duty cycle. Duty cycle can be programmed with a resistor, analog voltage, or the voltage output of a D/A converter. The active voltage range is from 1.3V to 3.9V to facilitate the use of single-supply control electronics. At 3.56V, output duty cycle is near 90%. At 1.5V, output duty cycle is near 10%.
Pin 2	Delay Adjust	This pin sets the duration of the initial 100% duty cycle before the output goes into PWM mode. Leaving this pin floating results in a delay of approximately 18µs, which is internally limited by parasitic capacitance. Minimum delay may be reduced to less than 1µs by tying the pin to 5V. This pin connects internally to a 3µA current source from V_S and to a 2.6V threshold comparator. When the pin voltage is below 2.6V, the output device is 100% ON. The PWM oscillator is not synchronized to the Input (pin 1), so the duration of the first pulse may be any portion of the programmed duty cycle.
Pin 3	Oscillator Frequency Adjust	PWM frequency is adjustable. A resistor to ground sets the current I_{REF} and the internal PWM oscillator frequency. A range of 500Hz to 100kHz can be achieved with practical resistor values. Although oscillator frequency operation below 500Hz is possible, resistors higher than 10M will be required. The pin then becomes a very high impedance node and is, therefore, sensitive to noise pickup and PCB leakage currents.
Pin 4	GND	This pin must be connected to system ground for the DRV103 to function. It carries the 0.4mA quiescent current plus the full load current when the power DMOS transistor is switched on.
Pin 5	OUT	The output is the drain of a power DMOS transistor with its source connected to ground. Its low on-resistance (0.5Ω typ) assures low power dissipation in the DRV103. Gate drive to the power device is controlled to provide a slew-rate limited rise and fall time. This reduces radiated RFI/EMI noise. A flyback diode is needed with inductive loads to conduct the load current during the off cycle. The external diode should be selected for low forward voltage and low storage time. The internal clamp diode (an ESD protection diode) provides some degree of back-EMF protection but it should not be used as a flyback diode.
Pin 6	+V_S	This is the power supply pin. Operating range is +8V to +32V. +V_S must be ≥ the supply voltage to the load.
Pin 7	Status OK Flag	Normally HIGH (active LOW), a Flag LOW signals either an over-temperature or over-current fault. The over-current flag (Status OK) is LOW only when the output is ON (constant DC output or the "ON" portion of PWM mode). A thermal fault (thermal shutdown) occurs when the die surface reaches approximately 160°C and latches until the die cools to 140°C. This output requires a pull-up resistor and it can typically sink 2mA, sufficient to drive a low-current LED. Sink current is internally limited at 10mA typical.
Pin 8	Input	The input is compatible with standard TTL levels. The device output becomes enabled when the input voltage is driven above the typical switching threshold, 1.7V. Below this level, the output is disabled. Input current is typically 10nA when driven HIGH and 10nA with the input LOW. The input should not be directly connected to the power supply (V_S) or damage will occur.

LOGIC BLOCK DIAGRAM

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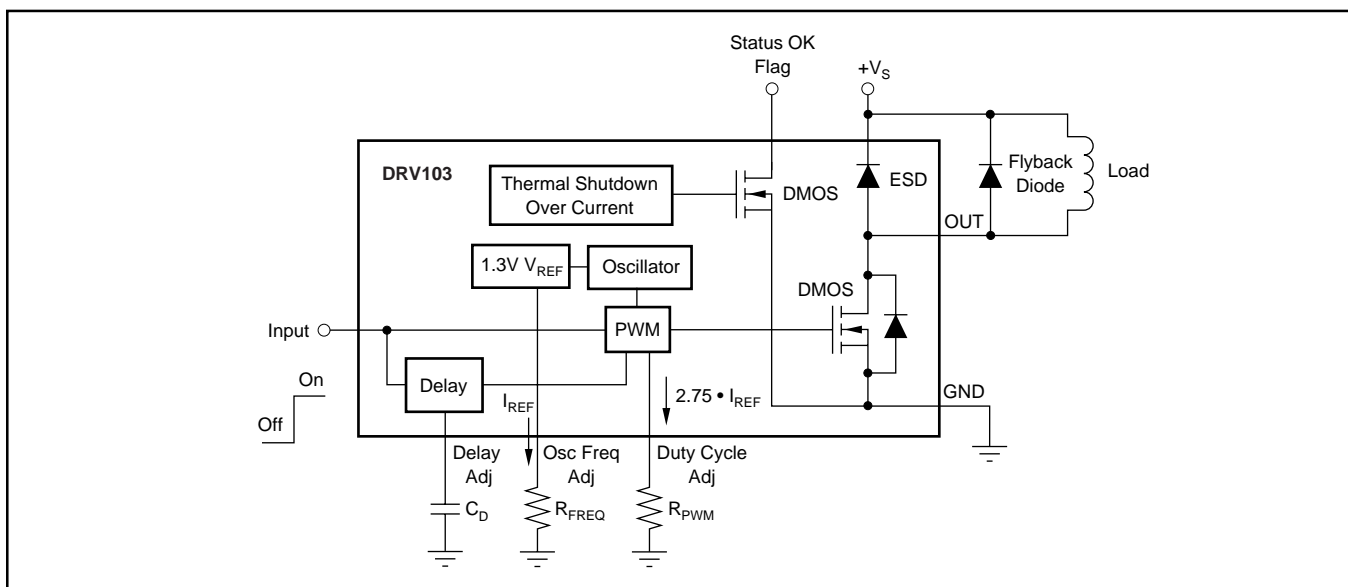
TYPICAL CHARACTERISTICS

At T_C = +25°C and V_S = +24V, unless otherwise noted.

V_OUT & I_OUT WAVEFORMS
SOLENOID LOAD

V_OUT & I_OUT WAVEFORMS
RESISTIVE LOAD

CURRENT LIMIT SHUTDOWN WAVEFORMS

QUIESCENT CURRENT
vs JUNCTION TEMPERATURE

CURRENT LIMIT
vs JUNCTION TEMPERATURE

DELAY vs JUNCTION TEMPERATURE

TEXAS
INSTRUMENTS
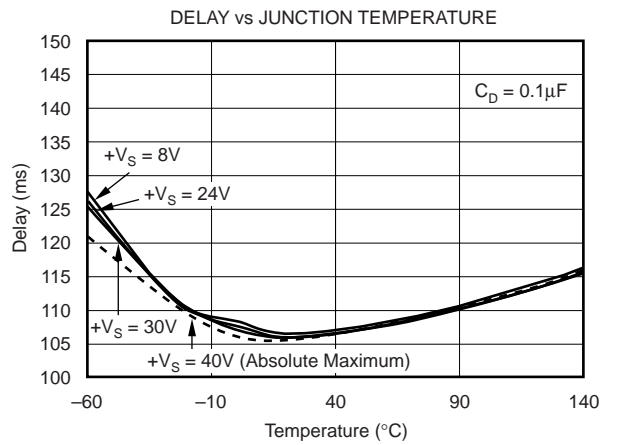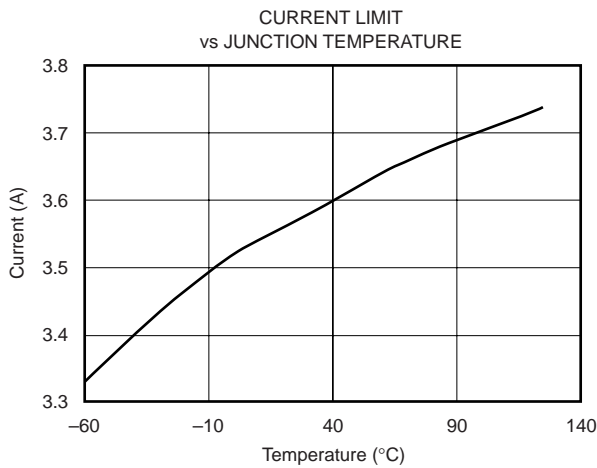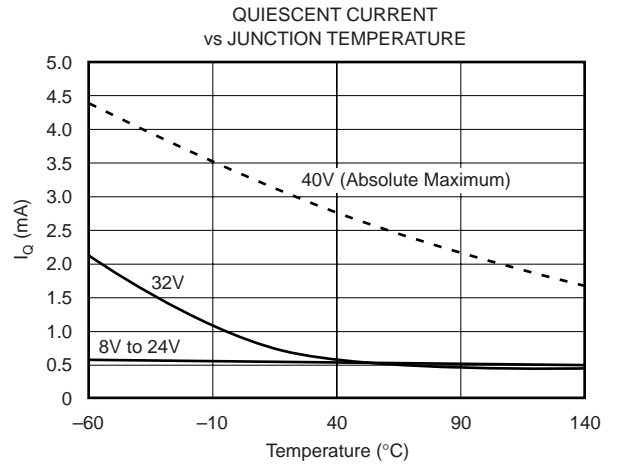
TYPICAL CHARACTERISTICS (Cont.)

At T_C = +25°C and V_S = +24V, unless otherwise noted.

MINIMUM DELAY vs JUNCTION TEMPERATURE

C_D = 0pF

OSCILLATOR FREQUENCY
vs JUNCTION TEMPERATURE

DUTY CYCLE vs JUNCTION TEMPERATURE

R_{PWM} = 137kΩ

V_{SAT} vs JUNCTION TEMPERATURE

I_O = 3A

I_O = 1.5A

I_O = 0.5A

I_O = 0.1A

V_{FREQ} vs JUNCTION TEMPERATURE

INPUT CURRENT vs INPUT VOLTAGE

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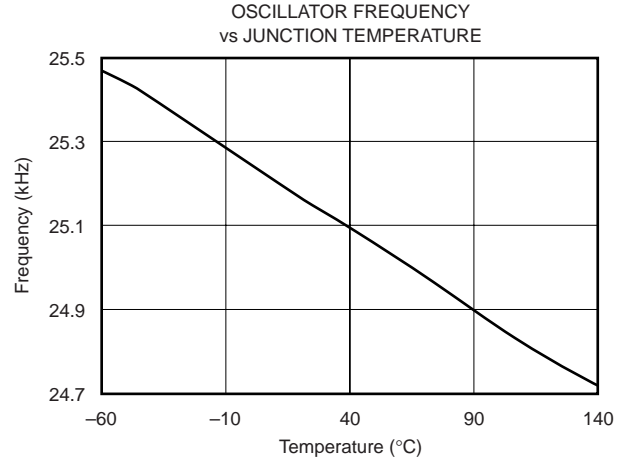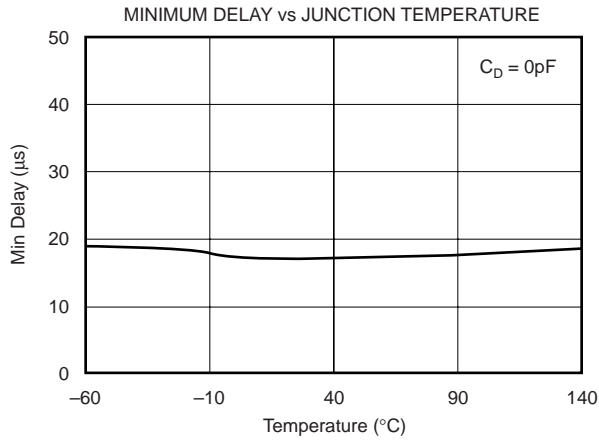
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BASIC OPERATION

The DRV103 is a low-side, DMOS power switch employing a Pulse-Width Modulated (PWM) output for driving electro-mechanical and thermal devices. Its design is optimized for two types of applications: a two-state driver (open/close) for loads such as solenoids and actuators; and a linear driver for valves, positioners, heaters, and lamps. Its low 0.5Ω "ON" resistance, small size, adjustable delay to PWM mode, and adjustable duty cycle make it suitable for a wide range of applications.

Figure 1 shows the basic circuit connections to operate the DRV103. A $1\mu F$ ($22\mu F$ when driving high current loads) or larger tantalum bypass capacitor is recommended on the power-supply pin.

Input (pin 8) is level-triggered and compatible with standard TTL levels. An input voltage between +2.2V and +5.5V turns the device's output ON, while a voltage of 0V to +1.2V shuts the DRV103's output OFF. Input bias current is typically 1pA. Delay Adjust (pin 2) and Duty Cycle Adjust (pin 1) allow external adjustment of the PWM output signal. The Delay Adjust pin can be left floating for minimum delay to PWM mode (typically $18\mu s$) or a capacitor can be used to

set a longer delay time. A resistor, analog voltage, or a voltage from a D/A converter can be used to control the duty cycle of the PWM output. The D/A converter must be able to sink a current $2.75 \cdot I_{REF}$ ($I_{REF} = 1.3V/R_{FREQ}$).

Figure 2 illustrates a typical timing diagram with the Delay Adjust pin connected to a 3.9nF capacitor, the duty cycle set to 75%, and oscillator frequency set to 1kHz. See the "Delay Adjust" and "Duty Cycle Adjust" text for equations and further explanation. Ground (pin 4) must be connected to system ground for the DRV103 to function. This serves as the load current path to ground, as well as the DRV103 signal ground. The load (relay, solenoid, valve, etc.) should be connected between the supply (pin 5) and output (pin 6). For an inductive load, an external "flyback" diode is required, as shown in Figure 1. The diode serves to maintain continuous current flow in the inductive load during OFF periods of PWM operation. For remotely located loads, the external diode is ideally located next to the DRV103. The internal ESD clamp diode between the output and supply is not intended to be used as a "flyback diode." The Status OK Flag (pin 7) provides fault status for over-current and thermal shutdown conditions. This pin is active LOW with output voltage of typically +0.3V during a fault condition.
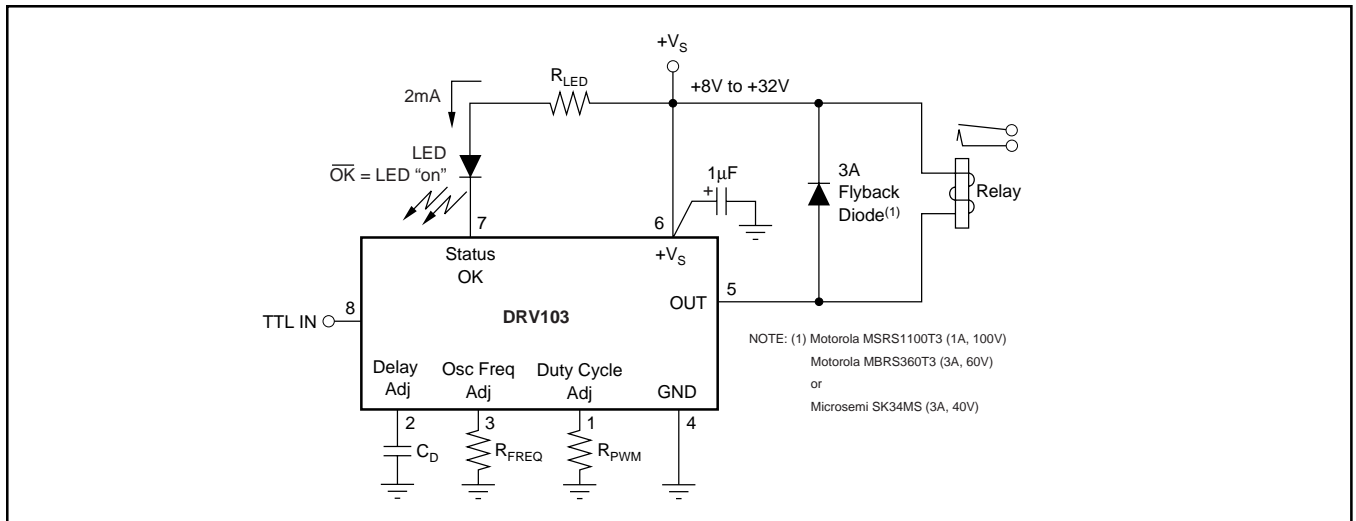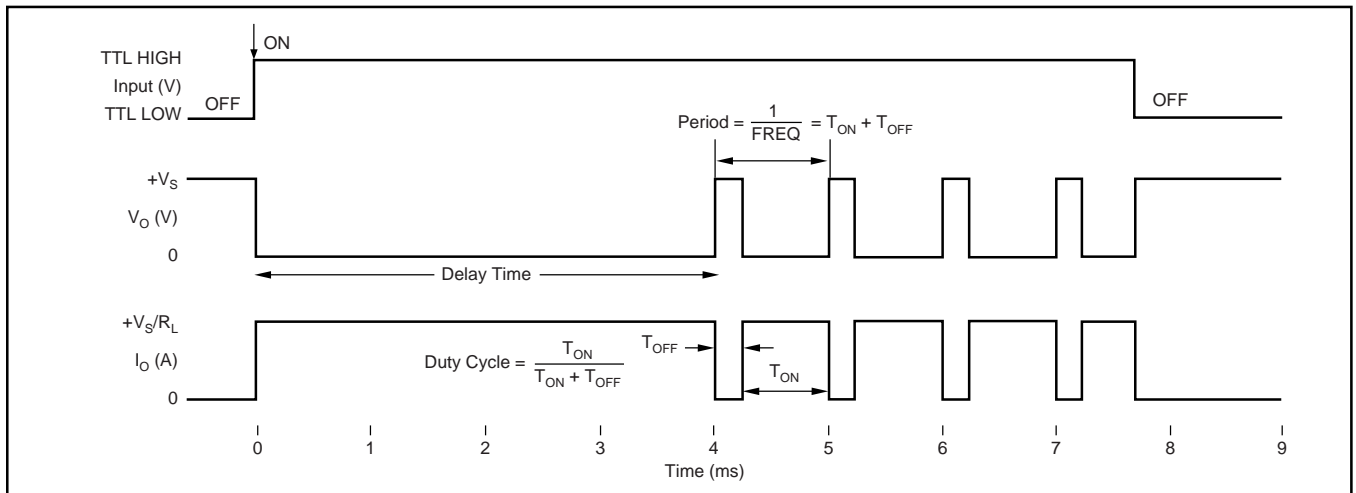

FIGURE 1. DRV103 Basic Circuit Connections.

FIGURE 2. Typical DRV103 Timing Diagram, with C_D = 3.9nF, OscFreq = 1kHz, and 75% Duty Cycle.

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TEXAS INSTRUMENTS

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APPLICATIONS INFORMATION

POWER SUPPLY

The DRV103 operates from a single +8V to +32V supply with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Performance Curves. The DRV103 supply voltage should be ≥ the supply voltage on the load.

ADJUSTABLE DELAY TIME (INITIAL 100% DUTY CYCLE)

A unique feature of the DRV103 is its ability to provide an initial constant DC output (100% duty cycle) and then switch to PWM mode output to save power. This function is particularly useful when driving solenoids that have a much higher pull-in current requirement than continuous hold requirement.

The duration of this constant DC output (before PWM output begins) can be externally controlled by a capacitor connected from Delay Adjust (pin 2) to ground according to the following equation:

$$\text{Delay Time} \approx C_D \bullet 10^6$$

(time in seconds, C_D in Farads $\bullet$ 1.1)

Leaving the Delay Adjust pin open results in a constant output time of approximately 18μs. The duration of this initial output can be reduced to less than 1μs by connecting the pin to 5V. Table I provides examples of delay times (constant output before PWM mode) achieved with selected capacitor values.

INITIAL CONSTANT OUTPUT DURATION	C_D
1μs	Pin 2 Tied to +5V
18μs	Pin 2 Open
110μs	100pF
1.1ms	1nF
11ms	10nF
110ms	100nF
1.1s	1μF
11s	10μF

TABLE I. Delay Adjust Times.

The internal Delay Adjust circuitry is composed of a 3μA current source and a 2.6V comparator, as shown in Figure 3. Thus, when the pin voltage is less than 2.6V, the output device is 100% ON (DC output mode).

OSCILLATOR FREQUENCY ADJUST

The DRV103 PWM output frequency can be easily programmed over a wide range by connecting a resistor (R_{FREQ}) between the Osc Freq Adj pin (pin 3) and ground. A range of 500Hz to 100kHz can be achieved with practical resistor values, as shown in Table II. Refer to "PWM Frequency vs R_{FREQ}" typical performance curve shown in Figure 4 for additional information. Although oscillator frequency operation below 500Hz is possible, resistors higher than 10M will be required. The pin becomes a very high impedance node and is, therefore, sensitive to noise pickup and PCB leakage currents if very high resistor values are used. Refer to Figure 3 for a simplified circuit of the frequency adjust input.

OSCILLATOR FREQUENCY (Hz)	R_{FREQ} (nearest 1% values) (Ω)
100k	47.5k
50k	100k
25k	205k
10k	523k
5k	1.07M
500	11.3M

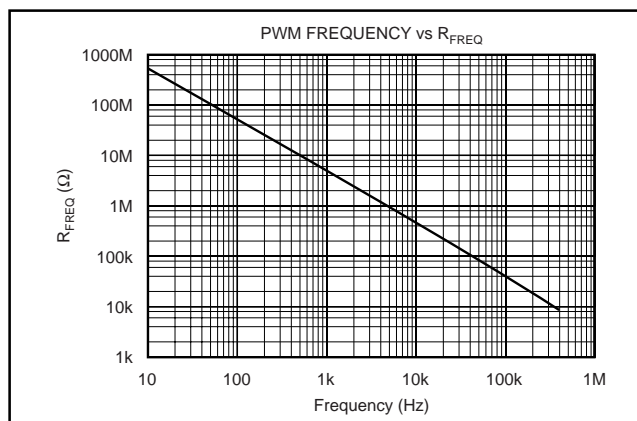TABLE II. Oscillator Frequency Resistance.

FIGURE 4. Using a Resistor to Program Oscillator Frequency.
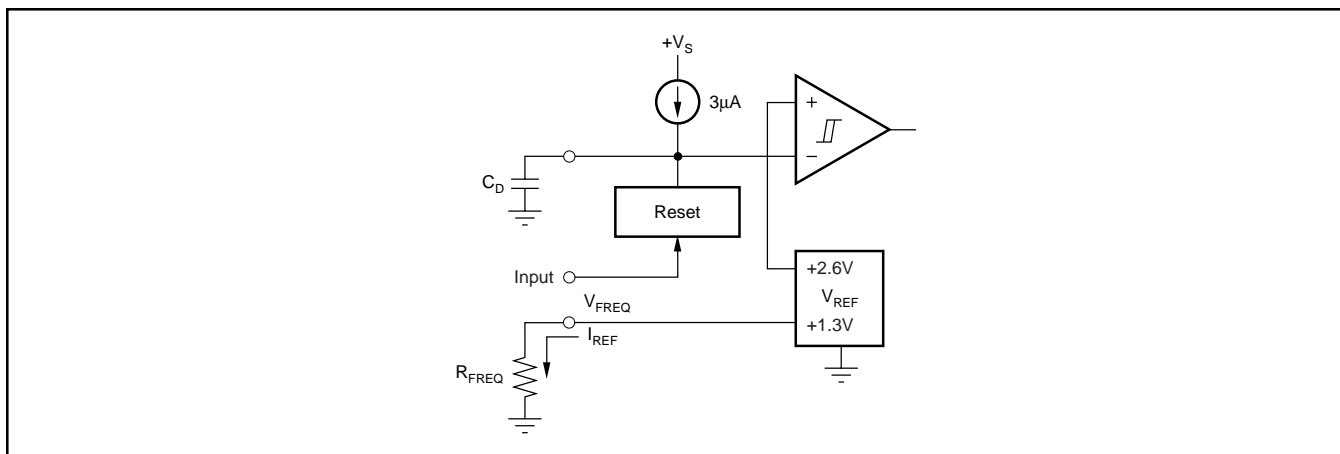$$R_{FREQ} \text{ (k}\Omega) = 6808417/F^{(1.0288)}$$

FIGURE 3. Simplified Delay Adjust and Frequency Adjust Inputs.

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The DRV103's adjustable PWM output frequency allows it to be optimized for driving virtually any type of load.

ADJUSTABLE DUTY CYCLE (PWM Mode)

The DRV103's externally adjustable duty cycle provides an accurate means of controlling power delivered to a load. Duty cycle can be set over a range of at least 10% to 90% with an external resistor, analog voltage, or the voltage output of a D/A converter. A low duty cycle results in reduced power dissipation in the load. This keeps the DRV103 and the load cooler, resulting in increased reliability for both devices.

Resistor Controlled Duty Cycle

Duty cycle is easily programmed by connecting a resistor (R_{PWM}) between the Duty Cycle Adjust pin (pin 1) and ground. High resistor values correspond to high duty cycles. Table III provides resistor values for typical duty cycles. Resistor values for additional duty cycles can be obtained from Figure 5. For reference purposes, the equation for calculating R_{PWM} is included in Figure 5.

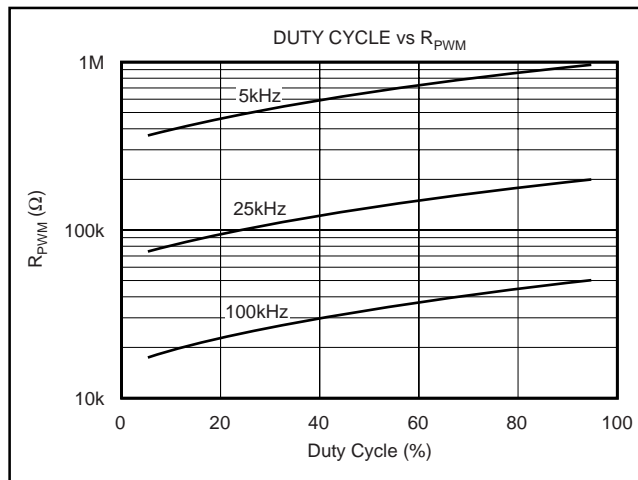| DUTY CYCLE	R_{PWM} (Nearest 1% Values)		
(%)	5kHz	25kHz	100kHz
5	374k	75k	16.9k
10	402k	80.6k	19.1k
20	475k	95.3k	22.6k
30	549k	110k	26.1k
40	619k	124k	29.4k
50	681k	137k	33.2k
60	750k	150k	37.4k
70	825k	165k	40.2k
80	887k	182k	44.2k
90	953k	196k	47.5k
95	1M	200k	49.9k

TABLE III. Duty Cycle Adjust Resistance.

FIGURE 5. Using a Resistor to Program Duty Cycle. At 25kHz: R_{PWM} (kΩ) = 67.46 + 1.41 • %DC.

A 100pF capacitor in parallel with R_{PWM} is recommended when switching a high load current to maintain a clean output switching waveform, as shown in Figure 6.
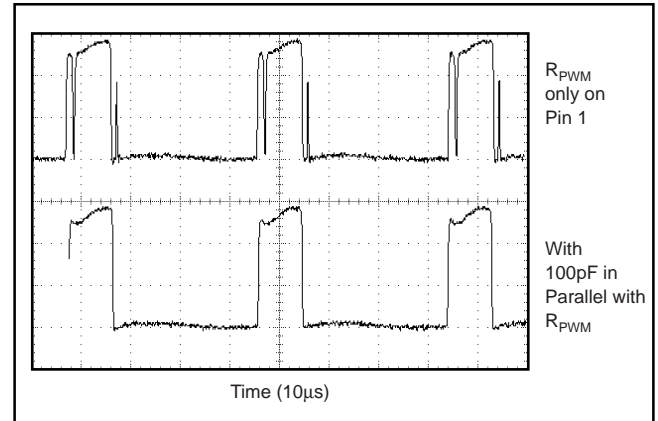

FIGURE 6. Output Waveform at High Load Current.

Voltage Controlled Duty Cycle

Duty cycle can also be programmed by an analog voltage, V_{PWM}. With $V_{PWM} \approx 3.56V$, duty cycle is about 90%. Decreasing this voltage results in decreased duty cycles. Table IV provides V_{PWM} values for typical duty cycles. The "Duty Cycle vs Voltage" typical performance curve for additional duty cycles is shown in Figure 7.
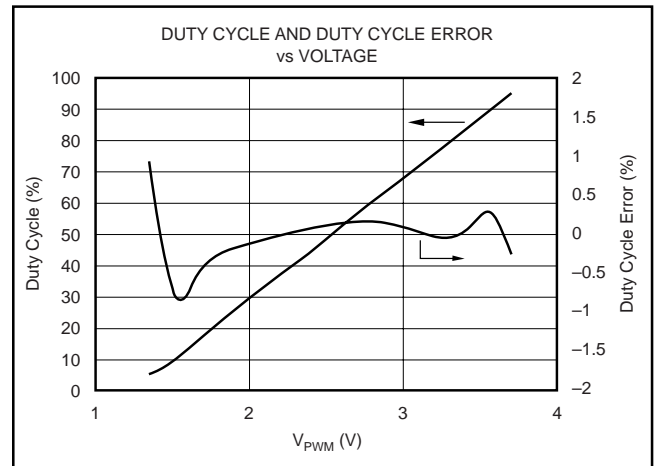

FIGURE 7. Using a Voltage to Program Duty Cycle. At V_S = 24V and F = 25kHz: V_{PWM} = 1.25 + 0.026 • %DC.

DUTY CYLE (%)	V_{PWM} (V)
5	1.344
10	1.518
20	1.763
40	2.283
60	2.788
80	3.311
90	3.561
95	3.705

TABLE IV. Duty Cycle Adjust Voltage.

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The Duty Cycle Adjust pin is internally driven by an oscillator frequency dependent current source and connects to the input of a comparator as shown in Figure 8. The DRV103's PWM adjustment is inherently monotonic. That is, a decreased voltage (or resistor value) always produces an increased duty cycle.
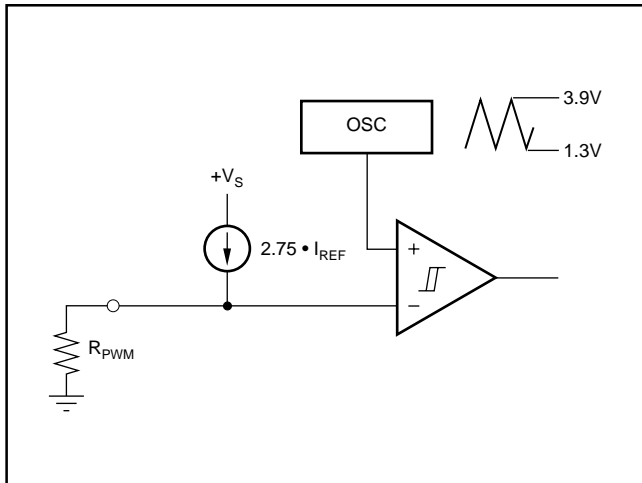

FIGURE 8. Simplified Duty Cycle Adjust Input.

STATUS FLAG

The OK Flag (pin 7) provides a fault indication for over-current and thermal shutdown conditions. During a fault condition, the Status OK Flag output is driven LOW (pin voltage typically drops to 0.3V). A pull-up resistor, as shown in Figure 9, is required to interface with standard logic. Figure 9 also gives an example of a non-latching fault monitoring circuit, while Figure 10 provides a latching version. The OK Flag pin can sink up to 10mA, sufficient to drive external logic circuitry, a reed relay, or an LED, as shown in Figure 11, to indicate when a fault has occurred. In addition, the OK Flag pin can be used to turn off other DRV103s in a system for chain fault protection.

Over Current Fault

An over-current fault occurs when the PWM peak output current is greater than approximately 3.75A. The OK flag is not latched. Since current during PWM mode is switched on and off, the OK flag output will be modulated with PWM timing (see OK flag waveforms in the Typical Performance Curves).

Avoid adding capacitance to pin 6 (Out) as it may cause momentary current limiting.

Over-Temperature Fault

A thermal fault occurs when the die reaches approximately 160°C, producing a similar effect as pulling the input low. Internal shutdown circuitry disables the output. The OK Flag is latched in the LOW state (fault condition) until the die has cooled to approximately 140°C.
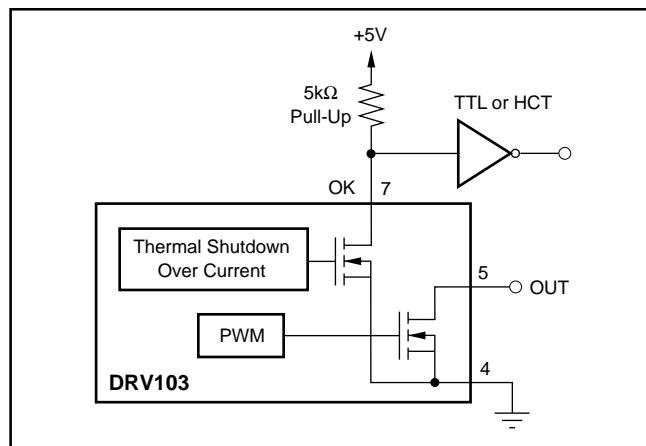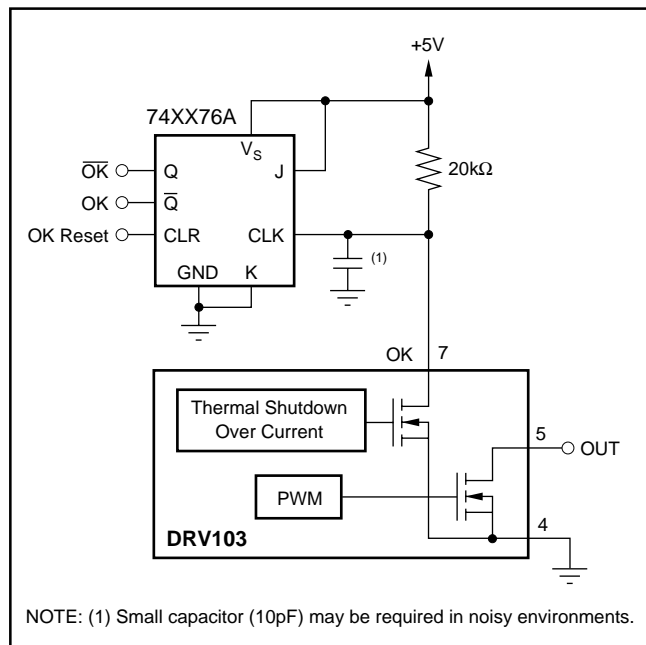

FIGURE 9. Non-Latching Fault Monitoring Circuit.

NOTE: (1) Small capacitor (10pF) may be required in noisy environments.
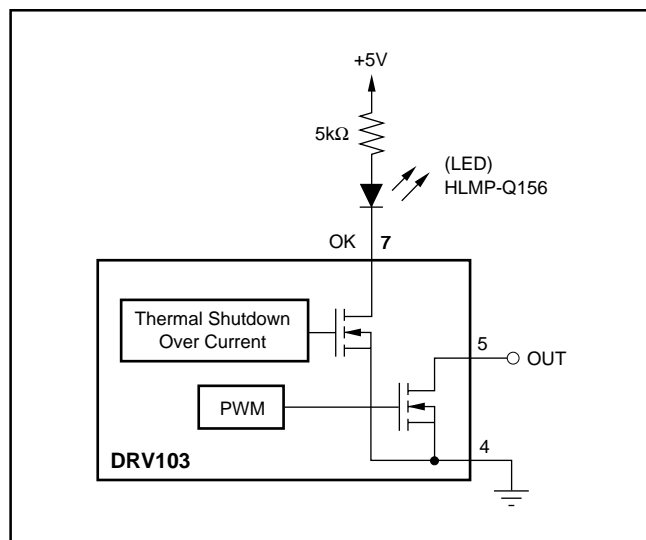
FIGURE 10. Latching Fault Monitoring Circuit.

FIGURE 11. LED to Indicate Fault Condition.

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PACKAGE MOUNTING

Figure 12 provides recommended PCB layouts for both the SO-8 (U) and the PowerPAD™ SO-8 (H) packages. Although the metal pad of the PowerPAD™ SO-8 (H) package is electrically connected to ground (pin 4), no current should flow in this pad. Do NOT use the exposed metal pad as a power ground connection or erratic operation will result. For lowest overall thermal resistance, it is best to solder the PowerPAD™ directly to a circuit board, as illustrated in Figure 13. Increasing the "heat sink" copper area improves heat dissipation. Figure 14 shows typical junction-to-ambient thermal resistance as a function of the PC board copper area.
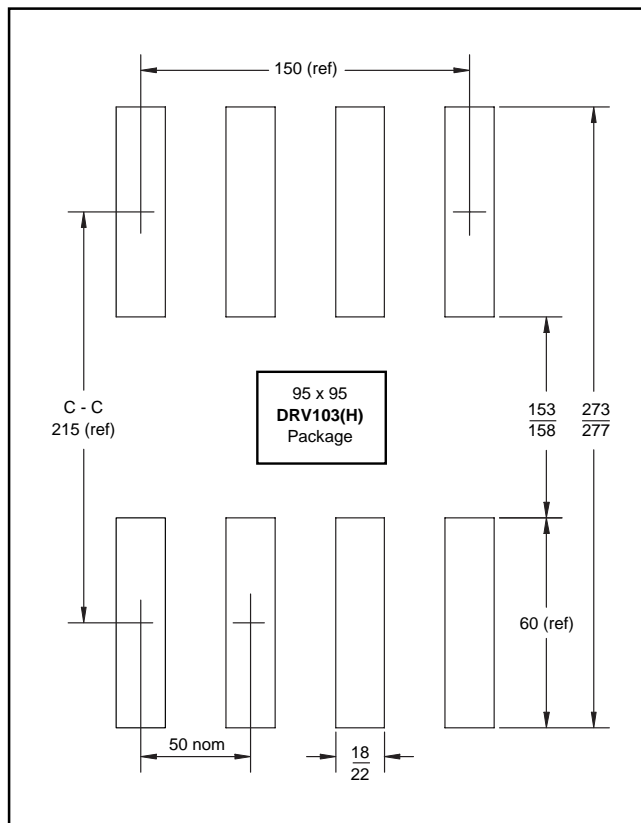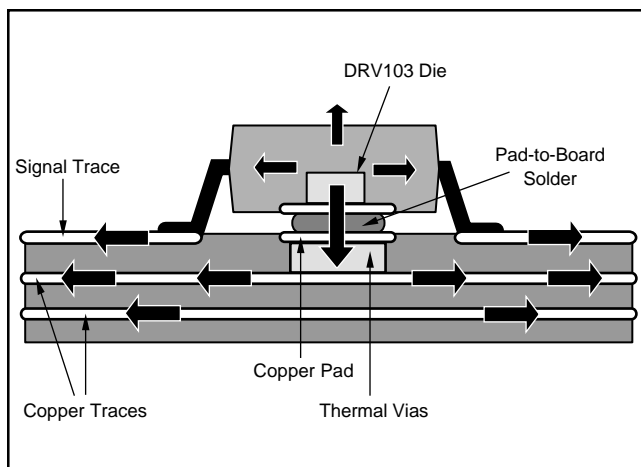

FIGURE 12. Recommended PCB Layout.

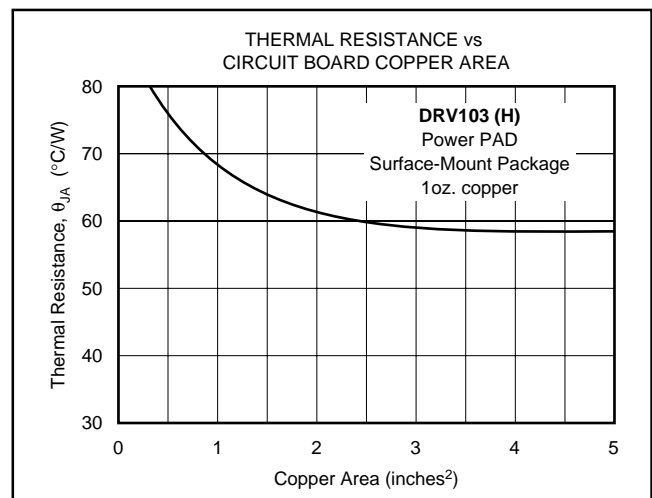FIGURE 13. PowerPAD Heat Transfer.

FIGURE 14. Heat Sink Thermal Resistance vs Circuit Board Copper Area.

POWER DISSIPATION

DRV103 power dissipation depends on power supply, signal, and load conditions. Power dissipation (P_D) is equal to the product of output current times the voltage across the conducting DMOS transistor times the duty cycle. Using the lowest possible duty cycle necessary to assure the required hold force can minimize power dissipation in both the load and in the DRV103. For low current, the output DMOS transistor on-resistance is 0.5Ω, increasing to 0.6Ω at high output current.

At very high oscillator frequencies, the energy in the DRV103's linear rise and fall times can become significant and cause an increase in P_D.

Application Bulletin SBFA002 at www.ti.com, explains how to calculate or measure power dissipation with unusual signals and loads.

THERMAL PROTECTION

Power dissipated in the DRV103 will cause its internal junction temperature to rise. The DRV103 has an on-chip thermal shutdown circuitry that protects the IC from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the driver but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 40°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

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The internal protection circuitry of the DRV103 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the DRV103 into thermal shutdown will degrade reliability.

HEAT SINKING

Most applications will not require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. However, junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the equation:

$$T_J = T_A + P_D\theta_{JA} \tag{1}$$

$$\text{where,} \quad \theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \tag{2}$$

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipated (W)

θ_{JC} = Junction-to-Case Thermal Resistance (°C/W)

θ_{CH} = Case-to-Heat Sink Thermal Resistance (°C/W)

θ_{HA} = Heat Sink-to-Ambient Thermal Resistance (°C/W)

θ_{JA} = Junction-to-Air Thermal Resistance (°C/W)

Using a heat sink significantly increases the maximum allowable power dissipation at a given ambient temperature.

The answer to the question of selecting a heat sink lies in determining the power dissipated by the DRV103. For DC output into a purely resistive load, power dissipation is simply the load current times the voltage developed across the conducting output transistor times the duty cycle. Other loads are not as simple. For further insight on calculating power dissipation, refer to Application Bulletin SBFA002 at www.ti.com. Once power dissipation for an application is known, the proper heat sink can be selected.

Heat Sink Selection Example

A PowerPAD™ SO-8 (H) package is dissipating 2W. The maximum expected ambient temperature is 35°C. Find the proper heat sink to keep the junction temperature below 125°C.

Combining Equations 1 and 2 gives:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CH} + \theta_{HA}) \tag{3}$$

T_J, T_A, and P_D are given. θ_{JC} is provided in the specification table, 16.7°C/W. θ_{CH} depends on heat sink size, area, and material used. A semiconductor's package type and mounting can also affect θ_{CH}. A typical θ_{CH} for a soldered-in-place PowerPAD™ SO-8 (H) package is 2°C/W. Now we can solve for θ_{HA}:

$$\theta_{HA} = \frac{T_J - T_A}{P_D} - \left(\theta_{JC} + \theta_{CH}\right)$$

$$\theta_{HA} = \frac{125°C - 35°C}{2W} - \left(16.7°C/W + 2°C/W\right) \tag{4}$$

$$\theta_{HA} = 26.3°C/W$$

To maintain junction temperature below 125°C, the heat sink selected must have a θ_{HA} less than 26.3°C/W. In other words, the heat sink temperature rise above ambient must be less than 52.6°C (26.3°C/W • 2W).

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower θ_{CA} ($\theta_{CH} + \theta_{HA}$) dramatically.

As mentioned earlier, once a heat sink has been selected, the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection.

RFI/EMI

Any switching system can generate noise and interference by radiation or conduction. The DRV103 is designed with controlled slew rate current switching to reduce these effects. By slowing the rise and fall times of the output to 0.3μs, much lower switching noise is generated.

Radiation from the DRV103-to-load wiring (the "antenna" effect) can be minimized by using "twisted pair" cable or by shielding. Good PCB ground planes are recommended for low noise and good heat dissipation. Refer to Bypassing section for notes on placement of the flyback diode.

BYPASSING

A 1μF tantalum bypass capacitor is adequate for uniform duty cycle control when switching loads of less than 0.5 amps. Larger bypass capacitors are required when switching high current loads. A 22μF tantalum capacitor is recommended for heavy-duty (3A) applications. It may also be desirable to run the DRV103 and the load on separate power supplies at high load currents. Near the absolute maximum supply voltage of 40V, bypassing is especially critical. In the event of a current overload, the DRV103 current limit responds in microseconds, dropping the load current to zero. With inadequate bypass, energy stored in the supply line inductance can lift the supply sufficiently to exceed voltage breakdown with catastrophic results.

Place the flyback diode at the DRV103 end when driving long (inductive) cables to a remotely located load. This minimizes RFI/EMI and helps protect the output DMOS transistor from breakdown caused by dI/dt transients. Fast rectifier diodes such as epitaxial silicon or Schottky types are recommended as flyback diodes.
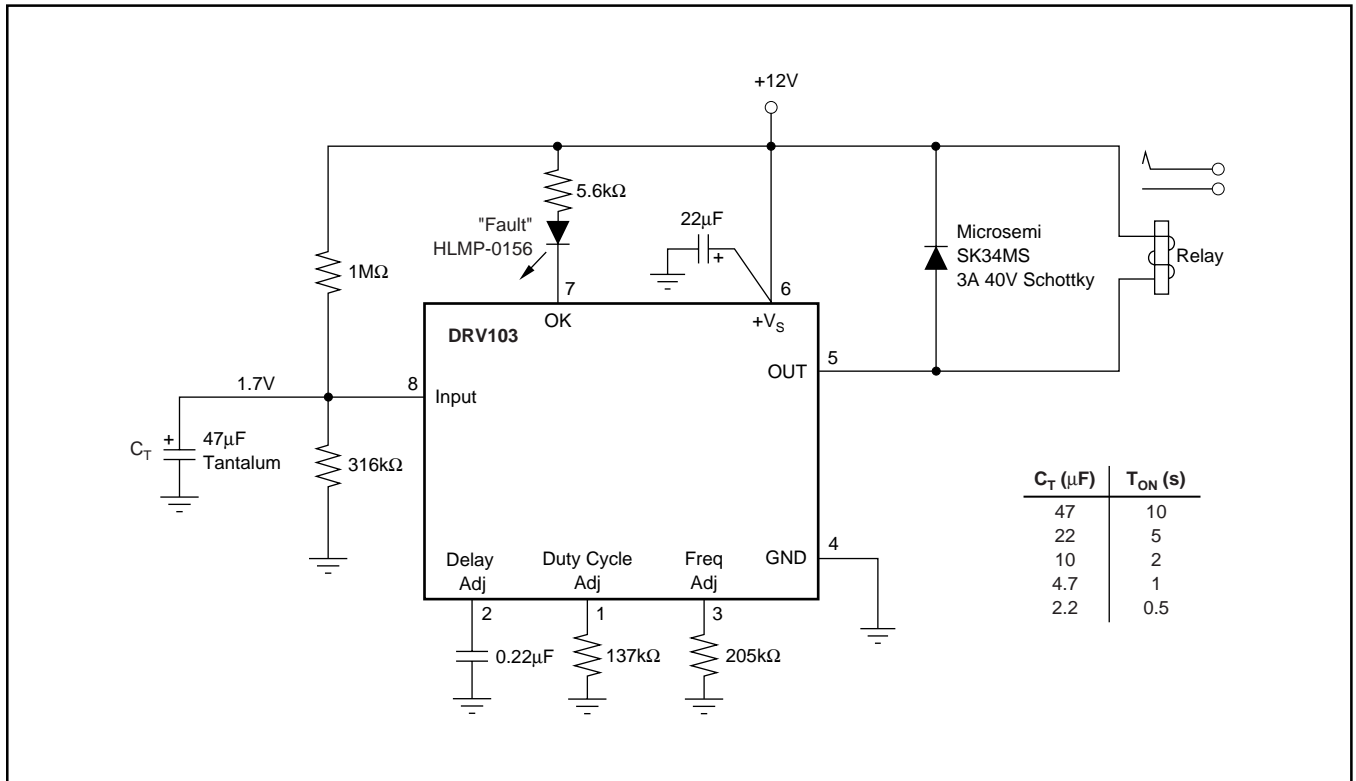
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APPLICATIONS CIRCUITS

C_T (μF)	T_{ON} (s)
47	10
22	5
10	2
4.7	1
2.2	0.5

FIGURE 15. Time Delay Relay Driver.
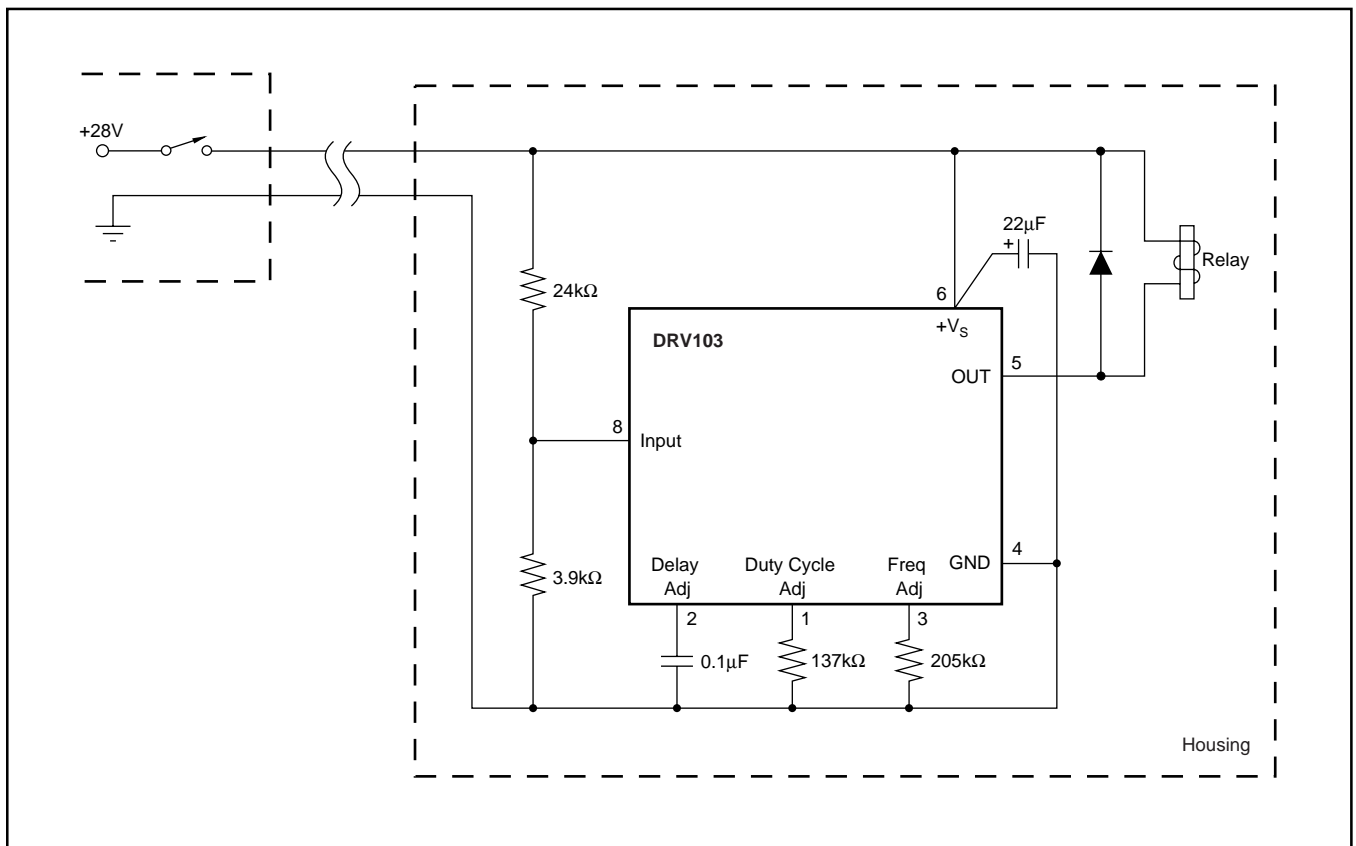
FIGURE 16. Remotely Operated Solenoid Valve or Relay.

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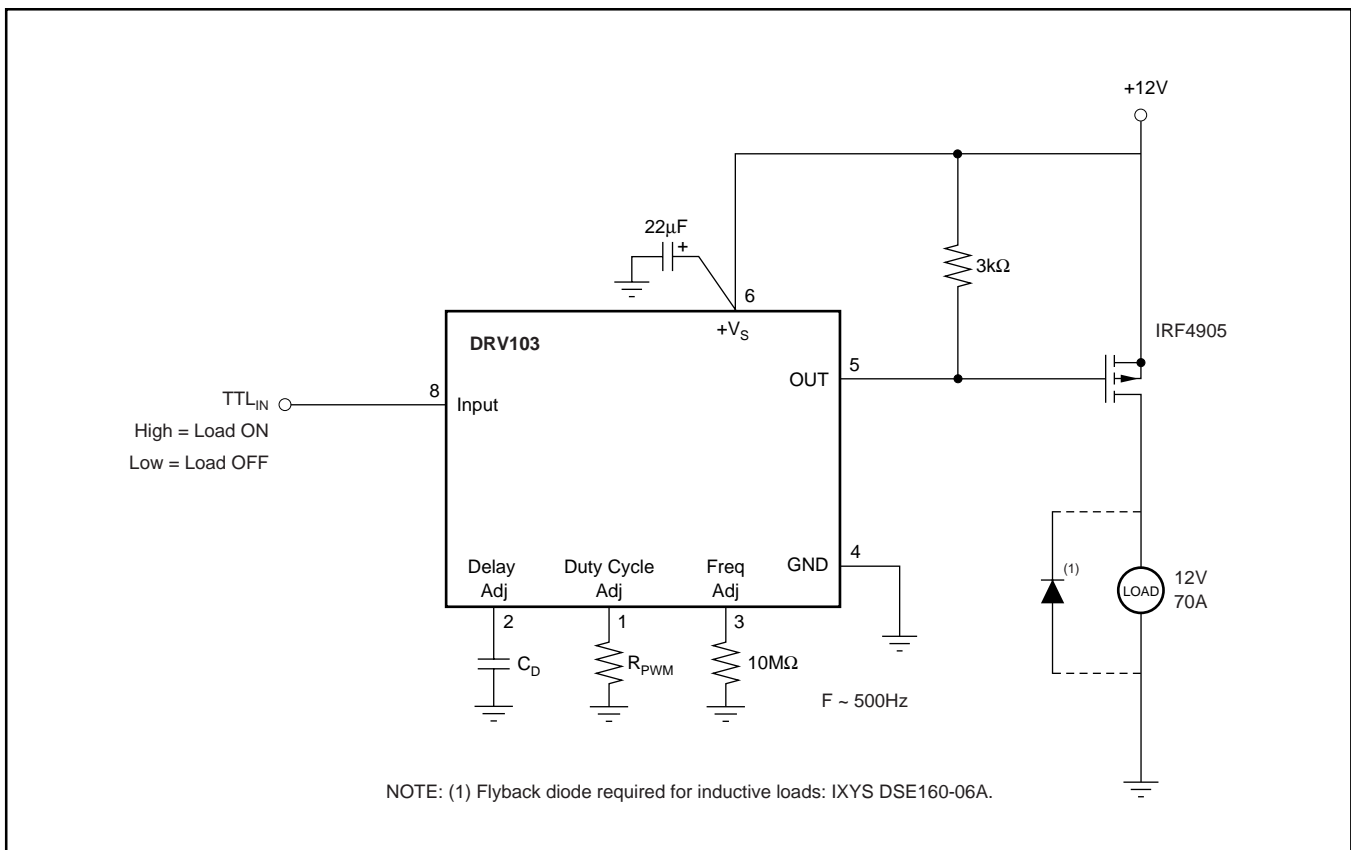
FIGURE 17. High Power High Side Driver.

FIGURE 18. Linear Valve Driver.

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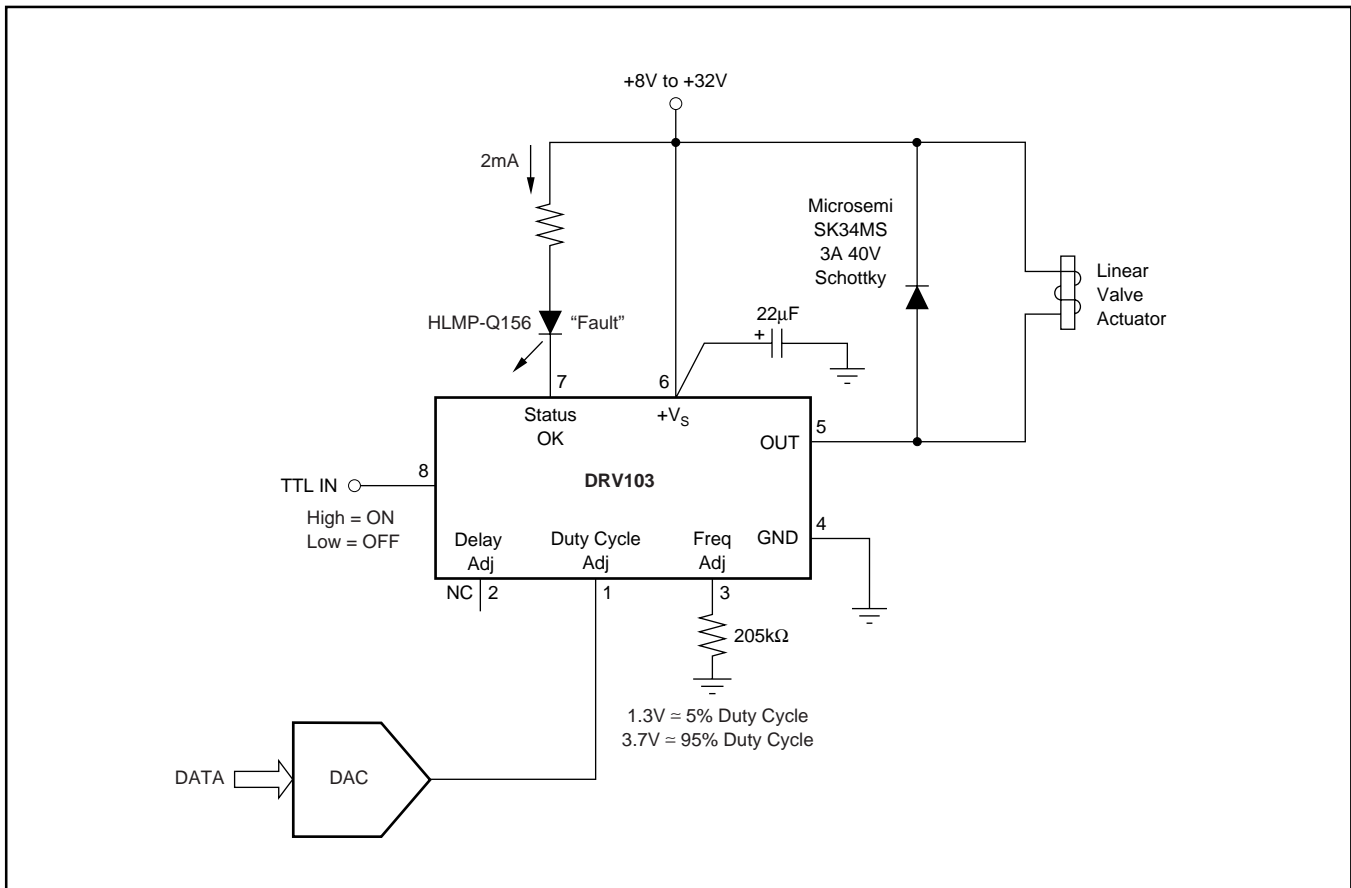
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