# MDS105AL

## CosMOS 5-Port 10/100 Mbps Ethernet Switch

DS5441 ISSUE 1 February 2001

**Ordering Information**
DS105AL

## 1 Features

- 4 10/100Mbps auto-negotiating RMII ports
- 1 10/100Mbps auto-negotiating MII/serial port (port 4) that can be used as a WAN uplink or as a 5th port
- External $I^2C$ EEPROM for power-up configuration
  - Default mode allows operation without external EEPROM
- Up to 4 port-based VLANs
- Full wirespeed layer 2 switching on all ports
- Internal 1k MAC address table
  - Auto address learning
  - Auto address aging
- Leading edge QoS capabilities provided based on 802.1p and IP TOS/DS field
  - 2 queues per output port
  - Packet scheduling based on Weighted Round-Robin (WRR) and Weighted Random Early Detection/Drop (WRED)
  - Without flow control can drop packets during congestion using WRED
  - 2 levels of packet drop provided
- Supports both Full/Half duplex ports
- Supports external parallel port for configuration updates
- Port 3 can be used to mirror traffic from the other 3 ports (0-2)
- Provides port-based prioritization of packets on up to 2 ports (0-1)
  - Input ports are defined to be high or low priority
  - Allows explicit identification of IP Phone ports
- Ports 0 & 1 can be trunked to provide a 200Mbps link to another switch or server
- Utilizes a single low-cost external SSRAM for buffer memory
  - 256k bytes or 512k bytes (1 chip)
- Flow Control capabilities
  - Provides back pressure for half-duplex
  - 802.3x flow control for full-duplex
- Special power-saving mode for inactive ports
- Ability to support WinSock2.0 and Windows2000 smart applications
- Transmit delay control capabilities
  - Provides maximum delay guarantee (<1ms)
  - Supports mixed voice-data networks
- Optimized pin-out for easy board layout
- Packaged in a 208 PQFP

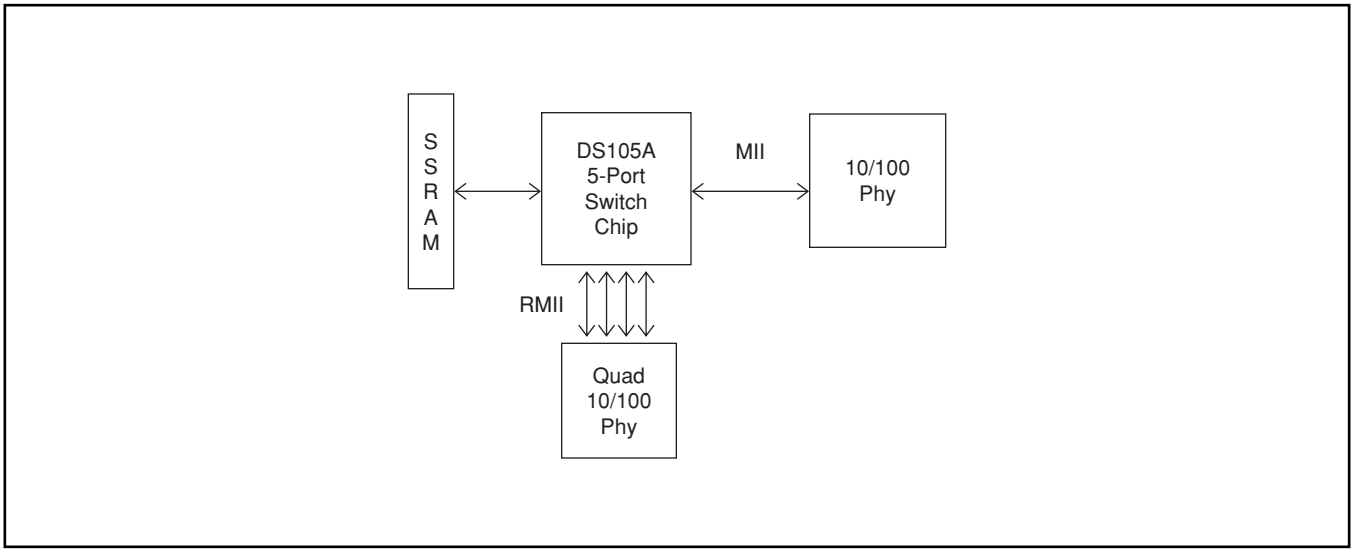



**Figure 1 - System Block Diagram**

## 2 Description

CoSMOS MDS105AL is a fully integrated 5-port Ethernet switch designed to support the low-cost requirements of unmanaged switch applications. The MDS105AL provides features that are normally not associated with plug-and-play technology, while not requiring an external processor to facilitate their utilization.

CoSMOS MDS105AL begins operating immediately at power-up, learning addresses automatically, and forwarding packets at full wire speed to any of its eight output ports or the XLink expansion port. The default configuration allows operation without using an external EEPROM.

With an EEPROM to configure the device at power up, however, the MDS105AL provides flexible features: port trunking, port mirroring, port-based VLANs, and Quality of Service (QoS) capabilities that are usually associated only with managed switches.

The built-in intelligence of CoSMOS MDS105AL allows it to recognize and offer packet prioritization using the CoSMOS QoS scheme. Packets are prioritized based upon their layer 2 VLAN priority tag or the layer 3 Type-Of-Service/Differentiated Services (TOS/DS) field. This priority can be defined as transmit and/or drop priority.

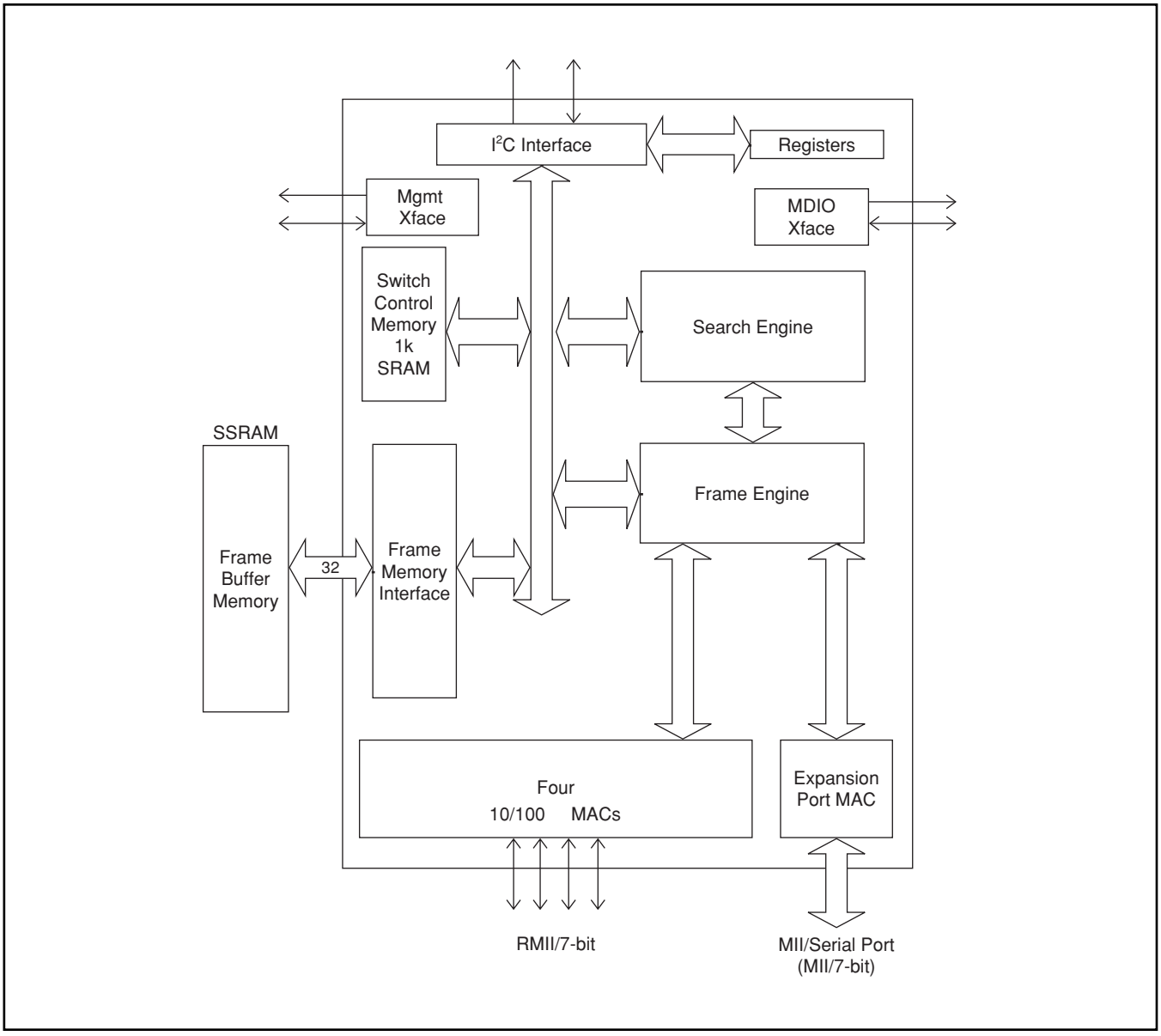
CoSMOS MDS105AL can be used to create an 8 port unmanaged switch with one WAN router port by connecting a CPU (ARM or MPC 850) to the additional MII port (port 8). The only external components needed are the physical layer transceivers and a single SSRAM, resulting in a low total system cost.

Designed to support the requirements of converging networks, the MDS105AL utilizes a power conserving architecture. To further enhance this power management, the chip automatically detects when a switch port is not being utilized, and turns off the logic associated with that port, thereby saving power and reducing the current load on the switch power supply.

Operating at 66 MHz internally, and with a 66 MHz interface to the external SSRAM, the MDS105AL sustains full wire-speed switching on all five ports.

The chip is packaged in a small 208 pin Plastic Quad Flat-Pak (PQFP) package.

## 3 MDS105AL Block Diagram



## 4 Functional Operation

CoSMOS MDS105AL is designed to provide a cost effective layer 2 switching solution, using technology from the XF2080 family to offer a highly integrated product for the unmanaged, Differentiated Services (DS) ready, Ethernet switch market.

Five 10/100 Media Access Controllers (MAC) provide the protocol interface. These MACs perform the required packet checks to ensure that each packet that is provided to the Frame Engine has met all the IEEE 802.1 standards. Each MAC supports half duplex “back pressure,” and full duplex 802.3x “PAUSE” Flow Control.

Data packets longer than 1518 (1522 with VLAN tag) bytes and shorter than 64 bytes are dropped, and the MDS105AL is designed to support minimum interframe gaps between incoming packets.

The Frame Engine (FE) is the primary packet buffering and forwarding engine within the MDS105AL. As such, the FE controls the storage of packets into and out of the external frame buffer memory, keeps track of frame buffer availability, and schedules packet transmissions. While packet data is being buffered, the FE extracts the necessary information from each packet header and sends it to the Search Engine for processing. Search results returned to the FE initiate the scheduling of packet transmission. When a packet is chosen for transmission, the FE reads the packet from external buffer memory and places it in the output FIFO of the output port.

## 5 Address Learning and Aging

CoSMOS MDS105AL is able to begin address learning and packet forwarding shortly after power up is completed. The Search Engine examines the contents of its internal Switch Database Memory for each valid packet that is received on a MDS105AL input port.

Unknown source and destination MAC addresses are detected when the Search Engine does not find a match within its database. These unknown source MAC addresses are learned by creating a new entry in the switch database memory, and storing the necessary resulting information in that location. Subsequent searches to a learned destination MAC address will return the new contents of that MAC Control Table (MCT) entry.

After each source address search the MCT entry aging flag is updated. MCT entries that have not been accessed during a user configurable time period (1 to 67,108 seconds) will be removed. This aging time period can be configured using the 16-bit value stored in the registers MAC Address Aging Timer Low and High (AGETIME_LOW, AGETIME_HIGH). The aging period is defined as the bit concatenation of AGETIME_HIGH with AGETIME_LOW, multiplied by 1024 ms. For example, if AGETIME_LOW = 25, and AGETIME_HIGH = 01 (in hexadecimal), then the concatenated value 125 is equal to decimal 293. Multiplying 293 by 1024 ms, we determine that the corresponding aging time is 300 ms. In fact, 300 ms is the default aging time for the MDS105AL.

The aging of all MCT entries is checked once during each time period. If the MCT entry has not been exercised before the end of the next time period, it will be deleted.

## 6 Quality of Service

The MDS105AL applies the CoSMOS architecture to provide new Quality of Service (QoS) capabilities for unmanaged switch applications. Similar to the QoS capabilities of the XF2080 chipset members, CoSMOS MDS105AL offers two transmit queues per output port.

The Frame Engine (FE) manages the output transmission queues for all MDS105AL ports. Once the destination address search is complete, and the switch decision is sent back to the FE, the packet is inserted into the appropriate output queue. Whether the packet is inserted into a high or low priority queue is determined by either the VLAN tag information or the Type of Service/Differentiated Services (TOS/DS) field in the IP header. Either of these priority fields can be used to select the transmission priority (as per the USE_TOS bit in the FCR register). The mapping of the priority field values into either the high or low priority queue can be configured using the MDS105AL configuration registers AVPM and TOSPM.

If the system uses the TOS/DS field to prioritize packets, there are two choices regarding which bits of the TOS/DS field are used. Bits [0:2] of the TOS byte (known as the IP precedence field) or bits [3:5] of the TOS byte (known as the Delay/Throughput Reliability, DTR, field) can be used to resolve the transmission queue priority. Either bit group, [0:2] or [3:5], can also be used to resolve packet drop precedence, as per bits 6 and 7 of the register FCBST.

CoSMOS MDS105AL utilizes Weighted Round Robin (WRR) to schedule packets for transmission. To enable CoSMOS' intelligent QoS scheduling capabilities requires the use of an external EEPROM to change the default register configurations.

Weighted Round Robin is an efficient method to ensure that each of the transmission queues receives at least a minimum service level. With two output transmission queues, the MDS105AL will transmit X packets from the high priority queue before transmitting a single packet from the low priority queue. The MDS105AL allows the designer to set the high priority weight X to a value between 1 and 15. If both queues contain packets, and the high priority weight is set to the value 4, then the MDS105AL will transmit 4 high priority packets before transmitting each low priority packet.

The MDS105AL also employs a proprietary mechanism to ensure the timely delivery of high priority packets. When the latency of high priority packets reaches a threshold, the MDS105AL will override the WRR weights and transmit only high priority packets until the high priority packet delays are below the threshold. This threshold limit is 1 ms (last-in-first-out). The MDS105AL's proprietary scheduling algorithm is also designed to push low priority traffic through the device faster, if necessary to unclog congested queues.

Loading the appropriate values into the configuration registers enables the QoS scheduling capabilities of the MDS105AL. QoS for packet transmission is enabled by performing the following four steps:

1. Select the TOS/DS or VLAN Priority Tag field as the decision-maker for IP packet scheduling. The selection is made using bit 7 of the Flooding Control Register (FCR).
   - FCR[7] = 0: Use VLAN Priority Tag field to determine the transmission priority, if this Tag field exists.
   - FCR[7] = 1: Use TOS/DS field for IP packet priority resolution.
2. Select which TOS/DS subfield to use as the decision-maker for packet transmission priority if the TOS/DS field was selected in step 1. The selection is made using bit 6 of the FCB Buffer Low Threshold Register (FCBST).
   - FCBST[6] = 0: Use DTR subfield to resolve the transmission priority.
   - FCBST[6] = 1: Use IP precedence subfield[1] to resolve the transmission priority.
3. Enable QoS using bit 5 of the Transmission Scheduling Control Register (AXSC). Set the transmission queue weight for the high priority queue using bits 0 to 3.
4. Create the mapping from the value in the TOS/DS or VLAN Priority Tag field to the corresponding high or low priority output queue. The mapping is created using the VLAN Priority Map (AVPM) and TOS Priority Map (TOSPM) registers.

Note that for half duplex operation, the priority queues[2] must be enabled using bit 7 in the Transmission Scheduling Control (AXSC) register to use QoS scheduling.

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1. IP precedence and DTR subfields are referred to as TOS/DS[0:2] and TOS/DS[3:5] in the IP TOS/DS byte.
2. In Half Duplex mode, QoS scheduling unctions are disabled by default.

When QoS and flow control are enabled, CoSMOS MDS105AL will utilize enhanced WRR to schedule packet transmission, and will use either back pressure or 802.3X flow control to handle buffer congestion. When QoS is enabled and flow control is disabled, the MDS105AL will utilize enhanced WRR to schedule packet transmission, and will use Weighted Random Early Detection/Drop (WRED) to drop random packets in order to handle buffer congestion. Because of WRED, only a few packet flows are slowed down while the remaining see no impact from the network traffic congestion.

WRED is a method of handling traffic congestion in the absence of flow control mechanisms[3]. When flow control is enabled, all devices that are connected to a switch node that is exercising flow control are effectively unable to transmit, including nodes that are not directly responsible for the congestion problem. This inability to transmit during flow control periods would wreak havoc with voice packets, or other high priority packet flows, and therefore flow control is not recommended for networks that mix voice and data traffic.

WRED allows traffic to continue flowing into ports on a switch, and randomly drops packets with different probabilities based upon each packet's priority markings. As the switch congestion increases, the probability of dropping an incoming packet increases, and as congestion decreases, the probability of dropping an incoming packet decreases. Not surprisingly, packets designated high-drop are sacrificed with higher odds during congestion than packets designated low-drop. The following table summarizes the WRED operation of the MDS105AL. It lists the buffer thresholds at which each drop probability takes effect.

3. Flow control, of course, provides the advantage of not dropping packets. However, its primary disadvantage is that a flow-controlled port may experience head-of-line blocking. This means that if even 1 packet is destined to a congested output port, then all other packets originating from the same source may, in the worst case, be delayed – even if these other packets have uncongested destinations. On the other hand, WRED may cause some packet loss, but with no such head-of-line blocking problem. Which method of handling traffic congestion should be chosen will depend on the application.

The WRED packet drop capabilities of the MDS105AL are enabled by performing the following four steps:

1. Select the TOS/DS or VLAN Tag field as the decision-maker for dropping packets. The selection is made using bit 7 of the Flooding Control Register (FCR).
   - FCR[7] = 0: Use VLAN Priority Tag field to resolve the drop level, if this field exists.
   - FCR[7] = 1: Use TOS/DS field for IP packet drop level resolution.
2. Select which TOS/DS Tag subfield to use for dropping packets provided that the TOS/DS field was selected in step 1. The selection is made using bit 7 of the FCB Buffer Low Threshold Register (FCBST).
   - FCBST[7] = 0: Use DTR subfield to resolve the drop precedence.
   - FCBST[7] = 1: Use IP precedence subfield to resolve the drop precedence.
3. Create the mapping from the values in the TOS DS or VLAN Tag field to the packet flags representing high or low drop precedence. The mapping is created using the VLAN Discard Map (AVDM) and TOS Discard Map (TOSDM) registers.
4. Make sure that the desired ports are flow control disabled, using the ECR1Px registers.

Note that to apply the WRED QoS function of the MDS105AL, flow control must be disabled.

## 6.1 A Few Examples

- **No QoS Scheduling Desired At All.** The default setting for the MDS105AL is no QoS scheduling at all. Packets are transmitted using a simple first-in-first-out (FIFO) approach, without the reordering that would result from prioritization. All destinations use 1 queue only. QoS scheduling can be disabled for the entire chip using AXSC[5].
- **No QoS Scheduling Desired for Half-Duplex Ports.** It is possible to disable QoS for half-duplex ports in the MDS105AL. Indeed, this is the default setting, because it is difficult to assure quality of service for half- duplex ports, which tend to experience unpredictable delay. All destinations configured as half-duplex use 1 transmission queue only in this setting. QoS scheduling can be disabled for all half-duplex ports using AXSC[7].
- **QoS Scheduling for Some Destinations, But Not Others.** The MDS105AL does not support this feature. The three options offered are: (a) all ports are QoS-enabled, (b) no ports are QoS-enabled, and (c) only full-duplex ports are QoS-enabled. Of course, the MDS105AL will still exhibit single-queue scheduling at a port if all packets destined for it are marked with a single transmission priority.
- **No Flow Control Desired.** It is possible to disable flow control for the entire chip, regardless of the individual port settings. During congestion, some packets will be lost. This capability is located in AXSC[6].
- **Flow Control Desired for Some Sources, But Not Others.** By configuring each port separately using bit 0 in the ECR1Px registers, one may enable flow control for some ports, but not others. Flow control cannot be globally disabled in AXSC[6] if this function is to be achieved. At a congested destination, an incoming packet from a flow control enabled source will trigger a flow control message sent back to that source. On the other hand, an incoming packet from a flow control disabled source may or may not be dropped, as per WRED, but will never trigger flow control.
- **Scheduling vs. Dropping.** Using the configuration registers in the MDS105AL, as in earlier examples, a port may or may not have flow control enabled, and a port may or may not have QoS scheduling enabled. All four combinations are permissible parameter settings, and which one is chosen depends on application.

In one common application, suppose voice, critical data, and web traffic packets originate from the same set of input ports, and are destined for the same set of output ports. The MDS105AL's enhanced WRR scheduling can be used to ensure a delay bound for the voice packets. Furthermore, because we want to guarantee that web traffic congestion does not block critical data or voice, we must disable flow control and use WRED to intelligently drop packets.

On the other hand, if the goal were file transfer without any packet dropping, one would enable the MDS105AL's flow control function, which halts incoming traffic when the system is congested. QoS scheduling can be disabled, both because flow control may make quality of service unpredictable, and because, in any case, delay is not critical in this application.

## 6.2 Port-Based Prioritization

Some applications may require an explicit prioritization of packets based upon the port the packet originates from. Defining specific ports of a switch to be IP Phone ports is a specific example

that makes use of CoSMOS MDS105AL's ability to assign default priorities to ports.

The MDS105AL can be configured to provide specific priority definitions on up to four ports (ports 0 – 3). These user defined port priorities override the packet priority markings (VLAN tag or TOS/DS), and the new priority is applied to all packets that enter the switch from that port. These port priority definitions are configured in the Port Priority (PTPRI) register. There are two bits for each of the four ports that can support port-based priorities. The EN bit allows the designer to turn on port priorities for each port, and the P bit allows the designer to select either high (1) or low (0) transmission priority for all packets that enter the switch through that port.

When port priorities are enabled, the remaining ports will provide QoS based upon the VLAN Tag or TOS DS field mappings in the configuration registers. Only those ports that have port priorities enabled will override the priority mappings.

## 7 Buffer Management

CoSMOS MDS105AL stores each input packet into the external frame buffer memory while determining the destination the packet is to be forwarded to. The total number of packets that can be stored in the frame buffer memory depends upon the size of the external SSRAM that is utilized. For a 256 KB SSRAM the MDS105AL can buffer 170 packets. For a 512 KB SSRAM the MDS105AL can buffer 340 packets.

In order to provide good quality of service characteristics, the MDS105AL must carefully allocate the available buffer space. Such careful allocation can be accomplished using the external EEPROM to load the appropriate values into the MDS105AL configuration registers. The Low Drop Precedence Buffer Threshold (LPBT) register assures that traffic designated as low-drop actually receives reserved buffer space. The designer can set the minimum number of buffers reserved for low-drop unicast traffic, by setting this register with a value between 0 and 255. Unreserved buffers are treated as shared, and are accessible to all types of incoming traffic.

To set the maximum number of buffers permitted for all multicast packets, use the Multicast Buffer Control Register (MBCR). Unlike the LPBT register, the MBCR register does not define a reserved area of buffer memory, but instead provides a bound on the number of multicast packets that can be buffered at any one time.

During operation the MDS105AL will continuously monitor the amount of frame buffer memory that is available, and when the unused buffer space falls below a designer configurable threshold, the MDS105AL will initiate flow control if enabled or WRED if not. This threshold is set using the FCB Buffer Low Threshold (FCBST) register.MDS105AL CoSMOS

## 8 Virtual LANs

CoSMOS MDS105AL provides the designer the ability to define a single port-based Virtual LAN (VLAN) for each of the five ports. This VLAN is individually defined for each port using the Port Control Registers (ECR1Px[6:4]). Bits [6:4] allow the designer to define a VLAN ID (value between 0 – 3) for each port.

When packets arrive at an input of the MDS105AL, the search engine will determine the VLAN ID for that port, and then determine which of the other ports are also members of that VLAN by matching their assigned VLAN ID values. The packet will then be transmitted to each port with the same VLAN ID as the source port.

## 9 Port Trunking

Port trunking allows the designer to configure the MDS105AL, such that ports 0 and 1 are defined as a single logical port. This provides a 200 Mbps link to a switch or server utilizing two 100 Mbps ports in parallel.

Ports 0 and 1 can be trunked by pulling the TRUNK_EN pin to the high state. In this mode, the source MAC addresses of all packets received from the trunk are checked against the MCT database to ensure that they have a port ID of 0 or 1. Packets that have a port ID other than 0 and 1 will cause the MDS105AL to learn the new MAC address for this port change.

On transmission, the trunk port is determined by hashing the source and destination MAC addresses. This provides a mapping between each MAC address and an associated trunk port. Subsequent packets with the same MAC address will always utilize the same trunk port.

The MDS105AL also provides a safe fail-over mode for port trunking. If one of the two ports goes down, as identified by the port's link status signal, then the MDS105AL will switch all traffic over to the remaining port in the trunk. Thus, the trunk link is maintained, albeit at a lower effective bandwidth.

## 10 Port Mirroring

Utilizing the four port mirroring control pins provides the ability to enable or disable port mirroring, select which of the remaining 3 ports is to be mirrored, and choose whether the receive or transmit data is being mirrored. The control for this function is shown in the following table.

| Mirrored Port | Mirror_Control [3] | Mirror Control [2] | Mirror_Control [1] | Mirror_Control [0] |
|---|---|---|---|---|
| **Port 0 RCV** | 1 | 0 | 0 | 0 |
| **Port 0 XMT** | 0 | 0 | 0 | 0 |
| **Port 1 RCV** | 1 | 0 | 0 | 1 |
| **Port 1 XMT** | 0 | 0 | 0 | 1 |
| **Port 2 RCV** | 1 | 1 | 1 | 0 |
| **Port 2 XMT** | 0 | 1 | 1 | 0 |
| **Disabled** | 0/1 | 1 | 1 | 1 |

When enabled, port mirroring will allow the user to monitor traffic going through the switch on output Port 3. If the port mirroring control pins MIR_CTL[3:0] are left floating, the MDS105AL will operate with the port mirroring function disabled.

When port mirroring is enabled, the user must configure Port 3 to operate in the same mode as the port it is mirroring (autonegotiation, duplex, speed, flow control).

## 11 Power Saving Mode in MAC

CoSMOS MDS105AL was designed to be power efficient. When the internal MAC sections detect that the external port is not receiving or transmitting packets, it will shut off and conserve power. When new packet data is loaded into the output transmit FIFO of a MAC in power saving mode, the MAC will return to life and begin operating immediately.

When the MAC is in power saving mode and new packet data is received on the RMII, the MAC will return to life and receive data normally into the receive FIFO. This wakeup occurs when the MAC sees the Carrier Sense Data Valid (CRS_DV) signal asserted.

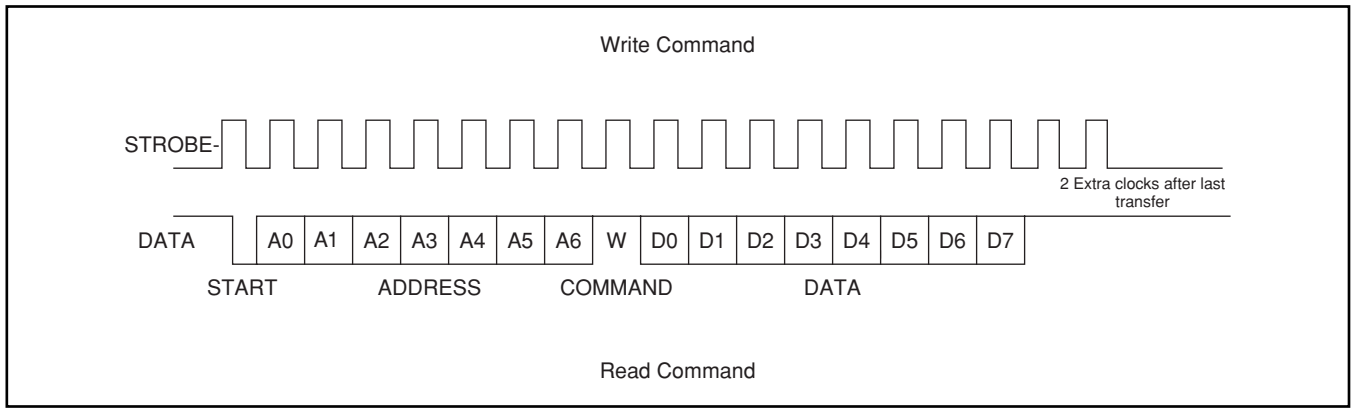
Using this method, the switch will turn off all MAC sections during periods when there is no network activity (at night, for example), and save power. For large networks this power savings could be large. To achieve the maximum power efficiency, the designer should use a physical layer transceiver that utilizes “Wake-On-LAN” technology.

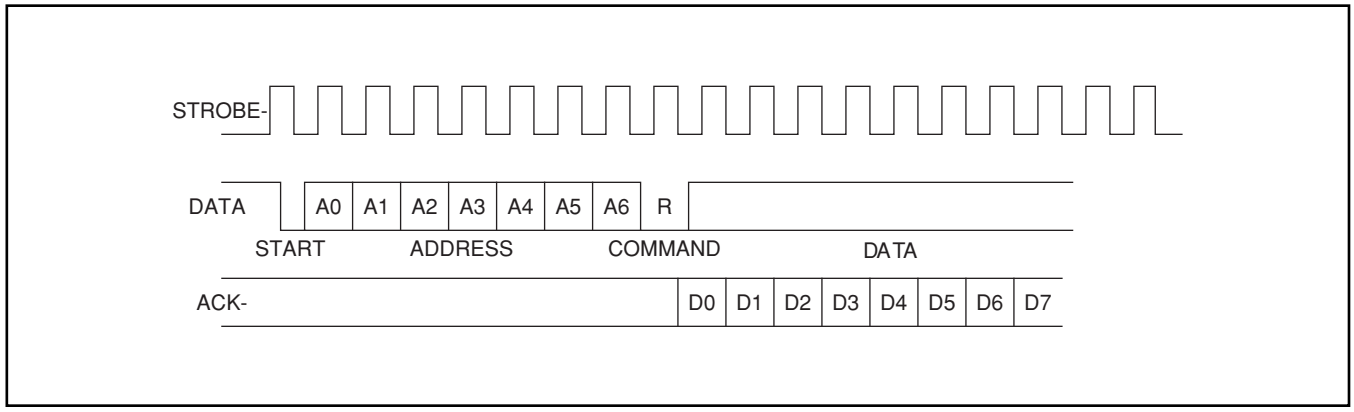
## 12 EEPROM $I^2C$ Interface

A simple 2 wire serial interface is provided to allow the configuration of CoSMOS MDS105AL from an external EEPROM. The MDS105AL utilizes a 1K bit EEPROM with an I 2 C interface.

## 13 Management Interface

CoSMOS MDS105AL uses a standard parallel port interface to provide external CPU access to the internal registers. This parallel interface is composed of 3 pins: DATA0, STROBE, and ACK. The DATA0 pin provides the address and data content input to the MDS105AL, while the ACK pin provides the corresponding output to the external CPU. The STROBE pin is provided as the clock for both serial data streams. Any of the MDS105AL internal registers can be modified through this parallel port interface[4].




Each management interface transfer consists of four parts:

1. A START pulse – occurs when DATA is sampled high when STROBE is rising followed by DATA being sampled low when STROBE falls.
2. Register address strobed into DATA0 pin, using the high level of the STROBE pin.
3. Either a read or write command (see waveforms above).
4. Data to be written provided on DATA0, or data to be read provided on ACK.

Any command can be aborted in the middle by sending an ABORT pulse to the MDS105AL. An ABORT pulse occurs when DATA is sampled low and STROBE is rising, followed by DATA being sampled high when STROBE falls.

4. The 3-bit parallel interface is not “parallel” in the usual sense of the word; it is actually a synchronous serial architecture. However, the MDS105AL management interface adheres to IEEE 1284 parallel port standards.

## 14 Configuration Register Definitions

The CoSMOS MDS105AL registers can be accessed via the parallel interface and/or the $I^2C$ interface. Some registers are only accessible through the parallel interface. The access method for each register is listed in the individual register definitions. Each register is 8 bits wide.

### 14.1 GCR - Global Control Register

- Access: parallel interface, Write Only
- Address: h30

| | | |
|---|---|---|
| Bit [0] | Save configuration into EEPROM | (Default = 0) |
| Bit [1] | Save configuration into EEPROM and reset system | (Default = 0) |
| Bit [2] | Start Built-In Self-Test (BIST) | (Default = 0) |
| Bit [3] | Reset system | (Default = 0) |

### 14.2 DCR - Device Status and Signature Register

- Access: parallel interface, Read Only
- Address: h31

| | |
|---|---|
| Bit 0 | Busy writing configuration from $I^2C$ |
| Bit 1 | Busy reading configuration from $I^2C$ |
| Bit 2 | Built-In Self-Test (BIST) in progress |
| Bit 3 | RAM error during BIST |
| Bits [7:6] | Revision number |

### 14.3 DA – DA Register

- Access: parallel interface, Read Only
- Address: h36

Returns 8-bit value DA (hexadecimal) if the parallel port connection is good. Otherwise, returns some other value indicating failure.

### 14.4 MBCR – Multicast Buffer Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h00

| | | | |
|---|---|---|---|
| Bits [7:0] | MAX_CNT_LMT | Maximum number of multicast frames allowed to be buffered inside the device at any one time | (Default = 1F) |

## 14.5 FCBST – FCB Buffer Low Threshold

- Access: parallel interface and $I^2C$, Read/Write
- Address: h01

| | | | |
|---|---|---|---|
| Bits [5:0] | BUF_LOW_TH | Buffer Low Threshold – the number of free buffers below which flow control or WRED is triggered | (Default = 1F) |
| Bit 6 | | Use IP precedence subfield (TOS[0:2]) for Transmission Priority | (Default = 0) |
| Bit 7 | | Use IP precedence subfield (TOS[0:2]) for Drop Level | (Default = 0) |

Note that, for Bits 6 and 7, Default = 0 means to use TOS[3:5].

## 14.6 LPBT – Low Drop Precedence Buffer Threshold

- Access: parallel interface and $I^2C$, Read/Write
- Address: h02

| | | | |
|---|---|---|---|
| Bits [7:0] | LOW_DROP_CNT | Number of frame buffers reserved for low-drop traffic | (Default 3F) |

## 14.7 FCR – Flooding Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h03

| | | | |
|---|---|---|---|
| Bits [3:0] | U2MR | Maximum number of flooded frames allowed within any time interval indicated by TimeBase bits (violations are discarded) | (Default = 8) |
| Bits [6:4] | TimeBase | 000 = 100 µs 001 = 200 µs<br>010 = 400 µs 011 = 800 µs<br>100 = 1.6 µs 101 = 3.2 µs<br>110 = 6.4 µs 111 = 100 µs | (Default = 000) |
| Bit [7] | USE_TOS | Use TOS instead of VLAN priority for IP packet | (Default = 0) |

## 14.8 AVTCL – VLAN TYPE CODE REGISTER LOW

- Access: parallel interface and $I^2C$, Read/Write
- Address: h04

| | | | |
|---|---|---|---|
| Bits [7:0] | VLANType_LOW | Lower 8 bits of VLAN type code | (Default 00) |

## 14.9 AVTCH – VLAN Type Code Register High

- Access: parallel interface and $I^2C$, Read/Write
- Address: h05

| | | | |
|---|---|---|---|
| Bits [7:0] | VLANType_HIGH | Upper 8 bits of VLAN type code | (Default 81) |

## 14.10 AVPM – VLAN Priority Map

- Access: parallel interface and $I^2C$, Read/Write
- Address: h06

Map VLAN tag into 2 transmit queues (0 = low priority, 1 = high priority).

| | | |
|---|---|---|
| Bit 0 | Mapped priority of tag value 0 | (Default 0) |
| Bit 1 | Mapped priority of tag value 1 | (Default 0) |
| Bit 2 | Mapped priority of tag value 2 | (Default 0) |
| Bit 3 | Mapped priority of tag value 3 | (Default 0) |
| Bit 4 | Mapped priority of tag value 4 | (Default 0) |
| Bit 5 | Mapped priority of tag value 5 | (Default 0) |
| Bit 6 | Mapped priority of tag value 6 | (Default 0) |
| Bit 7 | Mapped priority of tag value 7 | (Default 0) |

## 14.11 AVDM – VLAN Discard Map

- Access: parallel interface and $I^2C$, Read/Write
- Address: h07

Map VLAN tag into frame discard levels (0 = low drop, 1 = high drop).

| | | |
|---|---|---|
| Bit 0 | Frame discard for tag value 0 | (Default 0) |
| Bit 1 | Frame discard for tag value 1 | (Default 0) |
| Bit 2 | Frame discard for tag value 2 | (Default 0) |
| Bit 3 | Frame discard for tag value 3 | (Default 0) |
| Bit 4 | Frame discard for tag value 4 | (Default 0) |
| Bit 5 | Frame discard for tag value 5 | (Default 0) |
| Bit 6 | Frame discard for tag value 6 | (Default 0) |
| Bit 7 | Frame discard for tag value 7 | (Default 0) |

## 14.12 TOSPM – TOS Priority Map

- Access: parallel interface and $I^2C$, Read/Write
- Address: h08

Map TOS field in IP packet into 2 transmit queues (0 = low priority, 1 = high priority).

| | | |
|---|---|---|
| Bit 0 | Mapped priority when TOS is 0 | (Default 0) |
| Bit 1 | Mapped priority when TOS is 1[5] | (Default 0) |
| Bit 2 | Mapped priority when TOS is 2 | (Default 0) |
| Bit 3 | Mapped priority when TOS is 3 | (Default 0) |
| Bit 4 | Mapped priority when TOS is 4 | (Default 0) |
| Bit 5 | Mapped priority when TOS is 5 | (Default 0) |
| Bit 6 | Mapped priority when TOS is 6 | (Default 0) |
| Bit 7 | Mapped priority when TOS is 7 | (Default 0) |

## 14.13 PTPRI – Port Priority

- Access: parallel interface and $I^2C$, Read/Write
- Address: h09

Enable and configure port-based priorities for ports 0, 1, 2, and 3

| | | | |
|---|---|---|---|
| Bit 0 | EN0 | Port 0: Enable; 1 = enabled | (Default 0) |
| Bit 1 | P0 | Port 0: Priority; 1 = high, 0 = low | (Default 0) |
| Bit 2 | EN1 | Port 1: Enable; 1 = enabled | (Default 0) |
| Bit 3 | P0 | Port 1: Priority; 1 = high, 0 = low | (Default 0) |
| Bit 7:4 | Reserved | | |

## 14.14 TOSDM – TOS Discard Map

- Access: parallel interface and $I^2C$, Read/Write
- Address: h0A

Map TOS into frame discard levels (0 = low drop, 1 = high drop).

| | | |
|---|---|---|
| Bit 0 | Frame discard when TOS is 0 | (Default 0) |
| Bit 1 | Frame discard when TOS is 1 | (Default 0) |
| Bit 2 | Frame discard when TOS is 2 | (Default 0) |
| Bit 3 | Frame discard when TOS is 3 | (Default 0) |
| Bit 4 | Frame discard when TOS is 4 | (Default 0) |
| Bit 5 | Frame discard when TOS is 5 | (Default 0) |
| Bit 6 | Frame discard when TOS is 6 | (Default 0) |
| Bit 7 | Frame discard when TOS is 7 | (Default 0) |

5. TOS = 1 means the appropriate 3-bit TOS subfield is “001.

## 14.15 AXSC – Transmission Scheduling Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h0B

| | | |
|---|---|---|
| Bits [3:0] | Transmission Queue Service Weight for high priority queue | (Default F) |
| Bit [5] | Global Quality of Service Enable | (Default 0) |
| Bit [6] | Global Flow Control Disable – if 1, flow control is disabled globally; if 0, each port's flow control settings are separately configurable | (Default 0) |
| Bit [7] | Half Duplex Priority Enable – if 0, priority is disabled for all half duplex ports; if 1, priority is enabled unless AXSC[5] = 0 | (Default 0) |

## 14.16 MII_OP0 – MII Register Option 0

- Access by parallel interface and $I^2C$, Read/Write
- Address: h0C

Permits a non-standard address for the Phy Status Register. When low and high Address bytes are 0, the MDS105AL will use the standard address.

| | | |
|---|---|---|
| Bits [7:0] | Low order address byte | (Default 00) |

## 14.17 MII_OP1 – MII Register Option 1

- Access: parallel interface and $I^2C$, Read/Write
- Address: h0D

| | | |
|---|---|---|
| Bits [7:0] | High order address byte | (Default 00) |

## 14.18 AGETIME_LOW – MAC Address Aging Timer Low

- Access: parallel interface and $I^2C$, Read/Write
- Address: h0E

| | | |
|---|---|---|
| Bits [7:0] | Low byte of the MAC address aging timer. | (Default 25) |

## 14.19 AGETIME_HIGH – MAC Address Aging Timer High

- Access: parallel interface and $I^2C$, Read/Write
- Address: h0F

| | | |
|---|---|---|
| Bits [7:0] | High byte of the MAC address aging timer. | (Default 01) |
| | The aging time is based on the following formula: {AGETIME_HIGH, AGETIME_LOW} x 1024 ms | The default setting provides a 300 second aging time. |

## 14.20 ECR1P0 – Port 0 Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h10

| | | | |
|---|---|---|---|
| Bits [3:0] | Port Mode | | (Default 0000) |
| Bit [3] | | 1 – Force configuration based on Bits [2:0]<br>0 – Autonegotiate and advertise based on Bits [2:0] | |
| Bit [2] | | 1 – 10 Mbps<br>0 – 100 Mbps | |
| Bit [1] | | 1 – Half Duplex<br>0 – Full Duplex | |
| Bit [0] | | 1 – Flow Control Off<br>0 – Flow Control On | |
| Bits [6:4] | PVID | Port-based VLAN ID | (Default 000) |
| Bit [7] | Reserved | | |

## 14.21 ECR1P1 – Port 1 Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h11

| | | | |
|---|---|---|---|
| Bits [3:0] | Port Mode | | (Default 0000) |
| Bit [3] | | 1 – Force configuration based on Bits [2:0]<br>0 – Autonegotiate and advertise based on Bits [2:0] | |
| Bit [2] | | 1 – 10 Mbps<br>0 – 100 Mbps | |
| Bit [1] | | 1 – Half Duplex<br>0 – Full Duplex | |
| Bit [0] | | 1 – Flow Control Off<br>0 – Flow Control On | |
| Bits [6:4] | PVID | Port-based VLAN ID | (Default 000) |
| Bit [7] | Reserved | | |

## 14.22 ECR1P2 – Port 2 Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h12

| | | | |
|---|---|---|---|
| Bits [3:0] | Port Mode | | (Default 0000) |
| Bit [3] | | 1 – Force configuration based on Bits [2:0]<br>0 – Autonegotiate and advertise based on Bits [2:0] | |
| Bit [2] | | 1 – 10 Mbps<br>0 – 100 Mbps | |
| Bit [1] | | 1 – Half Duplex<br>0 – Full Duplex | |
| Bit [0] | | 1 – Flow Control Off<br>0 – Flow Control On | |
| Bits [6:4] | PVID | Port-based VLAN ID (Default 000) | |
| Bit [7] | Reserved | | |

## 14.23 ECR1P3 – Port 3 Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h13

| | | | |
|---|---|---|---|
| Bits [3:0] | Port Mode | | (Default 0000) |
| Bit [3] | | 1 – Force configuration based on Bits [2:0]<br>0 – Autonegotiate and advertise based on Bits [2:0] | |
| Bit [2] | | 1 – 10 Mbps<br>0 – 100 Mbps | |
| Bit [1] | | 1 – Half Duplex<br>0 – Full Duplex | |
| Bit [0] | | 1 – Flow Control Off<br>0 – Flow Control On | |
| Bits [6:4] | PVID | Port-based VLAN ID | (Default 000) |
| Bit [7] | Reserved | | |

## 14.24 ECR1P4 – Port 4 Control Register

- Access: parallel interface and $I^2C$, Read/Write
- Address: h14

| | | | |
|---|---|---|---|
| Bits [3:0] | Port Mode | | (Default 0000) |
| Bit [3] | | 1 – Force configuration based on Bits [2:0]<br>0 – Autonegotiate and advertise based on Bits [2:0] | |
| Bit [2] | | 1 – 10 Mbps<br>0 – 100 Mbps | |
| Bit [1] | | 1 – Half Duplex<br>0 – Full Duplex | |
| Bit [0] | | 1 – Flow Control Off<br>0 – Flow Control On | |
| Bits [6:4] | PVID | Port-based VLAN ID | (Default 000) |
| Bit [7] | Reserved | | |

## 14.25 FC_0 – Flow Control Byte 0

- Access: parallel interface and $I^2C$, Read/Write
- Address: h19

The flow control hold time parameter is the length of time a flow control message is effectual (i.e. halts incoming traffic) after being received. The hold time is measured in units of “slots,” the time it takes to transmit 64 bytes at wire speed. The default setting is 32 slots, or for a 100 Mbps port, approximately 164 ms.

| | | |
|---|---|---|
| Bits [7:0] | Flow control hold time byte 0 | (Default 20) |

## 14.26 FC_1 – Flow Control Byte 1

- Access: parallel interface and $I^2C$, Read/Write
- Address: h1A

| | | |
|---|---|---|
| Bits [7:0] | Flow control hold time byte 1 | (Default 00) |

## 14.27 FC_2 – Flow Control CRC Byte 0

- Access: parallel interface and $I^2C$, Read/Write
- Address: h1B

| | | |
|---|---|---|
| Bits [7:0] | Flow control frame CRC byte 0 | (Default E5) |

## 14.28 FC_3 – Flow Control CRC Byte 1

- Access: parallel interface and $I^2C$, Read/Write
- Address: h1C

| | | |
|---|---|---|
| Bits [7:0] | Flow control frame CRC byte 1 | (Default DE) |

## 14.29 FC_4 – Flow Control CRC Byte 2

- Access: parallel interface and $I^2C$, Read/Write
- Address: h1D

| | | |
|---|---|---|
| Bits [7:0] | Flow control frame CRC byte 2 | (Default 3F) |

## 14.30 FC_5 – Flow Control CRC Byte 3 (Address H1E)

- Access: parallel interface and $I^2C$, Read/Write
- Address: h1E

| | | |
|---|---|---|
| Bits [7:0] | Flow control frame CRC byte 3 | (Default 76) |

## 14.31 DMARH, DMARL, DTCR, DTST

These test registers are used for internal silicon testing only.

## 15 CoSMOS MDS105AL Pin Descriptions

| | | |
|---|---|---|
| Note: | # | Active low signal |
| | I | Input signal |
| | S | Input signal with Schmitt-Trigger |
| | O | Output signal |
| | OD | Open-Drain driver |
| | I/O | Input & Output signal |
| | SL | Slew Rate Controlled |
| | D | Pulldown |
| | U | Pullup |
| | 5 | 5V Tolerance |

| Pin No(s). | Symbol | Type | Name & Functions |
|---|---|---|---|
| **Frame Buffer Memory Interface** | | | |
| 201,200,199,197,196, 195,193,192,191,190, 188,187,186,185,183, 182,181,179,178,177, 176,174,173,172,170, 169,168,167,165,164, 163,161 | L_D[31:0] | I/O, U, SL | Databus to Frame Buffer Memory |
| 203,151,158,160, 10,9,8,6,5,4,2,1,208, 206,205,204,150, | L_A[18:2] | I/O, U, SL | Address pins for buffer memory |
| 153 | L_CLK | O | Frame Buffer Memory Clock |
| 155 | L_WE# | O, SL | Frame Buffer Memory Write Enable |
| 156 | L_OE# | O | Frame Buffer Memory Output Enable |
| 157 | L_ADSC# | O, SL | |
| **MII Management Interface** | | | |
| 120 | M_MDC | O | MII Management Data Clock |
| 122 | M_MDIO | I/O, U | MII Management Data I/O |
| **I2C Interface (Serial EEPROM Interface)** | | | |
| 123 | SCL | O, U, 5 | I2C Data Clock |
| 124 | SDA | I/O, U, OD, 5 | I2C Data I/O |
| **Parallel Port Management Interface** | | | |
| 127 | STROBE | I, U, S, 5 | |
| 128 | DATA0 | I, U, 5 | Data Pin |
| 129 | ACK | O, U, OD, 5 | |
| **Port 0 RMII Interface** | | | |
| 24,23 | M0_RXD[1:0] | I, U | Port 0 Receive Data |
| 22 | M0_CRS_DV | I, D | Port 0 Carrier Sense and Data Valid |
| 21,20 | M0_TXD[1:0] | O | Port 0 Transmit Data |

| Pin No(s). | Symbol | Type | Name & Functions |
|---|---|---|---|
| 19 | M0_TXEN | O | Port 0 Transmit Enable |
| **Port 1 RMII Interface** | | | |
| 31,30 | M1_RXD[1:0] | I, U | Port 1 Receive Data |
| 29 | M1_CRS_DV | I, D | Port 1 Carrier Sense and Data Valid |
| 28,27 | M1_TXD[1:0] | O | Port 1 Transmit Data |
| 26 | M1_TXEN | O | Port 1 Transmit Enable |
| **Port 2 RMII Interface** | | | |
| 79,78 | M2_RXD[1:0] | I, U | Port 2 Receive Data |
| 77 | M2_CRS_DV | I, D | Port 2 Carrier Sense and Data Valid |
| 76,75 | M2_TXD[1:0] | O | Port 2 Transmit Data |
| 74 | M2_TXEN | O | Port 2 Transmit Enable |
| **Port 3 RMII Interface** | | | |
| 86,85 | M3_RXD[1:0] | I, U | Port 3 Receive Data |
| 84 | M3_CRS_DV | I, D | Port 3 Carrier Sense and Data Valid |
| 83,82 | M3_TXD[1:0] | O | Port 3 Transmit Data |
| 81 | M3_TXEN | I, U | Port 3 Transmit Enable |
| **Port 4 MII Interface** | | | |
| 105,104,103,102 | M4_RXD[3:0] | I, U | Port 4 Receive Data |
| 113,112,111,110 | M4_TXD[3:0] | O | Port 4 Transmit Data |
| 109 | M4_TXEN | O | Port 4 Transmit Enable |
| 97 | M4_RXDV | I, D | Port 4 Receive Data Valid |
| 100 | M4_RXCLK | I, U | Port 4 Receive Clock |
| 107 | M4_TXCLK | I/O, U | Port 4 Transmit Clock |
| 114 | M4_LINK | I, U | Port 4 Link Status |
| 116 | M4_SPEED | I/O, U | Port 4 Speed Select (100Mb = 1) |
| 115 | M4_DUPLEX | I, U | Port 4 Full-Duplex Select (half-duplex = 0) |
| 98 | M4_COL | I, U | Port 4 Collision Detect |
| **Port 4 Serial Interface** | | | |
| 102 | S4_RXD | I, U | Port 4 Serial Receive Data |
| 100 | S4_RXCLK | I, U | Port 4 Serial Receive Clock |
| 97 | S4_CRS_DV | I, D | Port 4 Serial Carrier Sense and Data Valid |
| 110 | S4_TXD | O | Port 4 Serial Transmit Data |
| 107 | S4_TXCLK | I | Port 4 Serial Transmit Clock |
| 109 | S4_TXEN | O | Port 4 Serial Transmit Enable |
| 98 | S4_COL | I, U | Port 4 Serial Collision Detect |
| 114 | S4_LINK | I, U | Port 4 Link Status |
| 115 | S4_DUPLEX | I, U | Port 4 Full-Duplex Select (half-duplex = 0) |

| Pin No(s). | Symbol | Type | Name & Functions |
|---|---|---|---|
| **Miscellaneous Control Pins** | | | |
| 95 | M_CLK | I | Reference RMII Clock |
| 118 | M4_REFCLK | I, U | Port 4 Reference Clock |
| 148 | SCLK | I | System Clock (25 – 50 Mhz) |
| 125 | TEST# | I, U | NO Connect |
| 126 | TRUNK_EN | I, D | Port Trunking Enable |
| 146,145,144,143 | MIR_CTL[3:0] | I/O, U | Port Mirroring Control |
| 142 | RESIN_ | I, S | |
| 141 | RESETOUT_ | O | |
| **Test Pins** | | | |
| 139 | TMODE | I/O, U | Puts DS105A into test mode for ATE test |
| 138,137,136,135 | TSTOUT[7:4] | O | Test Outputs |
| 134,13,132,131 | TSTOUT[3:0] | I/O, U | Test Outputs |
| **NC Pins** | | | |
| 12,13,14,15,16,17,33,34, 35,36,37,38,40,41,42,43, 44,45,47,48,49,50,51,52, 53,54,55,56,57,58,60,61, 62,63,64,65,67,68,69,70, 71,72,88,89,90,91,92,93 | NC/Reserved | | NO Connect |
| **Power Pins** | | | |
| 3,39,73,96,130,159,184 | VDD (Core) | Input | +3.3 Volt DC Supply for Core Logic (7 pins) |
| 11,25,59,87,101,108, 119,147,152,166,175, 194,202 | VDD | Input | +3.3 Volt DC Supply for I/O Pads (13 pins) |
| 18,46,80,106,140,171, 198 | VSS (Core) | Input | Ground for Core Logic (7 pins) |
| 7,32,66,94,99,117,121, 149,154,162,180,189, 207 | VSS | Input | Ground for I/O Pads (13 pins) |

## S_CLK Speed Requirement

The S_CLK frequency requirement is highly depends on the system configuration and its maximum aggregated switching bandwidth.

The following table provides a general guideline for determining the S_CLK frequency. Any frequency higher than the value specified below up to 80MHz is acceptable.

| Port Configuration | | | 16 System Configuration | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Port 1-7** | **Port 8** | | **8+1/ 8+0** | **7+1/ 7+0** | **6+1/ 6+0** | **5+1/ 5+0** | **4+1/ 4+0** | **3+1/ 3+0** | **2+1/ 2+0** | **1+1** |
| Speed | Mode | Speed | S_CLK Frequency (Hz) | | | | | | | |
| 1M | Not Used | | 6M | 6M | 6M | 6M | 6M | 6M | 6M | |
| 1/10M | Not Used | | 6M | 6M | 6M | 6M | 6M | 6M | 6M | |
| 1/10M | Reg. | 10M | 6M | 6M | 6M | 6M | 6M | 6M | 6M | 6M |
| 1/10/25M | 4x | 100M | 20M | 18M | 17M | 16M | 15M | 13.3M | 12.5M | 11M |
| 1/10/33M | 3x | 100M | 26M | 24M | 23M | 21M | 20M | 18M | 16.6M | 15M |
| 1/10/50M | 2x | 100M | 39M | 36M | 34M | 32M | 29M | 27M | 25M | 22M |
| 10/100M | Not Used | | 54M | 49M | 44M | 40M | 35M | 30M | 26M | |
| 10/100M | Reg. | 100M | 58M | 54M | 49M | 44M | 40M | 35M | 30M | 26M |
| 10/100M | 2x | 200M | 65M | 60M | 55M | 51M | 46M | 41M | 36M | |
| 10/100M | 3x | 300M | 71M | 66M | 61M | 57M | 52M | 47M | | |
| 10/100M | 4x | 400M | 77M | 72M | 68M | 63M | 58M | | | |

## M8_REFCLK Speed Requirement

The M8_REFCLK pin can be either input or output pin depends on the Port 8 configuration.

- As an output pin, its output frequency is always equal to half of the M_CLK.
- As an input, it provides a reference clock source to the Port 8 MAC when it is configured in speed-up mode.
- M8_REFCLK input frequency is equal to 25% of the Port 8 speed (data rate).

| Port 8 Configuration | | M8_REFCLK | |
|---|---|---|---|
| **Mode** | **Speed** | **Input/Output** | **Freq.** |
| Reg. | 10/100M | Output | M_CLK/2 |
| 2x | 100M | Input | 25MHz |
| 3x | 100M | Input | 25MHz |
| 4x | 100M | Input | 25MHz |
| 2x | 200M | Input | 50MHz |
| 3x | 300M | Input | 75MHz |
| 4x | 400M | Input | 100MHz |

## 16.1 STRAP OPTIONS

The Strap options are relevant during the initial power-on period, when reset is asserted. During reset, CoSMOS will examine the boot strap address pin to determine its value and modify the internal configuration of the chip accordingly.

"1" means Pull UP

"0" means Pull Down with an external 1K Ohm

**Default value is 1,** (all boot strap pins have internal pull up resistor).

| Pin No(s) | Symbol | Name & Functions |
|---|---|---|
| **Boot Strap Pins** | | |
| 206 (L_A[5]) | Memory Size | 1 - Memory size = 256KB,<br>0 - Memory size = 512KB |
| 208 (L_A[6]) | EEPROM | 1 - NO EEPROM Installed<br>0 - EEPROM installed[1] |
| 151 (L_A[17]) | Port 8 MII/ Serial | 1 - MII Mode for port 8<br>0 - Serial mode for port 8 |
| 150 (L_A[2]) | Link Polarity | Link Polarity for serial interface<br>1 - Active Low<br>0 - Active High |
| 204 (L_A[3]) | FDX Polarity | Full/Half Duplex Polarity for serial interface<br>1 - Active Low<br>0 - Active High |
| 133 (TST[2]) | SRAM Self Test | For Board/System Manufacturing Test[2]<br>1 - Disable<br>0 - Enable |

1. If the MDS108AL is configured from EEPROM preset (L_A[6] pulled down at reset), it will try to load its configuration from the EEPROM. If the EEPROM is blank or not preset, it will not boot up. The parallel port can be used to program the EEPROM at any time.

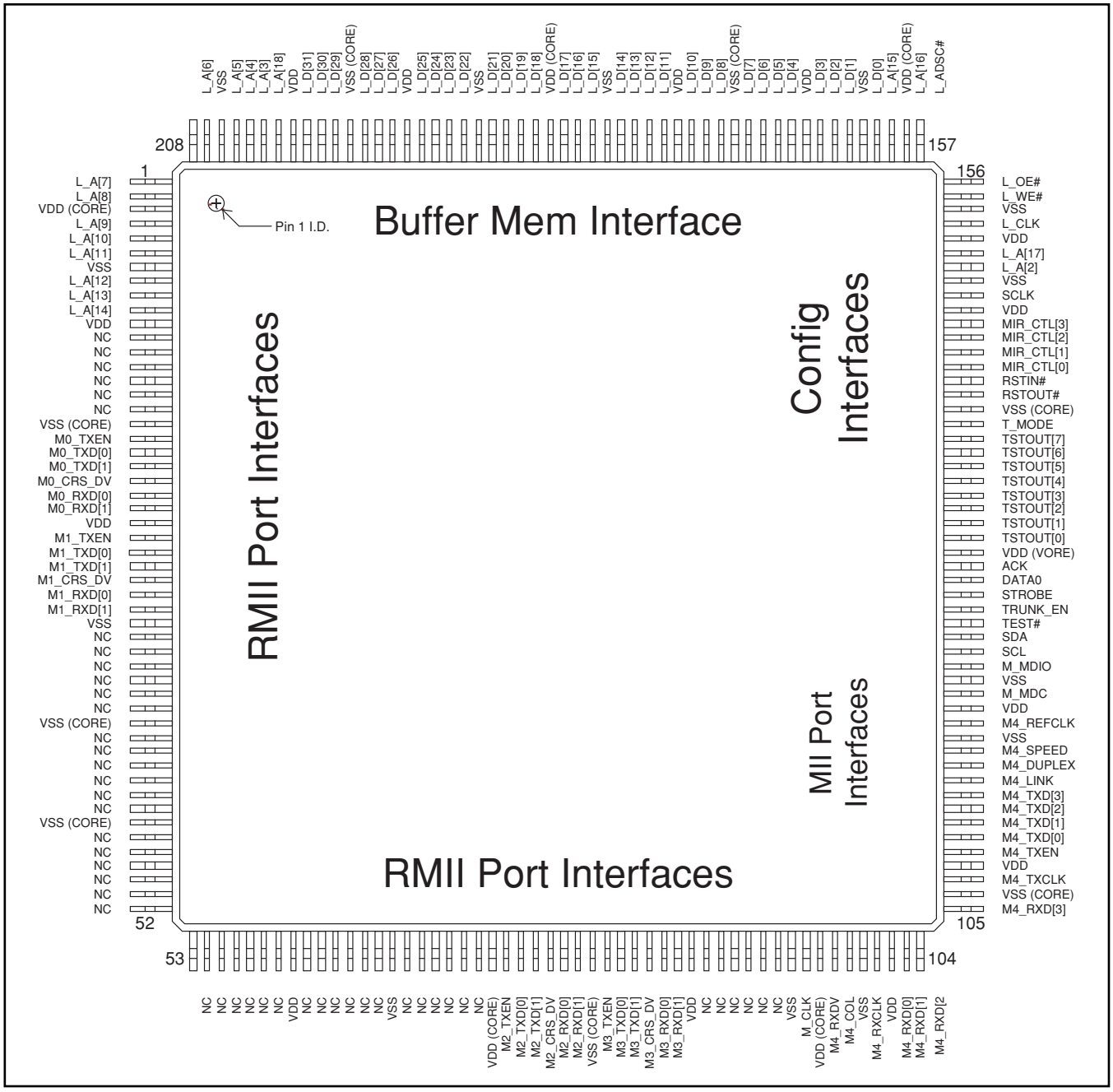
2. During normal power-up CoSMOS 2 will run through an external SSRAM memory test to ensure that there are no memory interface problems. If a problem is detected, the chip will stop functioning. To facilitate board debug in the event that a system stops functioning, the MDS108AL can be put into a continuous SS-RAM slef test mode to allow an operator to determione if there are stuck pins in the memory interface (using network analyzer).

## 16.2 PIN Reference Table

| Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # |
|---|---|---|---|---|---|---|---|
| L_A[7] | 1 | NC | 53 | M4_RXD[3] | 105 | L_ADSC# | 157 |
| L_A[8] | 2 | NC | 54 | VSS (CORE) | 106 | L_A[16] | 158 |
| VDD (CORE) | 3 | NC | 55 | M4_TXCLK/S4_TXCLK | 107 | VDD (CORE) | 159 |
| L_A[9] | 4 | NC | 56 | VDD | 108 | L_A[15] | 160 |
| L_A[10] | 5 | NC | 57 | M4_TXEN/S4_TXEN | 109 | L_D[0] | 161 |
| L_A[11] | 6 | NC | 58 | M4_TXD[0]/S4_TXD | 110 | VSS | 162 |
| VSS | 7 | VDD | 59 | M4_TXD[1] | 111 | L_D[1] | 163 |
| L_A[12] | 8 | NC | 60 | M4_TXD[2] | 112 | L_D[2] | 164 |
| L_A[13] | 9 | NC | 61 | M4_TXD[3] | 113 | L_D[3] | 165 |
| L_A[14] | 10 | NC | 62 | M4_LINK/S4_LINK | 114 | VDD | 166 |
| VDD | 11 | NC | 63 | M4_DUPLEX/ S4_DUPLEX | 115 | L_D[4] | 167 |
| NC | 12 | NC | 64 | M4_SPEED | 116 | L_D[5] | 168 |
| NC | 13 | NC | 65 | VSS | 117 | L_D[6] | 169 |
| NC | 14 | VSS | 66 | M8_REFCLK | 118 | L_D[7] | 170 |
| NC | 15 | NC | 67 | VDD | 119 | VSS (CORE) | 171 |
| NC | 16 | NC | 68 | M_MDC | 120 | L_D[8] | 172 |
| NC | 17 | NC | 69 | VSS | 121 | L_D[9] | 173 |
| VSS (CORE) | 18 | NC | 70 | M_MDIO | 122 | L_D[10] | 174 |
| M0_TXEN | 19 | NC | 71 | SCL | 123 | VDD | 175 |
| M0_TXD[0] | 20 | NC | 72 | SDA | 124 | L_D[11] | 176 |
| M0_TXD[1] | 21 | VDD (CORE) | 73 | TEST# | 125 | L_D[12] | 177 |
| M0_CRS_DV | 22 | M2_TXEN | 74 | TRUNK_ENABLE | 126 | L_D[13] | 178 |
| M0_RXD[0] | 23 | M2_TXD[0] | 75 | STROBE | 127 | L_D[14] | 179 |
| M0_RXD[1] | 24 | M2_TXD[1] | 76 | DATA0 | 128 | VSS | 180 |
| VDD | 25 | M2_CRS_DV | 77 | ACK | 129 | L_D[15] | 181 |
| M1_TXEN | 26 | M2_RXD[0] | 78 | VDD (CORE) | 130 | L_D[16] | 182 |
| M1_TXD[0] | 27 | M2_RXD[1] | 79 | TSTOUT[0] | 131 | L_D[17] | 183 |
| M1_TXD[1] | 28 | VSS (CORE) | 80 | TSTOUT[1] | 132 | VDD (CORE) | 184 |
| M1_CRS_DV | 29 | M3_TXEN | 81 | TSTOUT[2] | 133 | L_D[18] | 185 |
| M1_RXD[0] | 30 | M3_TXD[0] | 82 | TSTOUT[3] | 134 | L_D[19] | 186 |
| M1_RXD[1] | 31 | M3_TXD[1] | 83 | TSTOUT[4] | 135 | L_D[20] | 187 |
| VSS | 32 | M3_CRS_DV | 84 | TSTOUT[5] | 136 | L_D[21] | 188 |
| NC | 33 | M3_RXD[0] | 85 | TSTOUT[6] | 137 | VSS | 189 |
| NC | 34 | M3_RXD[1] | 86 | TSTOUT[7] | 138 | L_D[22] | 190 |
| NC | 35 | VDD | 87 | T_MODE | 139 | L_D[23] | 191 |
| NC | 36 | NC | 88 | VSS (CORE) | 140 | L_D[24] | 192 |
| NC | 37 | NC | 89 | RSTOUT# | 141 | L_D[25] | 193 |
| NC | 38 | NC | 90 | RSTIN# | 142 | VDD | 194 |
| VDD (CORE) | 39 | NC | 91 | MIRROR_CONTROL[0] | 143 | L_D[26] | 195 |

| Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # | Pin Name | Pin # |
|---|---|---|---|---|---|---|---|
| NC | 40 | NC | 92 | MIRROR_CONTROL[1] | 144 | L_D[27] | 196 |
| NC | 41 | NC | 93 | MIRROR_CONTROL[2] | 145 | L_D[28] | 197 |
| NC | 42 | VSS | 94 | MIRROR_CONTROL[3] | 146 | VSS (CORE) | 198 |
| NC | 43 | M_CLK | 95 | VDD | 147 | L_D[29] | 199 |
| NC | 44 | VDD (CORE) | 96 | SCLK | 148 | L_D[30] | 200 |
| NC | 45 | M4_RXDV/S4_CRS_DV | 97 | VSS | 149 | L_D[31] | 201 |
| VSS (CORE) | 46 | M4_COL/S4_COL | 98 | L_A[2] | 150 | VDD | 202 |
| NC | 47 | VSS | 99 | L_A[17] | 151 | L_A[18] | 203 |
| NC | 48 | M4_RXCLK/S4_RXCLK | 100 | VDD | 152 | L_A[3] | 204 |
| NC | 49 | VDD | 101 | L_CLK | 153 | L_A[4] | 205 |
| NC | 50 | M4_RXD[0]/S4_RXD | 102 | VSS | 154 | L_A[5] | 206 |
| NC | 51 | M4_RXD[1] | 103 | L_WE# | 155 | VSS | 207 |
| NC | 52 | M4_RXD[2] | 104 | L_OE# | 156 | L_A[6] | 208 |

## 16.3 MDS105AL Physical Pinout



## 17 DC Electrical Characteristics

### 17.1 Absolute Maximum Rating

| | |
|---|---|
| Storage Temperature | -65C to +150C |
| Operating Temperature | 0C to +70C |
| Supply Voltage VDD with Respect to $V_{SS}$ | +3.0 V to +3.6 V |
| Voltage on 5V Tolerant Input Pins | -0.5 V to (VDD +3.3V) |
| Voltage on Other Pins | -0.5V to (VDD +0.3V) |

**Caution:** Stresses above those listed may cause permanent deivce failure. Functionality at or above these limits is not implied. Exposure to the absolute Maximum Ratings for extended Ratings for extended periods may affect device reliability.

### 17.2 DC Electrical Characteristics

VDD = 3.0V to 3.6V (3.3v +/- 10%) $T_{AMBIENT}$ = 0 C to +70 C

| Symbol | Parameter Description | Preliminary | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ. | Max | |
| $f_{osc}$ | Frequency of Operation | 50 | 66 | 80 | MHz |
| $I_{DD}$ | Supply Current – @ 80 MHz (VDD =3.3 V) | | | TBD | mA |
| $V_{OH}$ | Output High Voltage (CMOS) | VDD - 0.5 | | | V |
| $V_{OL}$ | Output Low Voltage (CMOS) | | | 0.5 | V |
| $V_{IH-TTL}$ | Input High Voltage (TTL 5V tolerant) | VDD x70% | | VDD + 2.0 | V |
| $V_{IL-TTL}$ | Input Low Voltage (TTL 5V tolerant) | | | VDD x 30% | V |
| $I_{IH-5VT}$ | Input Leakage Current (0.1 V < $V_{IN}$ < VDD) (all pins except those with internal pull-up/ pull-down resistors) | | | TBD | µA |
| $I_{IL-5VT}$ | Output Leakage Current (0.1 V < $V_{OUT}$ < VDD) | | | TBD | µA |
| $I_{LI}$ | Input Leakage Current $V_{IH}$ = VDD - 0.1 V (pins with internal pull-down resistors) | | | TBD | µA |
| $I_{LO}$ | Input Leakage Current $V_{IL}$ = 0.1 V (pins with internal pull-up resistors) | | | TBD | µA |
| $C_{IN}$ | Input Capacitance | | | 5 | pF |
| $C_{OUT}$ | Output Capacitance | | | 5 | pF |
| $C_{I/O}$ | I/O Capacitance | | | 7 | pF |

## 17.3 Clock Frequency Specifications

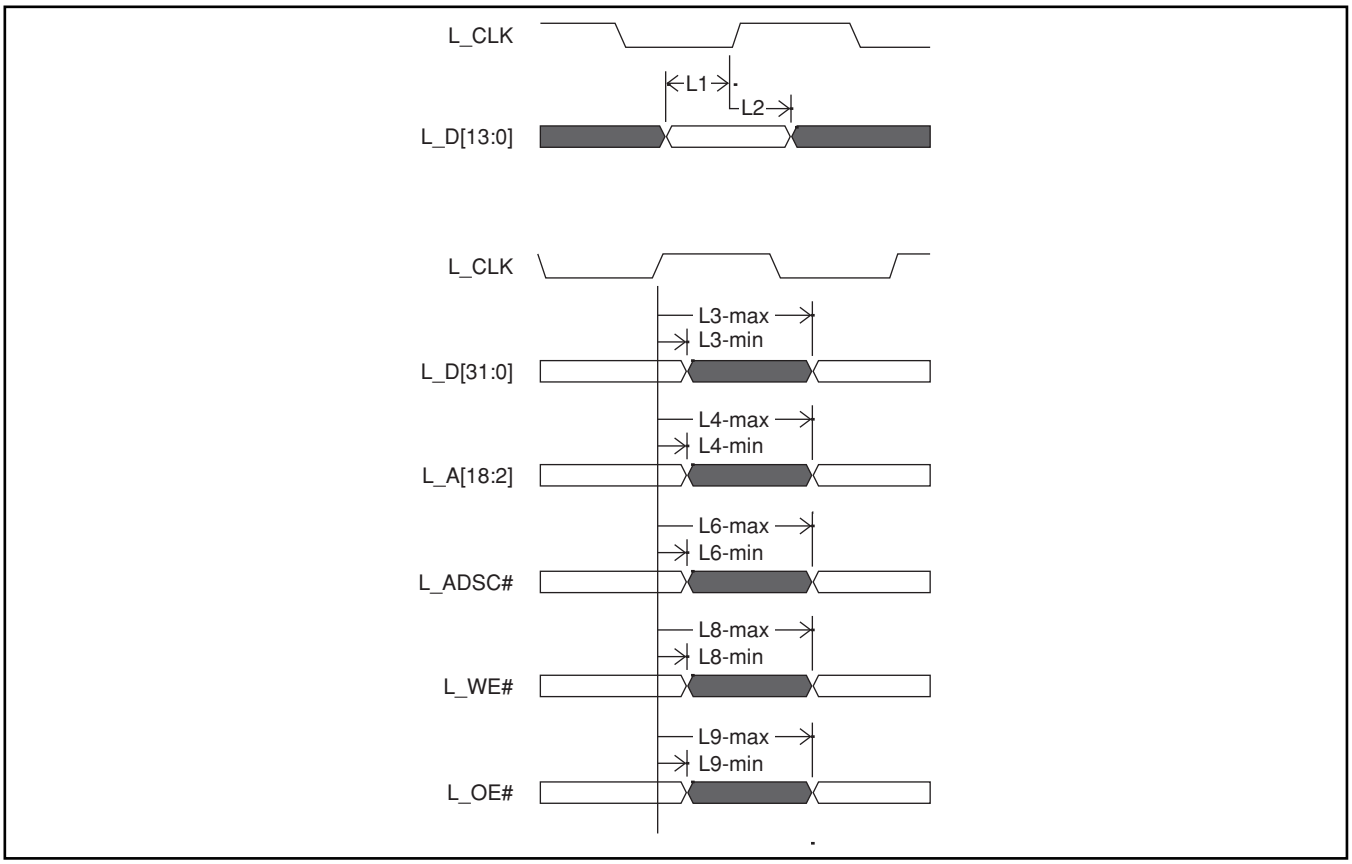
| Symbol | Parameter | (Hz) | Note: |
|---|---|---|---|
| C1 | SCLK – Core System Clock Input | 50M | |
| C2 | M_CLK – RMII Port Clock | 50M | |
| C3 | M8_REFCLK – MII Reference Clock | 25M | |
| C4 | L_CLK – Frame Buffer Memory Clock | 55M | L_CLK = SCLK |
| C5 | M_MDC – MII Management Data Clock | 1.56M | M_MDC=SCLK/32 |
| C6 | SCL – $I^2C$ Data Clock | 50K | SCL=M_CLK/1000 |

Suggestion Clock rate for various configurations:

| Configuration | | Input | | | Output | | |
|---|---|---|---|---|---|---|---|
| Port 0-7 | Port 8 | SCLK | M_CLK (RMII) | M8_REF | L_CLK | M_MDC | SCL |
| 10M RMII | 10/100M MII | 50M | 50M | -- | =SCLK | =SCLK/32 | 50K |
| 100M RMII | Not Used | 55M | 50M | -- | =SCLK | =SCLK/32 | 50K |
| 100M RMII | 10/100M MII | 60M | 50M | 25M | =SCLK | =SCLK/32 | 50K |
| 100M RMII | 200M MII | 66.66M | 50M | 50M | =SCLK | =SCLK/32 | 50K |
| 100M RMII | 300M MII | 75M | 50M | 75M | =SCLK | =SCLK/32 | 50K |
| 100M RMII | 400M MII | 80M | 50M | 100M | =SCLK | =SCLK/32 | 50K |

## 17.4 AC Timing Characteristics

### 17.4.1 Frame Buffer Memory Interface:



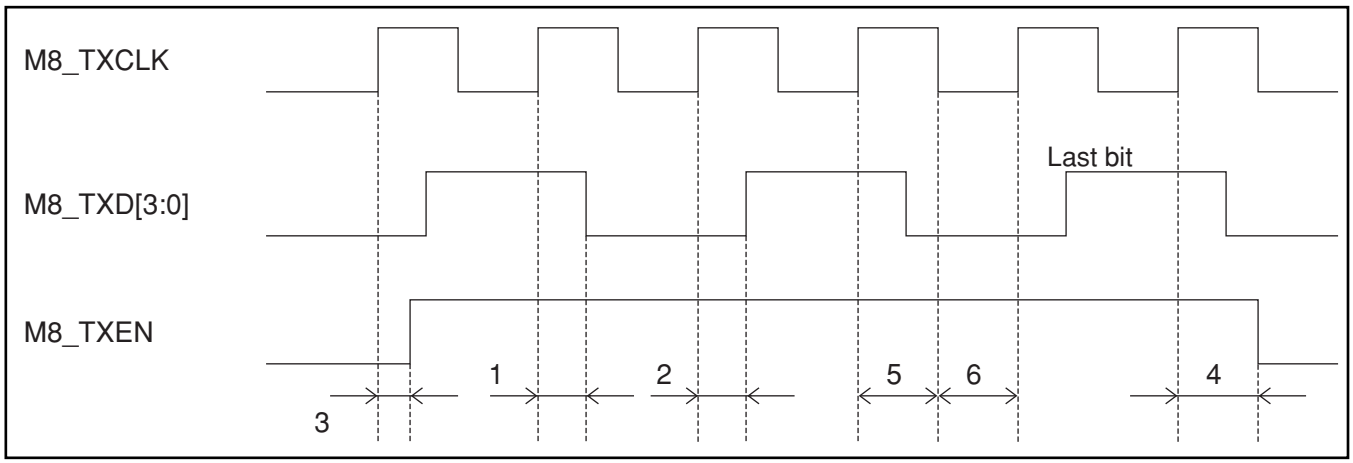

## 17.5 Frame Buffer Memory Interface Timing

| Symbol | Parameter | 50 MHz | | Note: |
|---|---|---|---|---|
| | | Min (ns) | Max (ns) | |
| L1 | L_D[31:0] input set-up time | 5 | | |
| L2 | L_D[31:0] input hold time | 0 | | |
| L3 | L_D[31:0] output valid delay | 1 | 8 | $C_L$ = 30pf |
| L4 | L_A[18:2] output valid delay | 1 | 8 | $C_L$ = 50pf |
| L6 | L_ADSC# output valid delay | 1 | 8 | $C_L$ = 50pf |
| L8 | L_WE# output valid delay | 1 | 8 | $C_L$ = 30pf |
| L9 | L_OE# output valid delay | 1 | 8 | $C_L$ = 30pf |

## 17.6 RMII Timing Requirements

| Symbol | Parameter | 50 MHz | | Note: |
|---|---|---|---|---|
| | | Min (ns) | Max (ns) | |
| M1 | M_CLK | 5 | | Reference Input Clock |
| M2 | M[7:0]_RXD[1:0] Input Setup Time | 4 | | |
| M3 | M[7:0]_RXD[1:0] Input Hold Time | 1 | | |
| M4 | M[7:0]_CRS_DV Input Setup Time | 4 | | |
| M5 | M[7:0]_TXEN Output Delay Time | 1 | 11 | $C_L$ = 30pf |
| M6 | M[7:0]_TXD[1:0] Output Delay Time | 1 | 11 | $C_L$ = 30pf |
| M7 | M[7:0]_LINK Input Setup Time | | | |

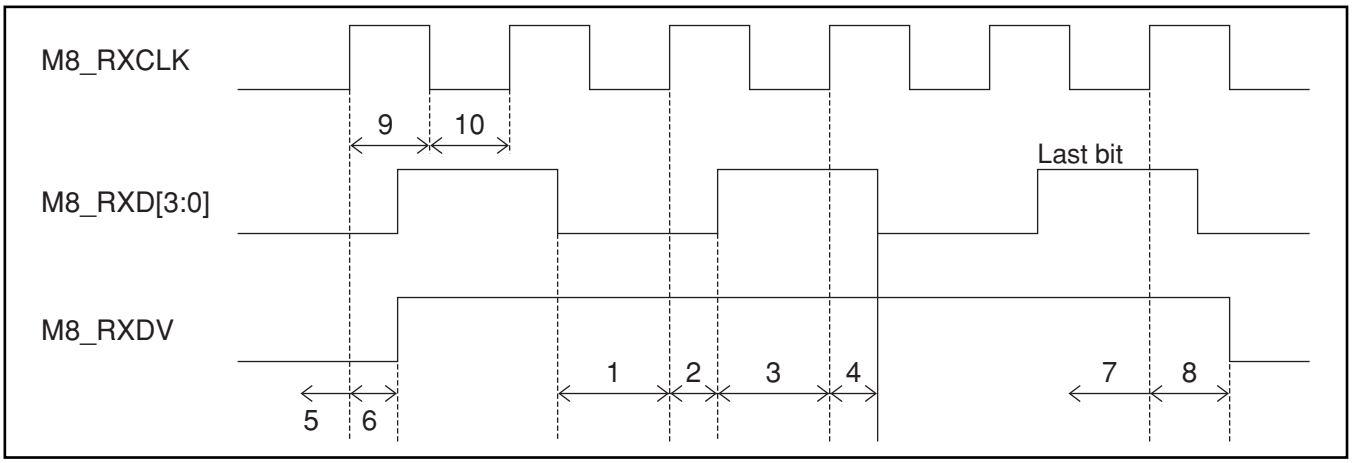
## 17.7 MII Timing Requirements




**Transmit timing**

| Symbol | Parameter | Time | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 1 | M8_TXCLK rise to M8_TXD[3:0] inactive delay | 5 | 20 | nS |
| 2 | M8_TXCLK rise to M8_TXD[3:0] active delay | 5 | 20 | nS |
| 3 | M8_TXCLK rise to M8_TXEN active delay | 5 | 20 | nS |
| 4 | M8_TXCLK rise of Last M8_TXD bit to M8_TXEN inactive delay | 5 | 20 | nS |
| 5 | M8_TXCLK Hi wide | 25 | Inf. | nS |
| 6 | M8_TXCLK Low wide | 25 | Inf. | nS |
| | M8_TXCLK input rise time require | | 5 | nS |
| | M8_TXCLK input fall time require | | 5 | nS |

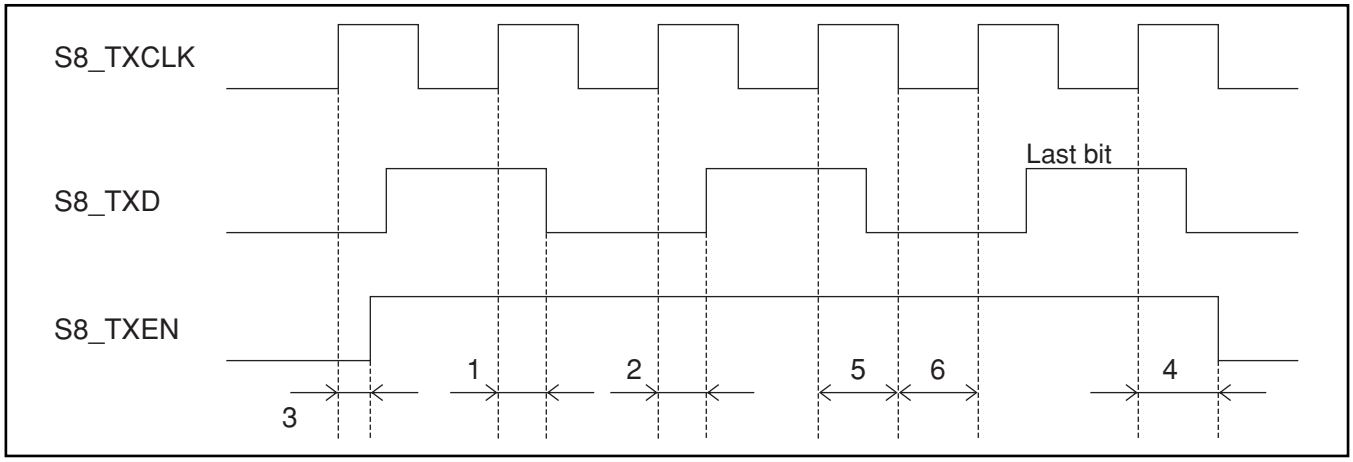
*Inf. = infinite




**Receive timing**

| Symbol | Parameter | Time | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 1 | M8_RXD[3:0] Low input set-up time | 10 | | nS |
| 2 | M8_RXD[3:0] Low input hold time | | 5 | nS |
| 3 | M8_RXD[3:0] Hi input set-up time | 10 | | nS |
| 4 | M8_RXD[3:0] Hi input hold time | | 5 | nS |
| 5 | M8_RXDV Low input set-up time | 10 | | nS |
| 6 | M8_RXDV Low input hold time | | 5 | nS |
| 7 | M8_RXDV Hi input set-up time | 10 | | nS |
| 8 | M8_RXDV Hi input hold time | | 5 | nS |
| 9 | M8_RXCLK Hi wide | 25 | Inf. | nS |
| 10 | M8_RXCLK Low wide | 25 | Inf. | nS |
| | M8_RXCLK input rise time require | | 5 | nS |
| | M8_RXCLK input fall time require | | 5 | nS |

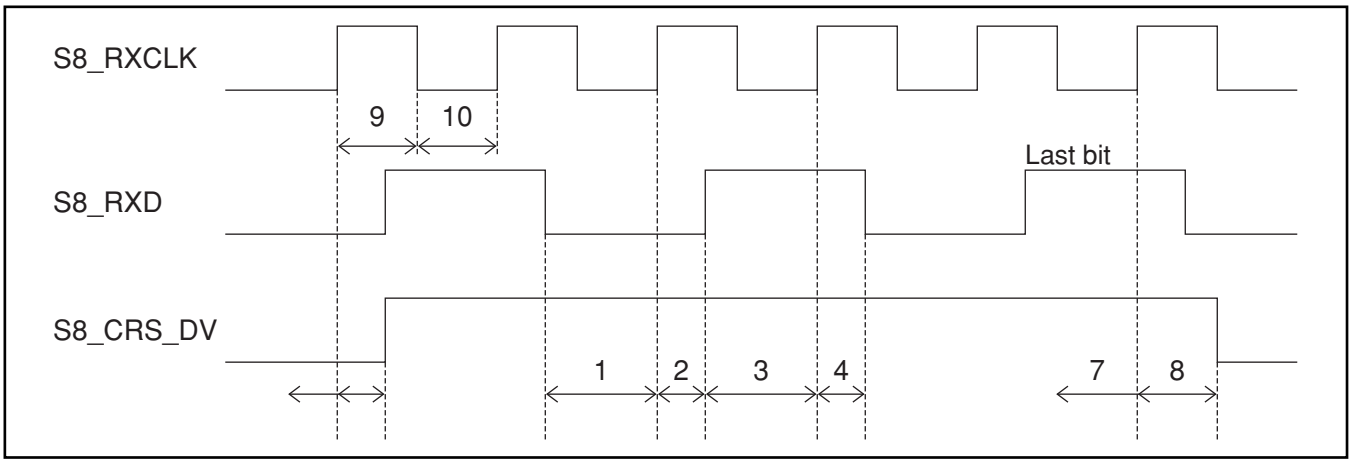
## 17.8 Port 8 Serial Mode AC Timing




**Transmit timing**

| Symbol | Parameter | Time | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 1 | S8_TXCLK rise to S8_TXD inactive delay | 5 | 20 | nS |
| 2 | S8_TXCLK rise to S8_TXD active delay | 5 | 20 | nS |
| 3 | S8_TXCLK rise to S8_TXEN active delay | 5 | 20 | nS |
| 4 | S8_TXCLK rise of Last S8_TXD bit to S8_TXEN inactive delay | 5 | 20 | nS |
| 5 | S8_TXCLK Hi wide | 25 | Inf. | nS |
| 6 | S8_TXCLK Low wide | 25 | Inf. | nS |
| | S8_TXCLK input rise time require | | 5 | nS |
| | S8_TXCLK input fall time require | | 5 | nS |

*Inf. = infinite

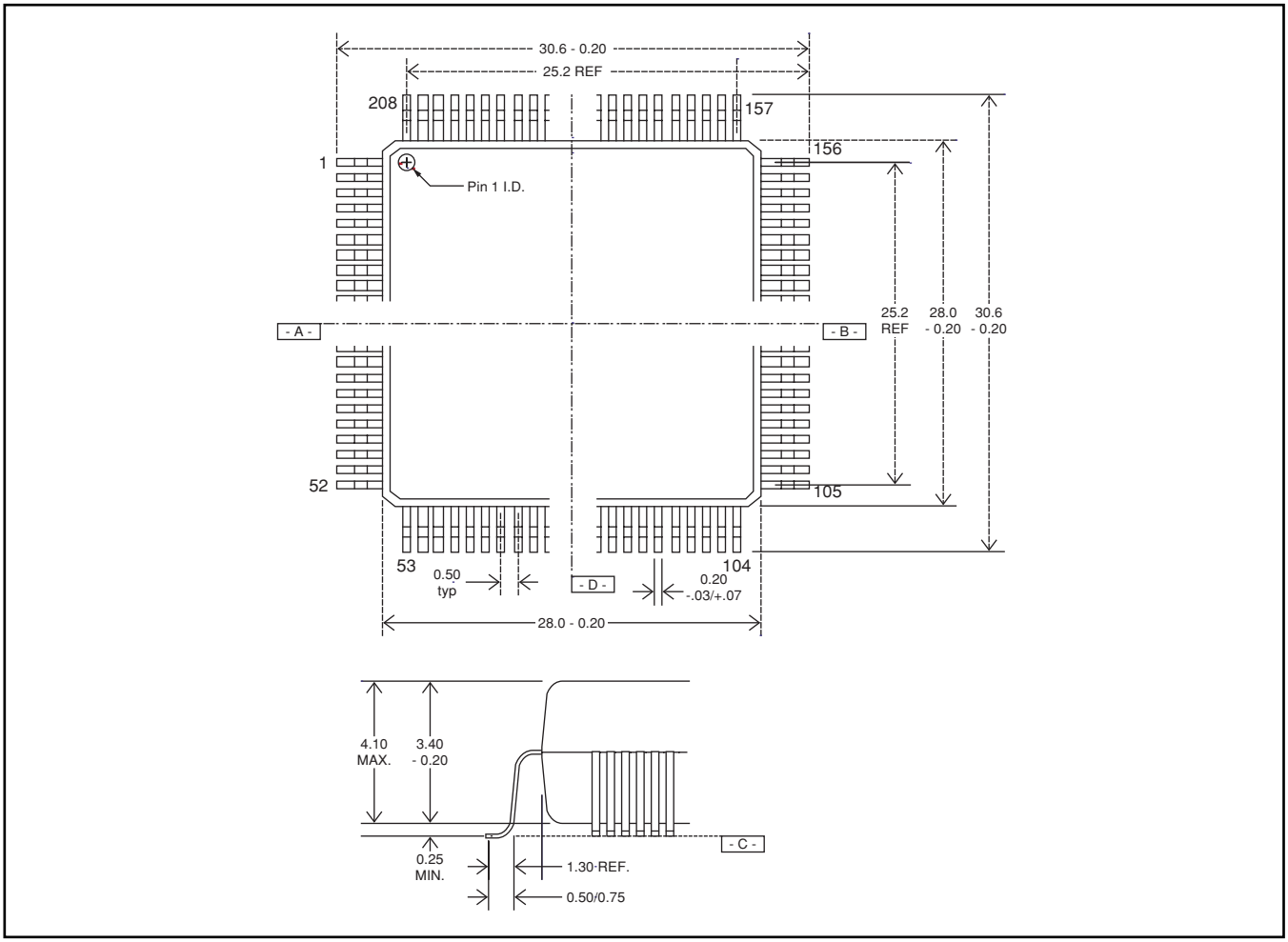



**Receive timing**

| Symbol | Parameter | Time | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 1 | S8_RXD Low input set-up time | 10 | | nS |
| 2 | S8_RXD Low input hold time | | 5 | nS |
| 3 | S8_RXD Hi input set-up time | 10 | | nS |
| 4 | S8_RXD Hi input hold time | | 5 | nS |
| 5 | S8_CRS_DV Low input set-up time | 10 | | nS |
| 6 | S8_CRS_DV Low input hold time | | 5 | nS |
| 7 | S8_CRS_DV Hi input set-up time | 10 | | nS |
| 8 | S8_CRS_DV Hi input hold time | | 5 | nS |
| 9 | S8_RXCLK Hi wide | 25 | Inf. | nS |
| 10 | S8_RXCLK Low wide | 25 | Inf. | nS |
| | S8_RXCLK input rise time require | | 5 | nS |
| | S8_RXCLK input fall time require | | 5 | nS |

## 18 Packaging

CoSMOS MDS105AL is packaged in a 208 pin PQFP (dimensions in mm)



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