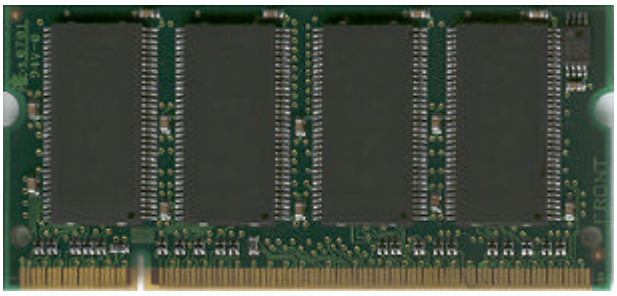
DTM67600

256MB - 32M x 64, 200-Pin Unbuffered DDR SODIMM



Identification

Part Number: DTM67600

Performance Range

266MHz/CL=2.5
200MHz/CL=2

Features

- Utilizes 133MHz DDR SDRAM
- Auto and self refresh capability
- SSTL_2 compatible inputs and outputs
- VDD/VDDQ= 2.5V ? 0.2V
- MRS cycle with address key programs Latency (Access from column address) Burst length (2,4, and 8 page) Data scramble (Sequential and Interleave)
- Serial presence detect with EPPROM
- 200-pin, JEDEC, double-sided SODIMM assembly, 2.66" wide by 1.25" high
- One Physical Bank (Rows)
- SDRAM Addressing (13/10/2) (Row/Col/Bank)

Description

The Dataram DTM67600 is a high-speed, random access, 256MB module configured as one physical bank (row) 32M deep and 64 bits wide. The DTM67600 is an unbuffered module, comprised of eight, 32Mx8 (256Mb) DDR Synchronous DRAMs in 66 pin, TSSOP-II packages. Each byte is controlled by a separate mask line (DQMBx) to mask writes and controls the output enable during read operations.

A 256 byte EEPROM provides critical timing and configuration information used by the system to identify and configure the memory. The lower 128 bytes are programmed by Dataram and contains the timing/configuration data. The upper 128 bytes are Read/Write enabled and may be used by the customer as needed.

DDR SDRAM SO-DIMM Pinout

Front side								Back side							
1	VREF	51	VSS	101	A9	151	DQ42	2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43	4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VDD	6	DQ4	56	DQ28	106	A6	156	VDD
7	DQ1	57	VDD	107	A5	157	VDD	8	DQ5	58	VDD	108	A4	158	$\overline{CK}$1
9	VDD	59	DQ25	109	A3	159	VSS	10	VDD	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	VSS	12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48	14	DQ6	64	VSS	114	VDD	164	DQ52
15	VSS	65	DQ26	115	A10/AP	165	DQ49	16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VDD	18	DQ7	68	DQ31	118	$\overline{RAS}$	168	VDD
19	DQ8	69	VDD	119	$\overline{WE}$	169	DQS6	20	DQ12	70	VDD	120	$\overline{CAS}$	170	DM6
21	VDD	71	CB0	121	$\overline{S}$0	171	DQ50	22	VDD	72	CB4	122	$\overline{S}$1	172	DQ54
23	DQ9	73	CB1	123	DU	173	VSS	24	DQ13	74	CB5	124	DU	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51	26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	DQS8	127	DQ32	177	DQ56	28	VSS	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	VDD	30	DQ14	80	CB6	130	DQ37	180	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57	32	DQ15	82	VDD	132	VDD	182	DQ61
33	VDD	83	CB3	133	DQS4	183	DQS7	34	VDD	84	CB7	134	DM4	184	DM7
35	CK0	85	DU	135	DQ34	185	VSS	36	VDD	86	DU	136	DQ38	186	VSS
37	$\overline{CK}$0	87	VSS	137	VSS	187	DQ58	38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	CK2	139	DQ35	189	DQ59	40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	$\overline{CK}$2	141	DQ40	191	VDD	42	DQ20	92	VDD	142	DQ44	192	VDD
43	DQ17	93	VDD	143	VDD	193	SDA	44	DQ21	94	VDD	144	VDD	194	SA0
45	VDD	95	CKE1	145	DQ41	195	SCL	46	VDD	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	DU (A13)	147	DQS5	197	VDDSPD	48	DM2	98	DU (BA2)	148	DM5	198	SA2
49	DQ18	99	A12	149	VSS	199	VDDID	50	DQ22	100	A11	150	VSS	200	DU

Notes:

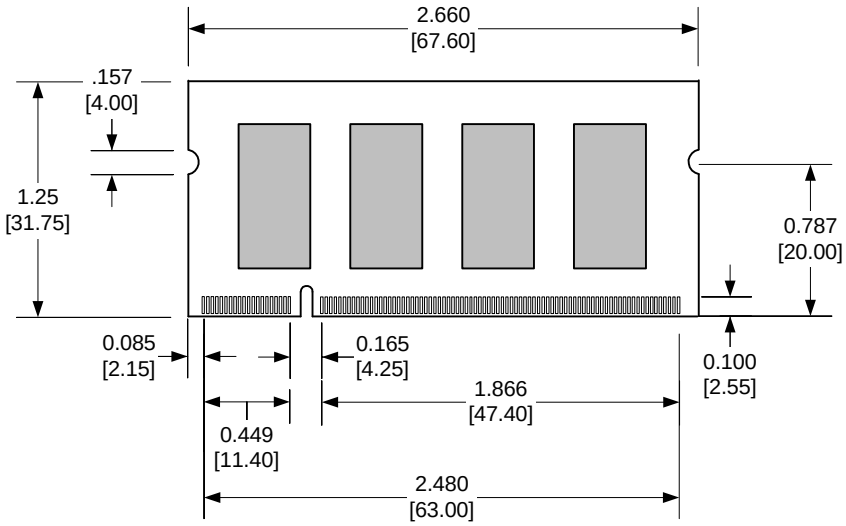
Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 variants of this module and are not used on the x64 versions.

Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version.

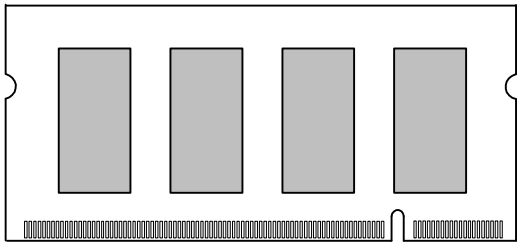
Pins 89, 91 are reserved for x72 modules or registered modules.

Pin 97 is reserved for higher density memories, requiring A13.

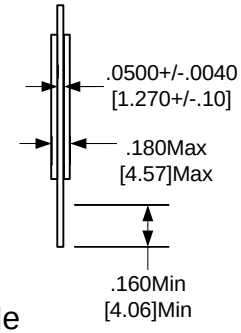
Pin 98 is reserved for devices with eight banks, requiring BA2.



Front



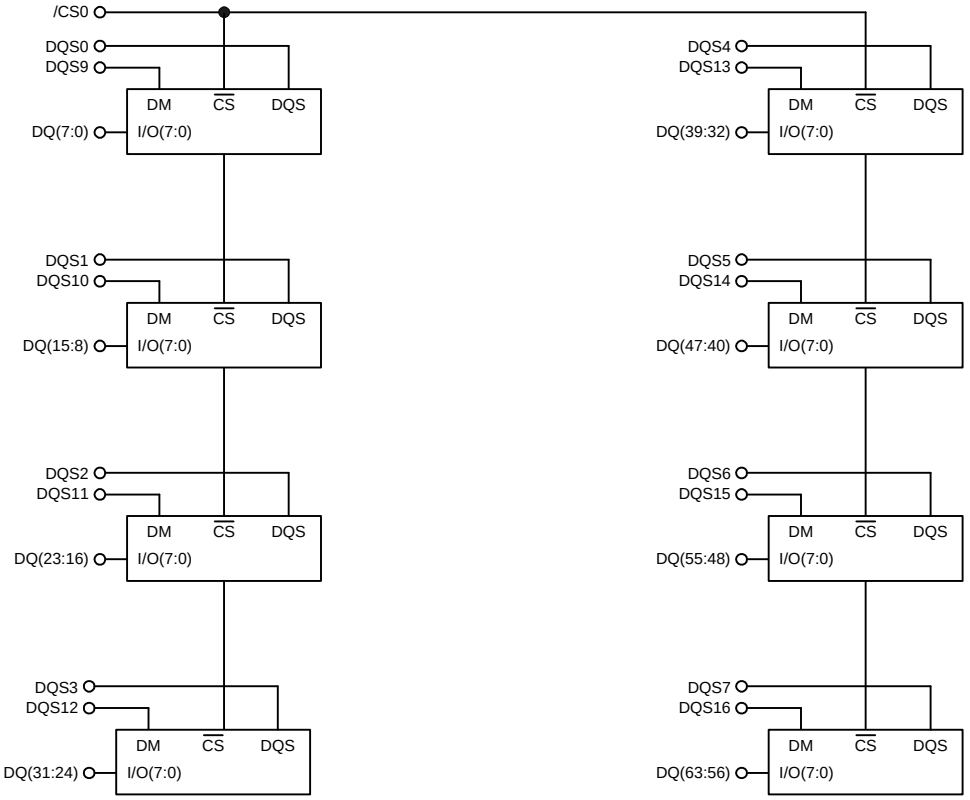
Back

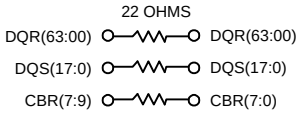


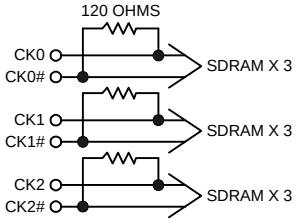
Side

Notes

All dimensions are expressed: inches [millimeters]
Tolerances on all dimensions except where otherwise indicated are ? .005 (.13)
The device used is 32Mx8 SDRAM, TSOP



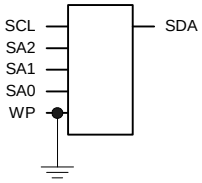




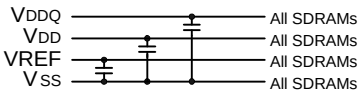
GLOBAL SDRAM CONNECTS

BA(1:0) →	BA(1:0)	(All SDRAMs)
A(12:0) →	A(12:0)	(All SDRAMs)
/RAS →	/RAS	(All SDRAMs)
/CAS →	/CAS	(All SDRAMs)
CKE0 →	CKE0	(All SDRAMs)
/WE →	/WE	(All SDRAMs)

SERIAL PD



DECOUPLING



Absolute maximum ratings

Voltage on V_{DD} Supply
Relative to V_{SS} ..... -0.3 to +3.6V
Voltage on V_{DDQ} Supply
Relative to V_{SS} ..... -0.3 to +3.6V
Voltage on V_{REF} and Inputs
Relative to V_{SS} ..... -0.3 to +3.6V
Voltage on I/O Pins
Relative to V_{SS} ..... -0.3V to V_{DDQ} +0.3V
Operating Temperature, T_A (ambient) .....0?C to +70?C
Storage Temperature (plastic) ..... -55?C to +150?C
Power Dissipation 8W
Short Circuit Output Current 50mA

***Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

DC Operating Conditions and Characteristics

(Notes: 1-6; notes appear below and on next page) (0?C ? T_A ? + 70?C; V_{DD} = +2.5V ? 0.2V, $V_{DD}Q$ = +2.5V ? 0.2V

	Symbol	Minimum	Maximum	Units	Notes
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	$V_{DD}Q$	2.3	V_{DD}	V	
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	7
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04	V_{REF} + 0.04	V	8
Input High (Logic 1) Voltage	V_{IH}	V_{REF} + 0.18	V_{DD} + 0.3	V	9
Input Low (Logic 0) Voltage	V_{IL}	-0.3	V_{REF} – 0.18	V	9
Clock Input Voltage; CK0 and CK0#	V_{IN}	-0.3	$V_{DD}Q$ + 0.3	V	
Clock Input Differential Voltage Level; CK0 and CK0#	V_{ID}	0.36	$V_{DD}Q$ + 0.6	V	10
Clock Input Crossing Point Voltage; CK0 and CK0#	V_{IX}	1.15	1.35	V	11
INPUT LEAKAGE CURRENT **Any input 0V ? V_{IN} ? V_{DD}** **(All other pins not under test=0v**	$I_{1(L)}$	-16	16	uA	
OUTPUT LEAKAGE CURRENT **(DQ_s are disabled; 0V ? V_{OUT} ? $V_{DD}Q$**	$I_{O(L)}$	-5	5	uA	
OUTPUT LEVELS **Output High Current (V_{OUT} = 1.95V, maximum V_{TT})**	I_{OH}	-15.2	-	mA	
Output Low Current (V_{OUT} = 0.35V, maximum V_{TT})	I_{OL}	15.2	-	mA	

NOTES:

1. All voltage referenced to VSS.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are quaranteed for the full voltage range specified.
3. Outputs measure with equivalent load: