DTM63621, 63622

1GB-128Mx72, 184-Pin Registered DDR SDRAM DIMM

Identification

DTM63621: PC2100 266 MHz/CL = 2.5

DTM63622: PC1600 200 MHz/CL = 2

Features

The 63621 utilizes 133MHz DDR SDRAM
The 63622 utilizes 100MHz DDR SDRAM

Auto & self refresh capability (8192 Cycles/64 MS)

SSTL_2 compatible inputs and outputs

VDD/VDDQ = 2.5V +/- 0.2V

MRS cycle, with address key, programs Latency (Access from Column address) Burst length (2,4, and 8 page)

Data scramble (Sequential & Interleave)

Serial Presence Detect

184-pin JEDEC DIMM, double-sided assembly, 5.25" wide by 1.20" high

Commands entered on each positive CK edge

DQS edge-aligned with Data for Reads; center-aligned with Data for Writes

Two Data accesses per clock cycle

DTM63621 and DTM63622 are two Physical Bank

SDRAM Addressing (13/11/2)(ROW/COL/BANK)

Description

The Dataram DTM63621 assembly is a 1.2" high PC2100 Registered 128Mx72 DDR Synchronous Dynamic RAM high-density memory module. The DTM63621 consists of eighteen externally stacked CMOS 128M x 4 bit DDR Synchronous DRAMs in a 66-pin TSOP-II 400mil package, two 13-bit to 26-bit Registered, one PLL and one 2K EEPROM used for serial presence detect (SPD).

The Dataram DTM63622 assembly is a 1.2" high PC1600 Registered 128Mx72 DDR Synchronous Dynamic RAM high-density memory module. The DTM63622 consists of eighteen externally stacked CMOS 128M x 4 bit DDR Synchronous DRAMs in a 66-pin TSOP-II 400mil package, two 13-bit to 26-bit Registers, one PLL and one 2K EEPROM used for serial presence detect (SPD).

Pin Configurations

Front side								Back side							
1	VREF	24	DQ17	47	DQS8	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ46
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DQS17	163	DQ47
3	VSS	26	VSS	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DQS11	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	VSS	97	DQS9	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	NC	98	DQ6	121	DQ22	144	CB7	167	NC
7	VDD	30	VDDQ	53	DQ32	76	NC	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DQS15
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	/RESET	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DQS13	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	VDDID	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DQS12	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DQS10	130	A3	153	DQ44	176	VSS
16	NC	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS	177	DQS16
17	NC	40	DQ27	63	WE	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS	88	DQ59	111	CKE1	134	CB4	157	S0	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5	158	S1	181	SA0
21	CKE0	44	CB0	67	DQS5	90	WP*	113	NC	136	VDDQ	159	DQS14	182	SA1
22	VDDQ	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	A12	138	/CK0	161	DQ46	184	VDDSPD

NC = No connect * = Not Used

Pin Names

Pin name	Function
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
CS[1:0]	Chip select
CK0,/CK0	Differential Clock inputs
CKE[1:0]	Clock enable input
BA[1:0]	Bank select input
A[12:0]	Address input(Multiplexed)
VREF	SSTL_2 reference input
VDDID	VDD identification flag
SCL	Serial clock
SDA	Serial Data I/O
SA[2:0]	Address EEPROM
CB[7:0]	Data I/Os: Check bits
DQS[17:0]	Data strobes
DQ[63:0]	Data I/Os: Data bus
VDDQ	DQ power supply: 2.5V +/- .2V
VDD	Power supply: 2.5V +/- .2V
VSS	Ground
VDDSPD	Serial EEPROM power supply
/RESET	Reset Enable
NC	No connects

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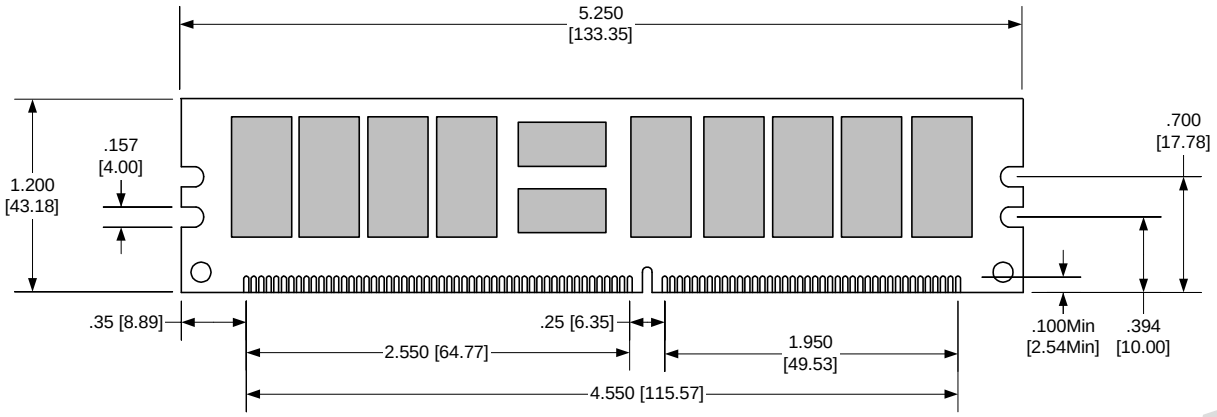
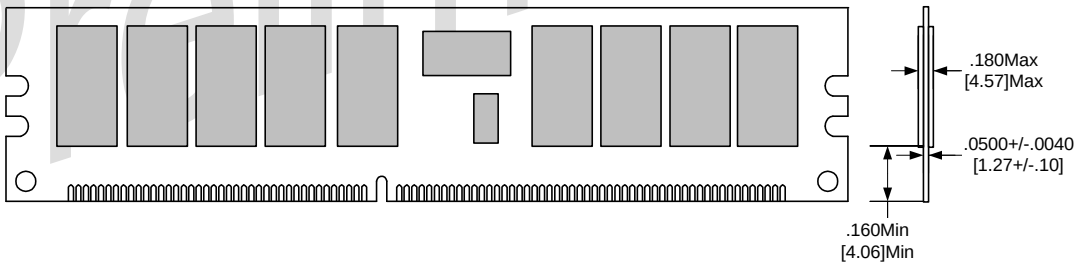


Front



Back Side

Notes

All dimensions are expressed: inches [millimeters].

Tolerances on all dimensions except where otherwise indicated are ? .005 (.13).

The device used is 128Mx4 STACKED SDRAM, TSOP.

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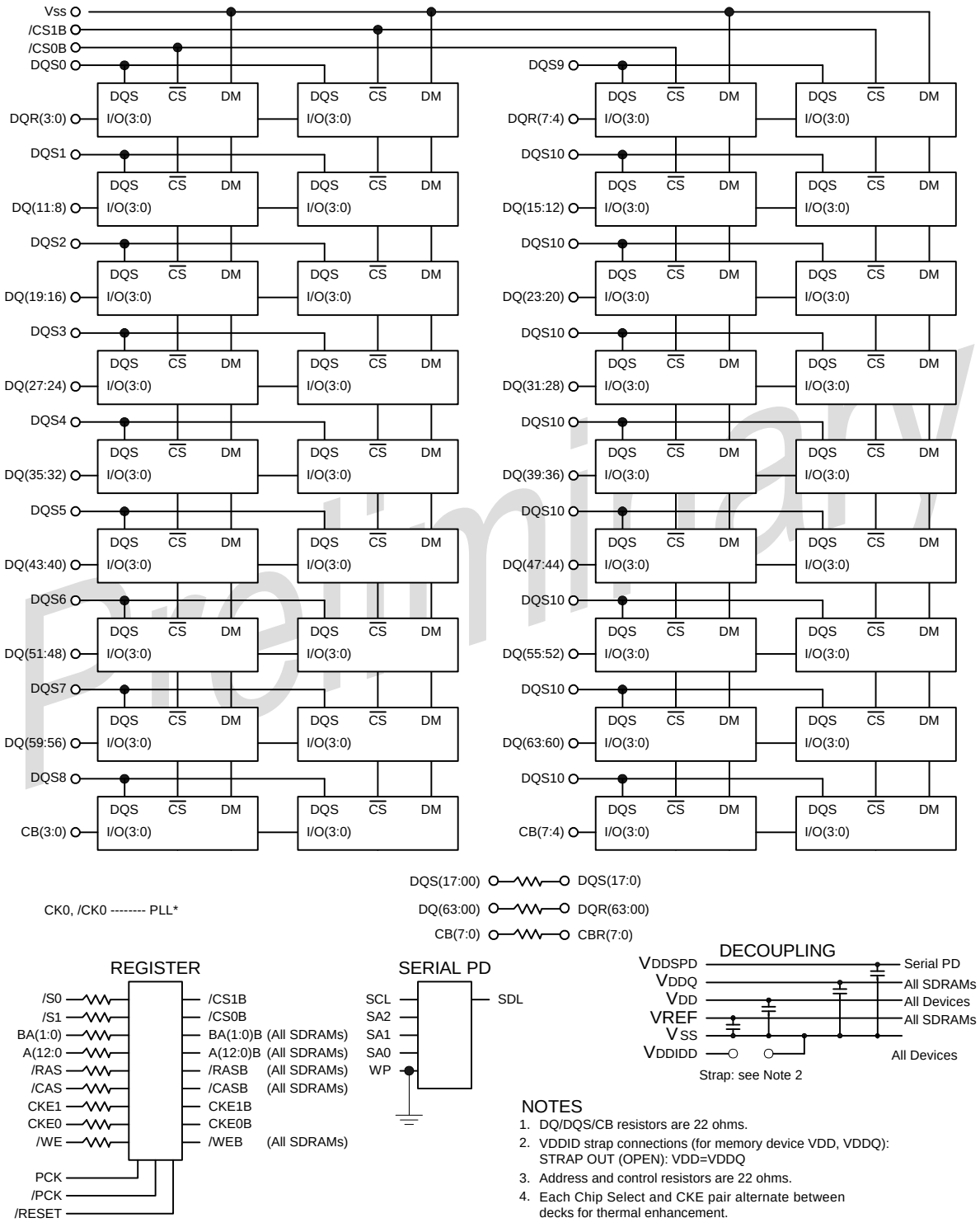

NOTES
1. DQ/DQS/CB resistors are 22 ohms.
2. VDDID strap connections (for memory device VDD, VDDQ): STRAP OUT (OPEN): VDD=VDDQ
3. Address and control resistors are 22 ohms.
4. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

Absolute Maximum Ratings (DTM63621, 63622)

PARAMETER	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN,VOUT	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDD	-0.5 ~ 0.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	18	W
Soldering Temperature Time	TSOLDER	260 10	°C

Note: Operation at above absolute maximum rating can adversely affect device reliability.

DC Operating Conditions (DTM63621, 63622) (T_A = 0 to 70ºC, Voltage referenced to V_{ss}=0V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Power Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.15	-	V_{DDQ} +0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	V_{REF} – 0.15	V	2
Termination Voltage	V_{TT}	V_{REF} + 0.04	V_{REF}	V_{REF}+0.04	V	
Reference Voltage	V_{REF}	1.15	1.25	1.35	V	3

Notes:

1. VDDG must not exceed the level of VDD
2. VIL (min) is acceptable - 1.5V AC pulse width with < 5ns of duration
3. The value of VREF is approximately equal to 0.5VDDQ.

Capacitance (DTM63621, 63622) (TA = 25°C, f=100MHz)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input capacitance	A0-A12,BA0,BA1	CIN1	5	9	pF
Input capacitance	RAS, CAS, WE	CIN2	5	9	pF
Input capacitance	CKE0, /CKE1	CIN3	5	9	pF
Input capacitance	CSO, CS1	CIN4	5	9	pF
Data input/output Capacitance	DQ0-DQ63, DQS0-DQS17	CI01	8	11	pF
Data input/output Capacitance	CB0~CB7	C102	8	11	pF

Notes:

1. VDD=min. to max., VDDQ=2.3V to 2.7V, VODC=VDDQ/2, Vopeak-to-peak=0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only