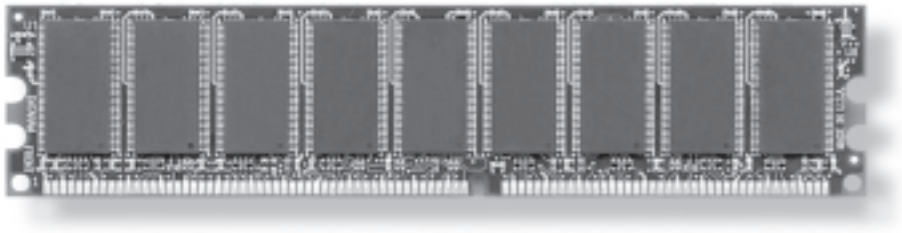
DTM63605,63607

128MB-16M x 72, 256MB-32M x 72, 184 Pin Unbuffered DDR SDRAM DIMMs



Performance range

266MHz/CL=2.5
200MHz/CL=2

Features

- Utilizes 133MHz DDR SDRAM
- Auto & self refresh capability
- SSTL_2 compatible inputs and outputs
- VDD/VDDQ=2.5V+/-0.2V
- MRS cycle, with address key, programs Latency (Access from column address) Burst length (2, 4 and 8 page) Data scramble (Sequential & Interleave)
- Serial Presence Detect
- 184-pin JEDEC DIMM double-sided assembly, 5.250" wide by 1.25" high
- Commands entered on each positive CK edge
- DQS edge-aligned with data for Reads; center-aligned with Data for Writes
- Two Data accesses per clock cycle
- DTM63605 is one physical bank
- DTM63607 is two physical banks
- SDRAM Addressing (12/10/2) (Row/Col/Bank)

Description

The Dataram DTM63605 assembly is a 16Mx72 DDR Synchronous Dynamic RAM high density memory module. The DTM63605 consists of nine CMOS monolithic 16M x 8bit DDR Sychronous DRAMs in a 66 pin TSOP-II 400mil package. The Dataram DTM63607 assembly is a 32M x 72 DDR Synchronous Dynamic RAM high density memory module. The DTM63607 consists of eighteen CMOS monolithic 16M x 8bit DDR Synchronous DRAMS in a 66pin TSOP-II 400mil package. One 2K EEPROM for serial presence detect is used on all assemblies. These DDR SDRAM modules use a double data rate architecture to achieve high speed operation. Synchronous design allows for precise cycle control with the use of a differential system clock.

Pin configurations

Front side								Back side							
1	VREF	24	DQ17	47	DQS8	70	VDD	93	Vss	116	VSS	139	VSS	162	DQ46
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DQS17	163	DQ47
3	VSS	26	VSS	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DQS11	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	VSS	97	DQS9	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	CK2#	98	DQ6	121	DQ22	144	CB7	167	NC
7	VDD	30	VDDQ	53	DQ32	76	CK2	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DQS15
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	NC	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DQS13	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	VDDID	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DQS12	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DQS10	130	A3	153	DQ44	176	VSS
16	CK1	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS#	177	DQS16
17	CK1#	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS#	88	DQ59	111	CKE1	134	CB4	157	CS0#	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5	158	CS1#	181	SA0
21	CKE0	44	CB0	67	DQS5	90	NC	113	NC	136	VDDQ	159	DQS14	182	SA1
22	VDDQ	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SDL	115	NC	138	CK0#	161	DQ46	184	VDDSPD

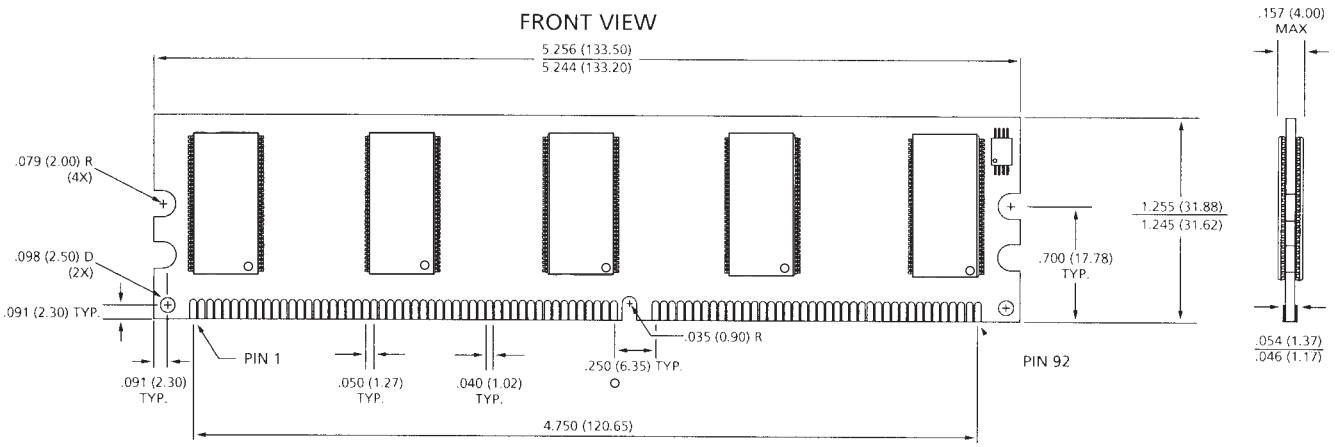
Pin names

Pin name	Function
RAS#	Row address strobe
CAS#	Column address strobe
WE#	Write enable
*CS#[1:0]	Chip select
CK[2:0],CK#[2:0]	Differential Clock Inputs
*CKE[1:0]	Clock enable input
BA[1:0]	Bank Select Input
A[11:0]	Address input (Multiplexed)
VREF	SSTL_2 reference input
VDDID	VDD identification flag
SCL	Serial clock
SDA	Serial data I/O
SA[2:0]	Address EEPROM
CB[7:0]	Data I/Os: Check bits
DQS[17:0]	Data Strobes
DQ[63:0]	Data I/Os: Data bus
VDDQ	DQ power supply: 2.5V +/-.2V
VDD	Power supply: 2.5V +/-.2V
VSS	Ground
VDDSPD	Serial EEPROM power supply
NC	No connects

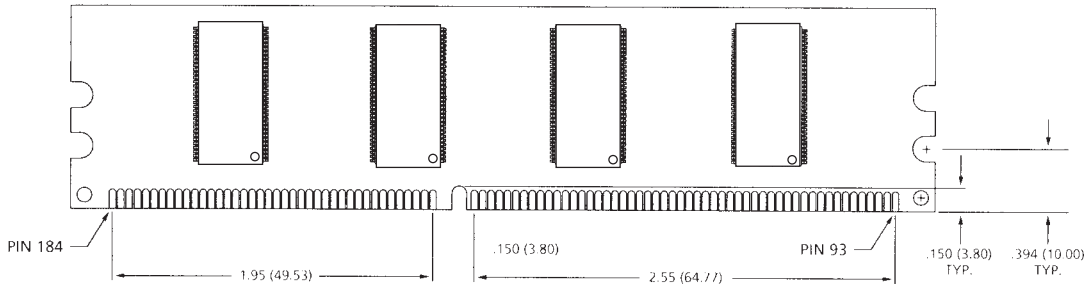
* CS1# and CKE are not used on the DTM63605.

DTM63605 184-PIN DIMM

FRONT VIEW

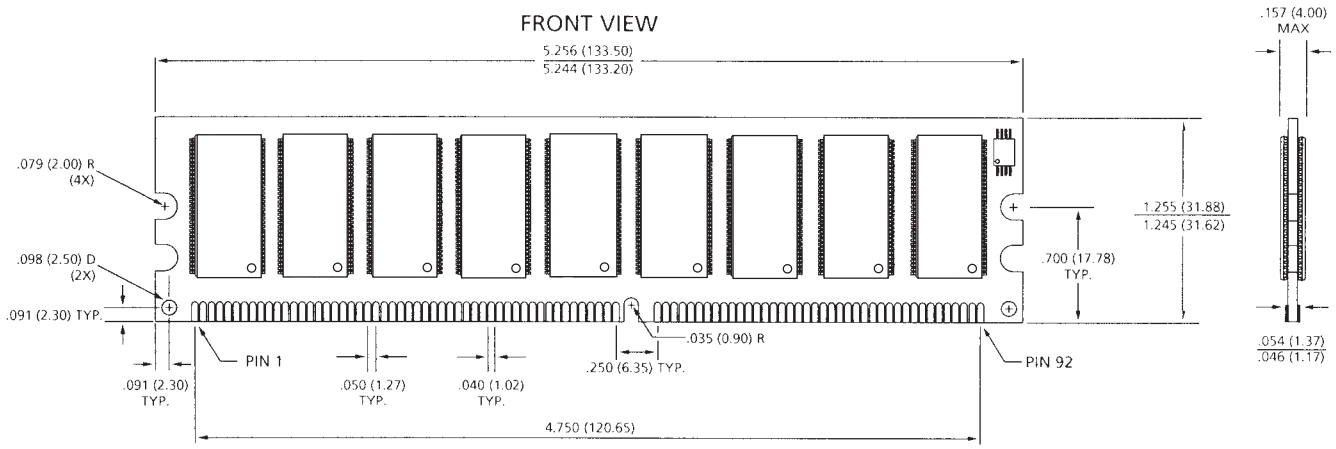


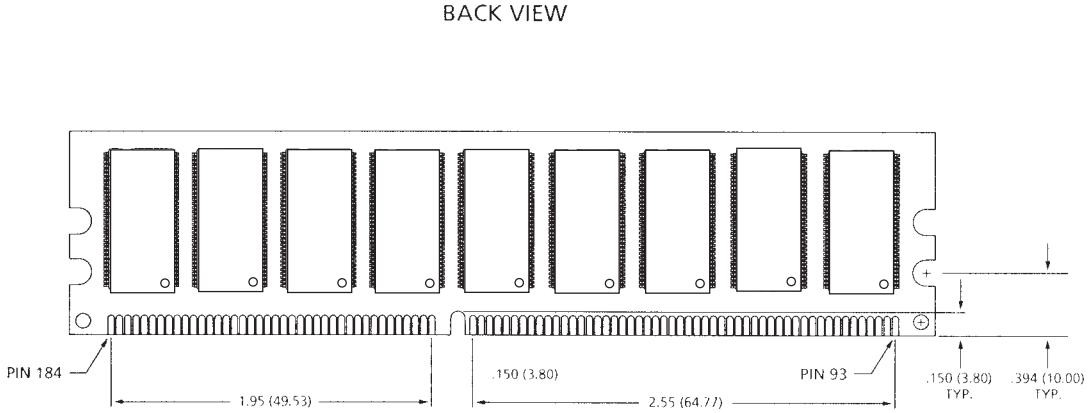
BACK VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

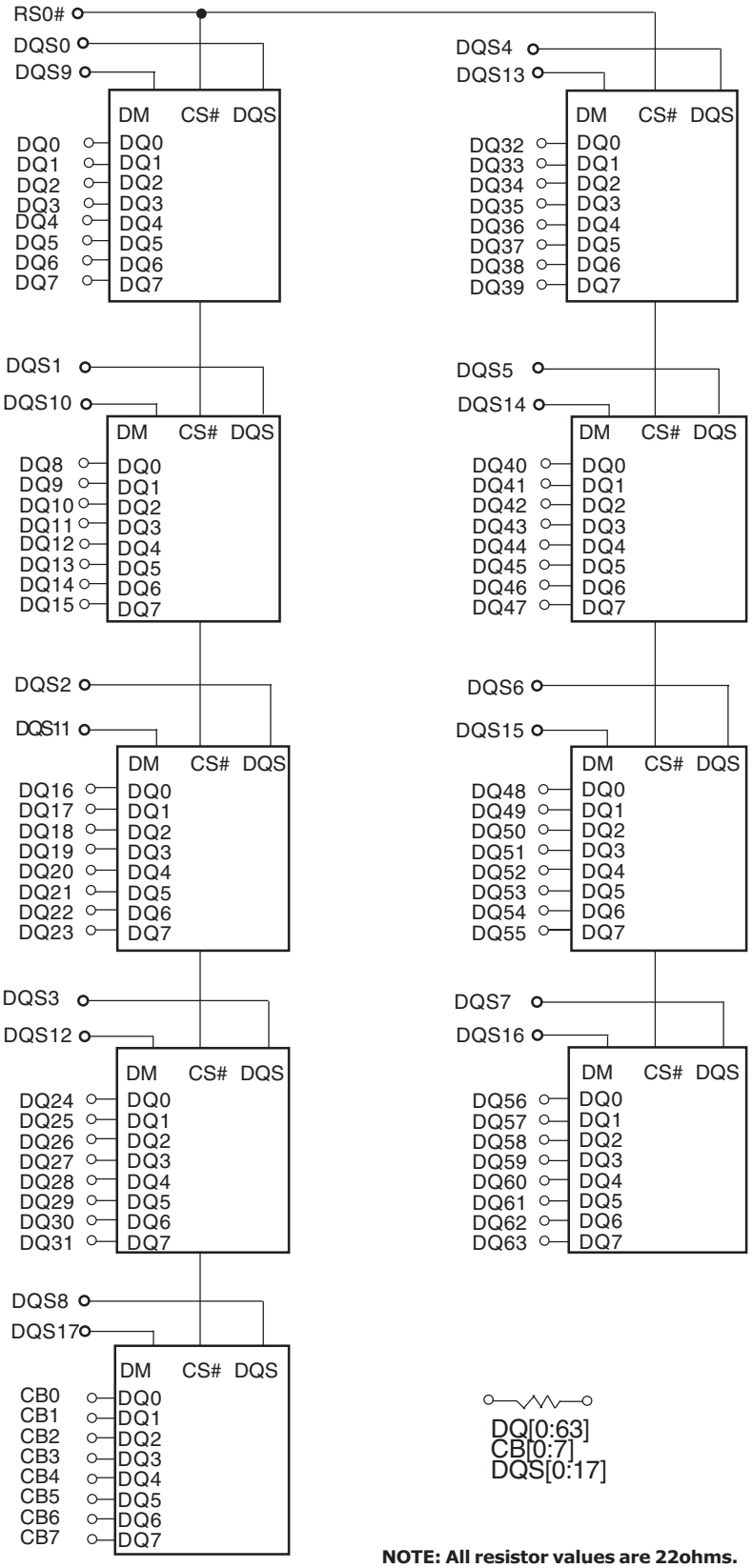
DTM63607 184-PIN DIMM





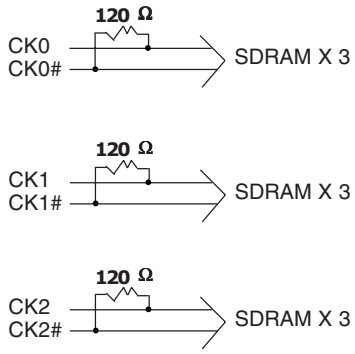
NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

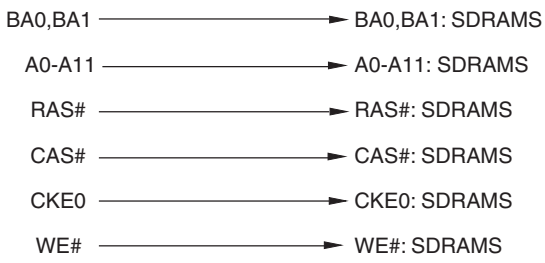
FUNCTIONAL BLOCK DIAGRAM OF THE DTM63607

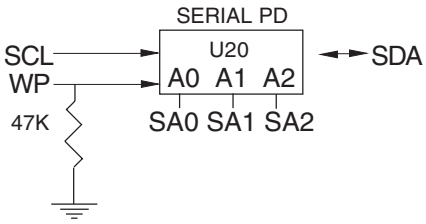


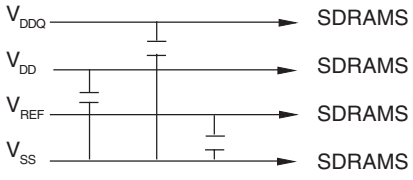
NOTE: All resistor values are 22ohms.

DTM63605

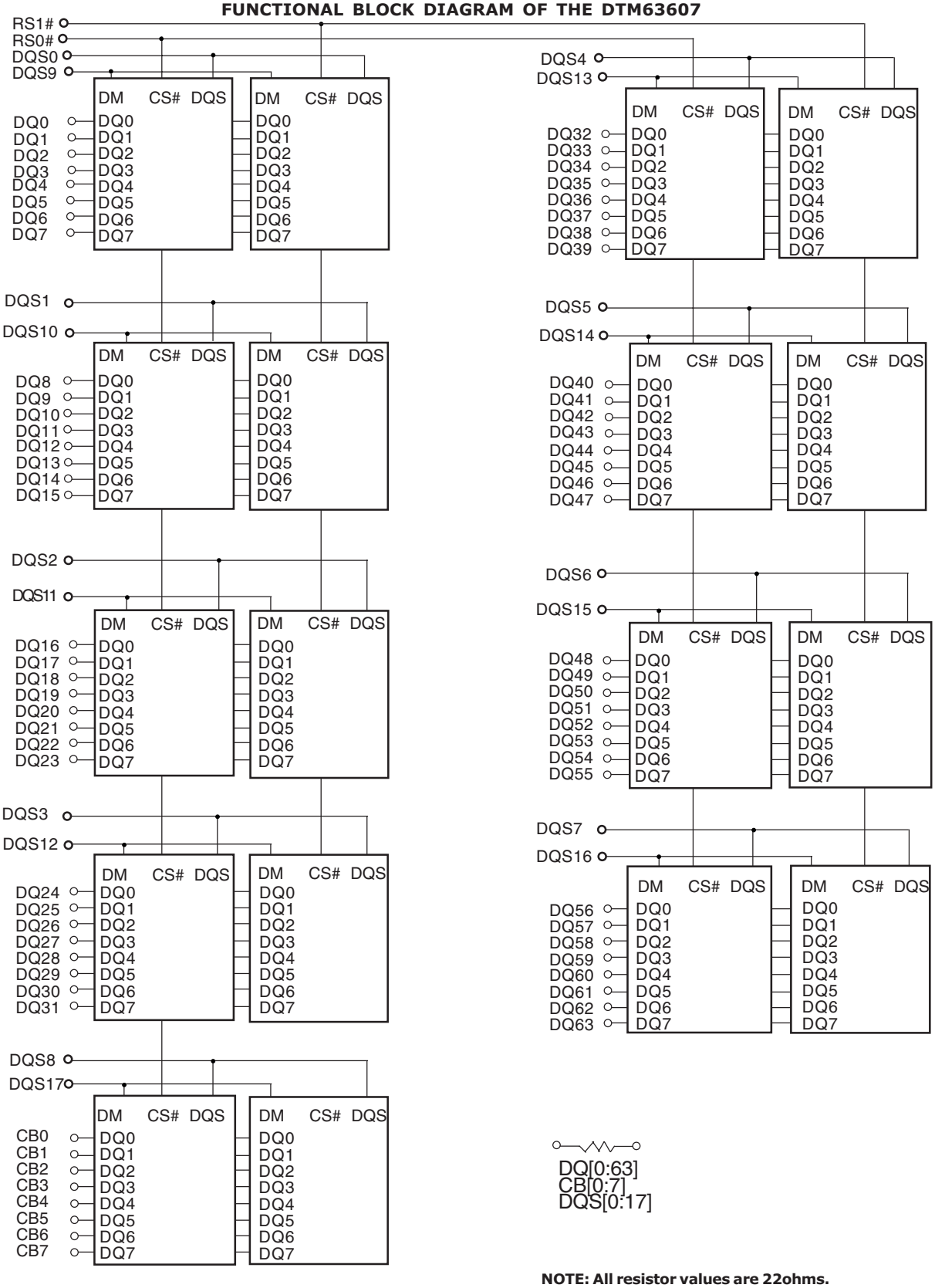

120 Ω
CK0
CK0#
SDRAM X 3
120 Ω
CK1
CK1#
SDRAM X 3
120 Ω
CK2
CK2#
SDRAM X 3


BA0,BA1
BA0,BA1: SDRAMS
A0-A11
A0-A11: SDRAMS
RAS#
RAS#: SDRAMS
CAS#
CAS#: SDRAMS
CKE0
CKE0: SDRAMS
WE#
WE#: SDRAMS


SERIAL PD
U20
SCL
WP
A0 A1 A2
SDA
47K
SA0 SA1 SA2

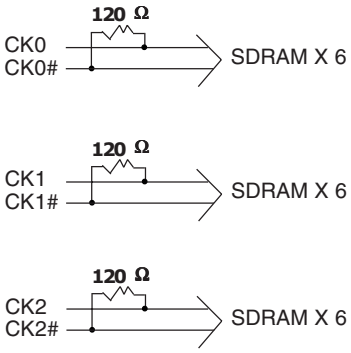

V_{DDQ}
SDRAMS
V_{DD}
SDRAMS
V_{REF}
SDRAMS
V_{SS}
SDRAMS

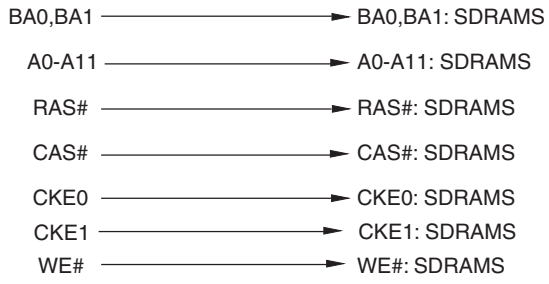
FUNCTIONAL BLOCK DIAGRAM OF THE DTM63607

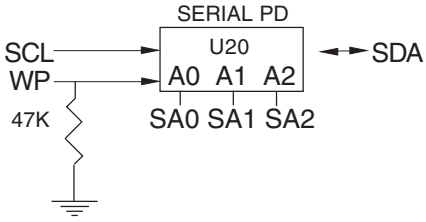


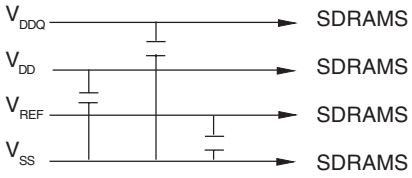
NOTE: All resistor values are 22ohms.

DTM63607


120 Ω
CK0
CK0#
SDRAM X 6
120 Ω
CK1
CK1#
SDRAM X 6
120 Ω
CK2
CK2#
SDRAM X 6


BA0,BA1
BA0,BA1: SDRAMS
A0-A11
A0-A11: SDRAMS
RAS#
RAS#: SDRAMS
CAS#
CAS#: SDRAMS
CKE0
CKE0: SDRAMS
CKE1
CKE1: SDRAMS
WE#
WE#: SDRAMS


SERIAL PD
U20
SCL
WP
A0 A1 A2
SDA
47K
SA0 SA1 SA2


V_{DDQ}
SDRAMS
V_{DD}
SDRAMS
V_{REF}
SDRAMS
V_{SS}
SDRAMS

Absolute maximum ratings

Voltage on V_{DD} Supply
Relative to V_{SS}.....-1V to +4.6V
Voltage on $V_{DD}Q$ Supply
Relative to V_{SS}.....-1V to +3.6V
Voltage on V_{REF} and Inputs
Relative to V_{SS}.....-1V to +3.6V
Voltage on I/O Pins
Relative to V_{SS}.....-0.5V to $V_{DD}Q$ +0.5V
Operating Temperature, T_A (ambient) ...0°C to +70°C
Storage Temperature (plastic) .....-55°C to + 150°C
Power Dissipation.....18W
Short Circuit Output Current.....50mA

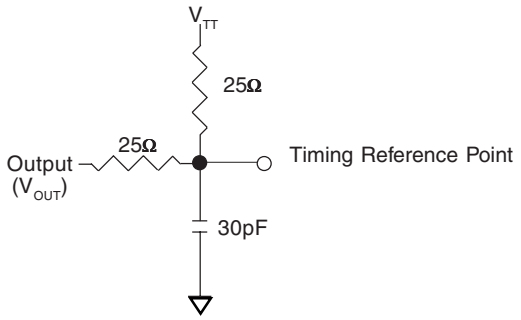
***Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

DC operating conditions and characteristics

(Notes: 1-6; notes appear below and on next page) (0°C ≤ T_A ≤ +70°C; V_{DD}=+2.5V ± 0.2V, $V_{DD}Q$ = +2.5V ± 0.2V)

		Symbol	Minimum	Maximum	Units	Notes
Supply voltage		V_{DD}	2.3	2.7	V	
I/O Supply Voltage		$V_{DD}Q$	2.3	2.7	V	
I/O Reference voltage		V_{REF}	0.49 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	7
I/O Termination voltage(system)		V_{TT}	V_{REF}-0.04	V_{REF} + 0.04	V	8
Input High (Logic 1) Voltage		V_{IH}	V_{REF}+0.18	V_{DD} + 0.3	V	9
Input Low (Logic 0) Voltage		V_{IL}	-0.3	V_{REF} - 0.18	V	9
Clock Input Voltage Level; CK0 and CK0#		V_{IN}	-0.3	$V_{DD}Q$ + 0.3	V	
Clock Input Differential Voltage; CK0 and CK0#		V_{ID}	0.36	$V_{DD}Q$ + 0.6	V	10
Clock Input Crossing Point Voltage; CK0 and CK0#		V_{IX}	1.15	1.35	V	11
INPUT LEAKAGE CURRENT **Any input 0V≤ V_{IN} ≤ V_{DD}** **(All other pins not under test=0V**	**WE#,RAS#,CAS#,BA0 BA1**	I_{11}	-36	36	uA	
	S0#,S1#,CKE0,CKE1	I_{12}	-18	18	uA	
	CK,CK#	I_{13}	-12	12		
OUTPUT LEAKAGE CURRENT **(DQ_S are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$**	**DQ0-DQ63, CB0-CB7 DQS0-DQS17**	I_{OZ}	-10	10	uA	
OUTPUT LEVELS **Output High Current (V_{OUT}=1.95V, maximum V_{TT})**		I_{OH}	-15.2	-	mA	
Output Low Current (V_{OUT}=0.35V, minimum V_{TT})		I_{OL}	15.2	-	mA	

NOTE: 1. All voltages referenced to V_{SS}.
2. Tests for AC timing. I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measure with equivalent load:



NOTES: (continued)

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (ie., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE $\leq$ 0.3x $V_{DD}Q$ is recognized as LOW.

7. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed $\pm$2 percent of the DC value. Thus, from $V_{DD}Q/2$, V_{REF} is allowed $\pm$25mV for DC error and $\pm$ 25mV for AC noise.

8. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

9. The DC values define where the input slew rate requirements are imposed, and the input signal, must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge.

10. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

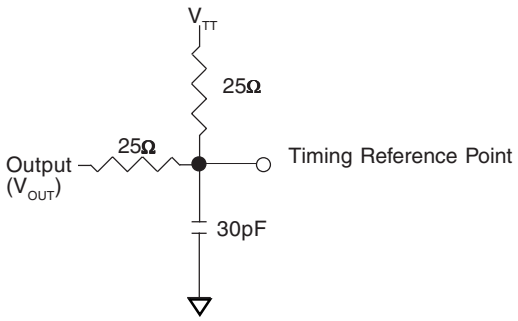
11. The value of V_{ix} is expected to equal $V_{DD}Q/2$ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING CONDITIONS

(Notes:1-6) (0°C ≤ T_A ≤ +70°C; V_{DD} = +2.5V ± 0.2V, $V_{DD}Q$=+2.5V ±0.2V)

PARAMETER/CONDITION	Symbol	Minimum	Maximum	Unit	Note
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.35	-	V	7,8
Input Low (Logic 0) Voltage	V_{IL}(AC)	-	V_{REF} - 0.35	V	7,8
Clock Input Differential Voltage; CK and CK#	V_{ID}(AC)	0.7	$V_{DD}Q$ + 0.6	V	9
Clock Input Crossing Point Voltage; CK and CK#	V_{IX}(AC)	0.5 X $V_{DD}Q$-0.2	0.5 X $V_{DD}Q$ + 0.2	V	10

Note:
1. All voltage referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equalivalent load:



NOTES: (continued)

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (ie., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE≤ 0.3x VDDQ is recognized as LOW.

7. Input slew rate=1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the V_{IL}(AC) maximum and V_{IH}(AC) minimum points. For slew rates between 0.5V/ns and 1V/ns, ^tIS and ^tIH must be increased by at least 20 percent.

8. The DC values define where the input slew rate requirements are imposed, and the input signal, must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge.

9. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

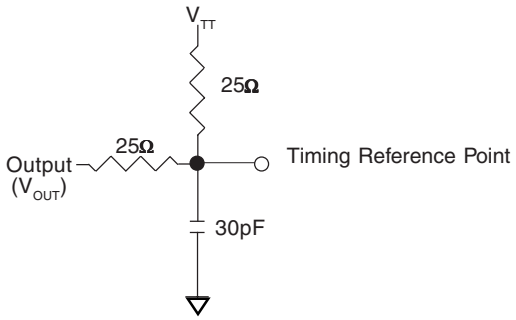
10. The value of Vix is expected to equal $V_{DD}Q/2$ of the transmitting device and must track variations in the DC level of the same.

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes:1-8; notes appear below and on next page)
(0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ± 0.2V, V_{DD}=+2.5V ±0.2V)

PARAMETER/CONDITION		Symbol	Size	266MHz	200MHz	Units	Notes
OPERATING CURRENT: One bank;Active-Precharge;^tRC= ^tRC MIN;^tCK=^tCK MIN; DQ,DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle; CL=2.5		IDD0	128MB	1,125	1,080	mA	9
			256MB	1,665	1,620		
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst=2; ^tRC=^tRC MIN; CL=2.5; ^tCK=^tCK MIN; L_{OUT}=0mA; Address and control inputs changing once per clock cycle		IDD1	128MB	900	900	mA	9
			256MB	1,440	1,440		
PRECHARGE POWER-DOWN STANDBY CURRENT:All banks idle; Power-down mode; CKE=LOW; ^tCK=^tCK MIN		IDD2P	128MB	270	270	mA	
			256MB	540	540		
IDLE STANDBY CURRENT: CS#=HIGH; All banks idle; CKE=HIGH; ^tCK=^tCK MIN; Address and other control inputs changing once per clock cycle		IDD2N	128MB	495	450	mA	
			256MB	990	900		
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; CKE=LOW; ^tCK=^tCK MIN		IDD3P	128MB	270	270	mA	
			256MB	540	540		
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH One bank; Active-Precharge; ^tRC=^tRAS MAX*; ^tCK=^tCK MIN; DQ,DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing one per clock cycle		IDD3N	128MB	540	540	mA	9
			256MB	1,080	1,080		
OPERATING CURRENT: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL=2.5; ^tCK=^tCK MIN;I_{OUT}=0mA		IDD4R	128MB	1,125	1,035	mA	
			256MB	1,665	1,575		
OPERATING CURRENT: Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL=2.5; ^tCK=^tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle		IDD4W	128MB	945	900	mA	
			256MB	1,485	1,440		
AUTO REFRESH CURRENT	^tRC=^tRFC MIN	IDD5	128MB	1,305	1,260	mA	9
			256MB	2,610	2,520		
	^tRC=15.625uS	IDD6	128MB	225	225	mA	10
			256MB	450	450		
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	IDD7	128MB	9	18	mA	11
			256MB	18	26		
	Low power (L)	IDD8	128MB	5.4	5.4	mA	11
			256MB	10.8	10.8		

NOTE: 1. All voltages referenced to V_{SS}.
2. Tests for AC timing. I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measure with equivalent load:



NOTES: (continued)

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (ie., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.

7. I_{DD} specifications are tested after the device is properly initialized.

8. Input slew rate=1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the VIL(AC) maximum and V_{IH}(AC) minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{t}IH must be increased by at least 20 percent.

9. MIN* (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS MAX* for IDD measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

10. This limit is actually a niminal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (ie., during standby).

11. Enables on-chip refresh and address counters.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS*

(Notes:1-9; notes appear below and on next page)
(0°C ≤ T_A ≤ +70°C; $V_{DD}Q$ = +2.5V ± 0.2V, V_{DD}=+2.5V ±0.2V)

AC CHARACTERISTICS			266MHz		200MHz			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access window of DQ_S from CK/CK#		tAC	-0.75	0.75	-0.8	0.8	ns	
CK high-level width		tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width		tCL	0.45	0.55	0.45	0.55	tCK	
Clock cycle time	CL=2.5	tCK	7.5	15	8	15	ns	
	CL=2	tCK	10	15	10	15	ns	
Auto precharge write recovery plus precharge time		tDAL	35		35		ns	
DQ and DM input hold time		tDH	0.5		0.6		ns	
DQ and DM input setup time		tDS	0.5		0.6		ns	
DQ and DM input pulse width (for each input)		tDIPW	1.75		2		ns	
Access window of DQS from CK/CK#		tDQSCK	-0.75	0.75	-0.8	0.8	ns	
DQS input high pulse width		tDQSH	0.35		0.35		tCK	
DQS input low pulse width		tDQSL	0.35		0.35		tCK	
DQS-DQ-DQ skew (first to last transition per access)		tDQSQ		0.5		0.6	ns	
Write command to first DQS latching transition		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		tCK	
DQ/DQS output valid window		tDV	0.35		0.35		tCK	10
Data-out high-impedance window from CK/CK#		tHZ	-0.75	0.75	-0.8	0.8	ns	11
Data-out low-impedance window from CK/CK#		tLZ	-0.75	0.75	-0.8	0.8	ns	11
Address and control input hold time		tIH	0.75		1.1		ns	12
Address and control input setup time		tIS	0.75		1.1		ns	12
Address and control input pulse width		tIPW	2		2.5		ns	
LOAD MODE REGISTER command cycle time		tMRD	15		16		ns	
ACTIVE to PRECHARGE command		tRAS	45	120K	50	120K	ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		tRC	65		70		ns	
AUTO REFRESH to ACTIVE/AUTO REFRESH command period		tRFC	75		80		ns	
REFRESH to REFRESH command interval		tREFC		31.2		31.2	us	13
Average periodic refresh interval		tREFI		15.6		15.6	us	13
ACTIVE to READ or WRITE delay		tRCD	20		20		ns	
PRECHARGE command period		tRP	20		20		ns	
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank a to active bank b command		tRRD	15		15		ns	
Terminating voltage delay to V_{DD}		tVTD	0		0		ns	
DQS Write preamble		tWPRE	0.25		0.25		tCK	
DQS write preamble setup time		tWPRES	0		0		ns	14,15
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	16
DQS write recovery time		tWR	15		15		ns	
Internal WRITE to READ command delay		tWTR	1		1		tCK	
Exit SELF REFRESH to non-READ command		tXSNR	75		80		ns	
Exit SELF REFRESH to read command		tXSRD	200		200		tCK	

NOTES: (continued)

4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (ie., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).

6. Input slew rate=1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the V_{IL}(AC) maximum and V_{IH}(AC) minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{T}IH must be increased by at least 20 percent.

7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.

8. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE≤0.3x V_{DD}Q is recognized as LOW.

9. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.

10. ^{t}DV is derived assuming a 45/55 clock HIGH-to-LOW ratio. The ^{t}DV is improved directly proportional to the reduction in the clock HIGH-to-LOW ratio.

11. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

12. Input slew rate=1V/ns. If the slew rate exceeds the maximum specified by 20 percent, functionality is uncertain. If the slew rate exceeds the minimum specified, timing is no longer referenced to the mid-point but to the V_{IL}(AC) maximum and V_{IH}(AC) minimum points. For slew rates between 0.5V/ns and 1V/ns, ^{t}IS and ^{T}IH must be increased by at least 20percent.

13. The refresh period is 64ms. This equates to an average refresh rate of 15.625us. Howerver an AUTO REFRESH command must be asserted at least once every 31.2us; burst refreshing or postings greater than 2 are not allowed.

14. The minimum limit for this parameter is not a device limit. The device will operate with a negative value for this parameter, but system performance (bus turnaround) will degrade accordingly.

15. The specific requirement is that DQS be valid (HIGH or LOW) on or before this CK edge. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be high at this time, depending on ^{t}DQSS.

16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

CAPACITANCE

		128MB		256MB		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**Units**
Input/Output Capacitance: DQs,DQSs,CBs	CI0	5.0	7.0	10.0	14.0	pf
Input Capacitance: CK, CK#	CI1	9	12	18	24	pf
Input Capacitance: A0-A11, BA0/1, RAS#, CAS#, WE#	CI2	24	33	48	66	pf
Input Capacitance: S0#, S1#, CKE0, CKE1	CI3	24	33	24	33	pf

Note: This parameter is sampled. V_{DD}=+2.5V ± 0.2V, $V_{DD}Q$ = +2.5V ± 0.2V, f=100MHz, T_A= 25°C, $V_{OUT(DC)}=V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.