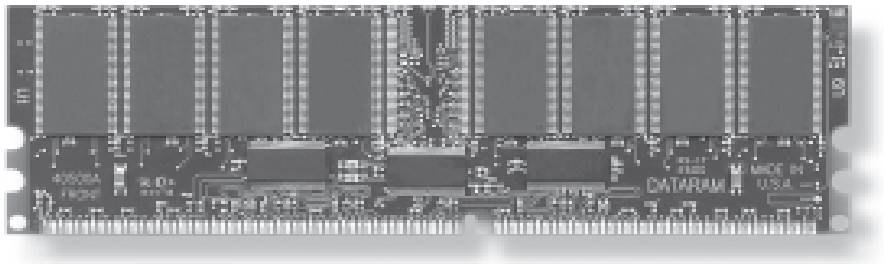
DTM63602,63603

128MB-16M x 64, 256MB-32M x 64, 184 Pin Registered DDR SDRAM DIMMs



Identification

DTM63602:16Mx64
DTM63603:32Mx64

Performance range

266MHz(CL=2.5)
200MHz(CL=2)

Features

- Utilizes 133MHz DDR SDRAM
- Auto & self refresh capability
- SSTL_2 compatible inputs and outputs
- VDD/VDDQ=2.5V+/-0.2V
- MRS cycle, with address key, programs Latency (Access from column address) Burst length (2, 4 and 8 page)
- Data scramble (Sequential & Interleave)
- Serial Presence Detect
- 184-pin JEDEC DIMM double-sided assembly, 5.250" wide by 1.7" high
- Commands entered on each positive CK edge
- DQS edge-aligned with data for Reads; center-aligned with Data for Writes
- Two Data accesses per clock cycle
- DTM63600 is two Physical Banks
- DTM63601 is one Physical Bank
- SDRAM Addressing (12/10/2)(Row/Col/Bank)

Description

The Dataram DTM63602 assembly is a Registered DDR Synchronous Dynamic RAM high density memory module. The DTM63602 consists of sixteen CMOS monolithic 16M x 8bit DDR Synchronous DRAMS in a 66pin TSOP-II 400mil package. Two 14-bit Registers and one PLL. The Dataram DTM63603 assembly is a Registered 16Mx64 DDR Synchronous Dynamic RAM high density memory module. The DTM63603 consists of eight CMOS monolithic 16M x 8bit DDR Sychronous DRAMs in a 66 pin TSOP-II 400mil package. Two 14-bit Registers and one PLL.One 2K EEPROM for serial presence detect is used on all assemblies. These DDR SDRAM modules use a double data rate architecture to achieve high speed operation. Synchronous design allows for precise cycle control with the use of a differential system clock.

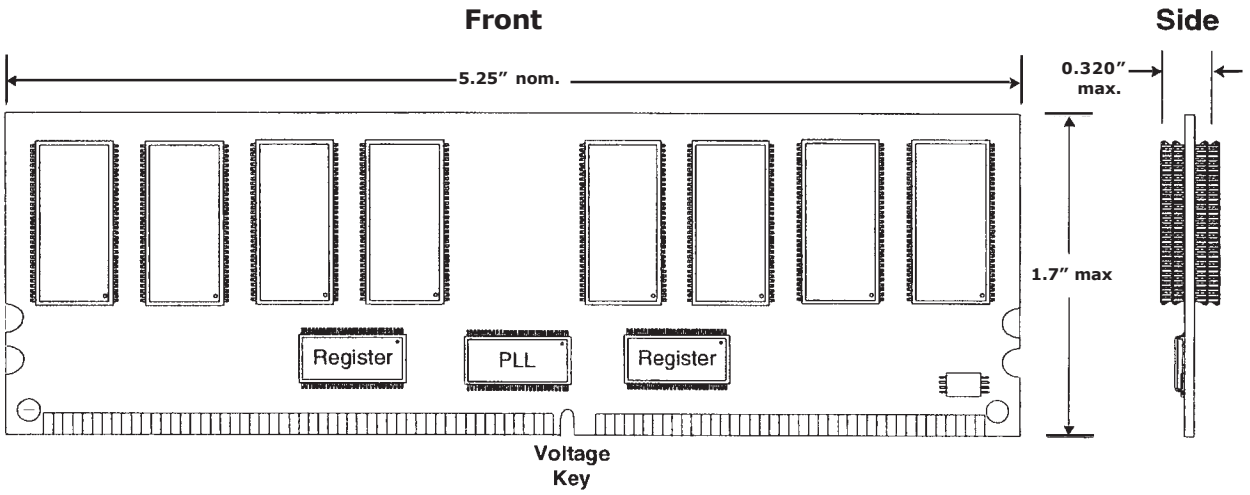
Pin configurations

Front side								Back side							
1	VREF	24	DQ17	47	DQS8*	70	VDD	93	Vss	116	VSS	139	VSS	162	DQ46
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DQS17*	163	DQ47
3	VSS	26	VSS	49	CB2*	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DQS11	142	CB6*	165	DQ52
5	DQS0	28	DQ18	51	CB3*	74	VSS	97	DQS9	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	NC	98	DQ6	121	DQ22	144	CB7*	167	NC
7	VDD	30	VDDQ	53	DQ32	76	NC	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DQS15
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	/RESET	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	DQ55
11	VSS	34	VSS	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DQS13	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	VDDID	105	DQ12	128	VDDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DQS12	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DQS10	130	A3	153	DQ44	176	VSS
16	NC	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS	177	DQS16
17	NC	40	DQ27	63	WE	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS#	88	DQ59	111	CKE1	134	CB4*	157	S0	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5*	158	S1	181	SA0
21	CKE0	44	CB0*	67	DQS5	90	WP	113	NC	136	VDDQ	159	DQS14	182	SA1
22	VDDQ	45	CB1*	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	A12	138	/CK0	161	DQ46	184	VDDSPD

NC=No Connect ***=Not Used**

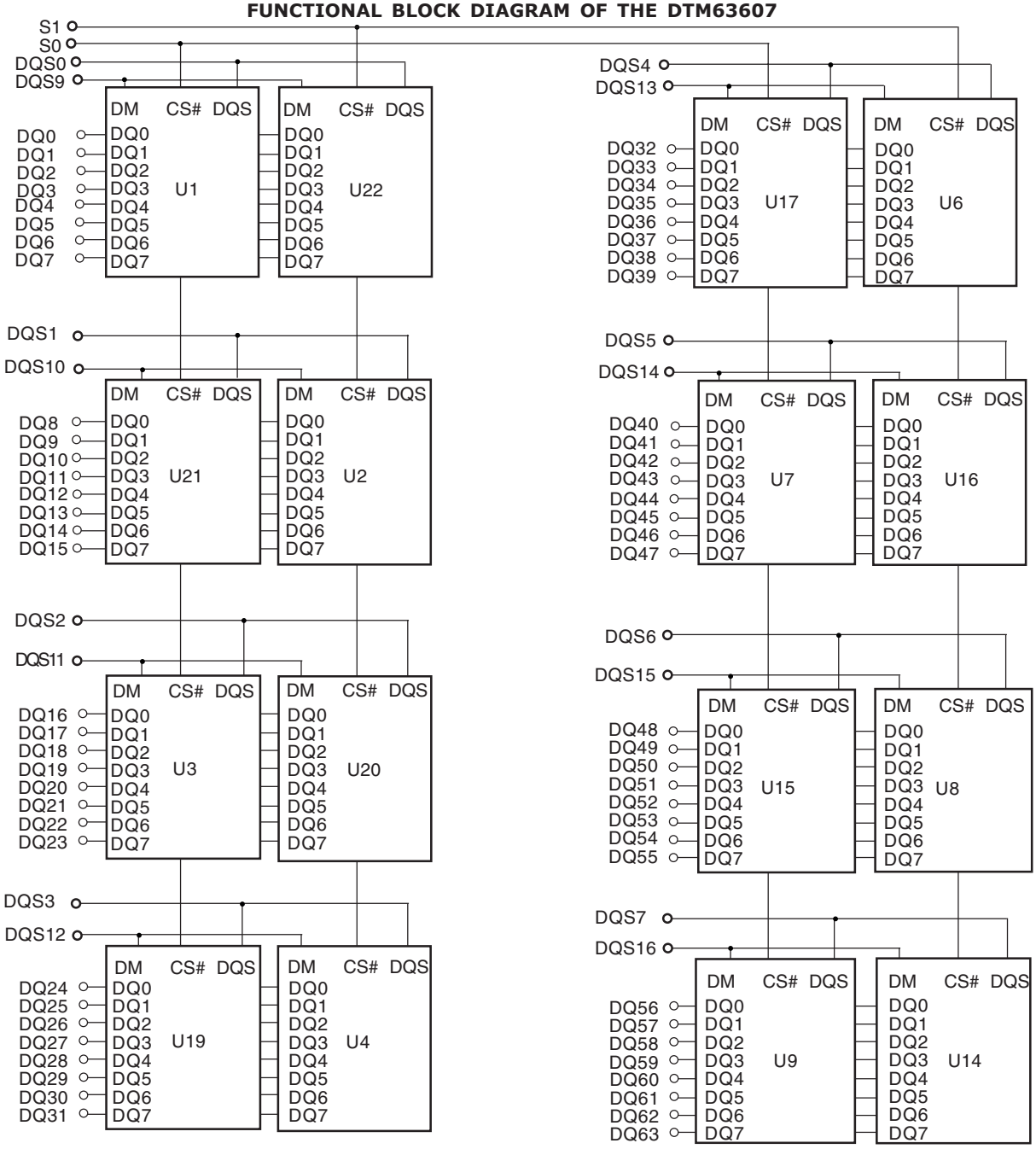
Pin names

Pin name	Function
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
CK0,S	Chip select
CK0	Differential Clock Inputs
CKE[1:0]	Clock enable input
BA[1:0]	Bank Select Input
A[11:0]	Address input (Multiplexed)
VREF	SSTL_2 reference input
VDDID	VDD identification flag
SCL	Serial clock
SDA	Serial data I/O
SA[2:0]	Address EEPROM
DQS[16:9,7:0]	Data Strobes/masks
DQ[63:0]	Data I/Os: Data bus
VDDQ	DQ power supply: 2.5V +/-.2V
VDD	Power supply: 2.5V +/-.2V
VSS	Ground
VDDSPD	Serial EEPROM power supply
/RESET	Reset Enable
NC	No connects



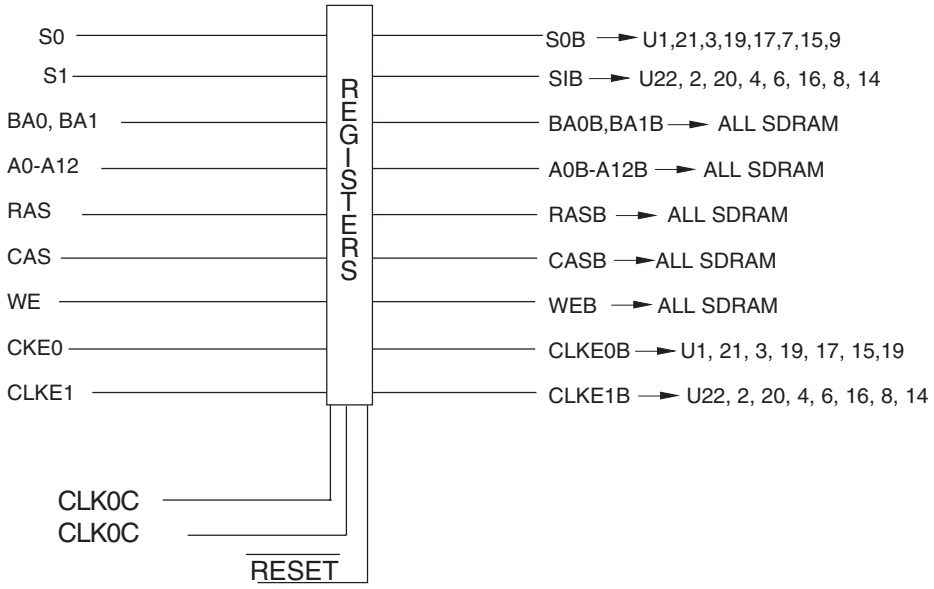
Note:
The keying in this example defines the DIMM as a 2.5V V_{DD}/V_{DDQ} DDR DIMM.
- **The key position defines the voltage for the DIMM: Left=2.5 Volt $V_{DDQ.}$**

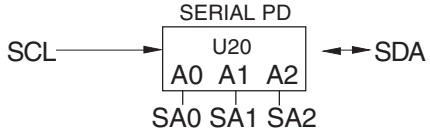
FUNCTIONAL BLOCK DIAGRAM OF THE DTM63607

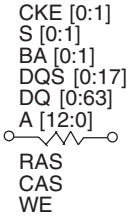


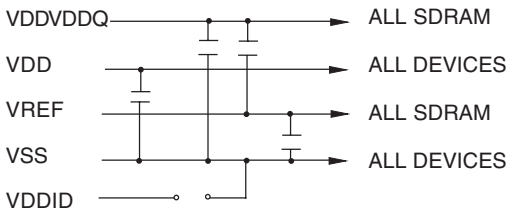
NOTES:

1.DQ/DQS resistors are 22 Ohms.
2.VDDID strap connections(formemory device VDD, VDDQ);
strap out :(open) : VDD=VDDQ
strap in (VSS) : VDD≠VDDQ
3. S0 and S1 alternate btw the back and front sides of the DIMM
4. Address and control resistors should be 22 Ohms


S0
S1
BA0, BA1
A0-A12
RAS
CAS
WE
CKE0
CLKE1
REGISTERS
CLK0C
CLK0C
RESET
S0B → U1,21,3,19,17,7,15,9
SIB → U22, 2, 20, 4, 6, 16, 8, 14
BA0B,BA1B → ALL SDRAM
A0B-A12B → ALL SDRAM
RASB → ALL SDRAM
CASB → ALL SDRAM
WEB → ALL SDRAM
CLKE0B → U1, 21, 3, 19, 17, 15,19
CLKE1B → U22, 2, 20, 4, 6, 16, 8, 14


SERIAL PD
SCL
U20
A0 A1 A2
SDA
SA0 SA1 SA2


CKE [0:1]
S [0:1]
BA [0:1]
DQS [0:17]
DQ [0:63]
A [12:0]
RAS
CAS
WE


VDDVDDQ
ALL SDRAM
VDD
ALL DEVICES
VREF
ALL SDRAM
VSS
ALL DEVICES
VDDID

DC OPERATING CONDITIONS

(T_A = 0 to 70°C, Voltage referenced to V_{SS}= 0V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Power Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.15	-	V_{DDQ}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	V_{REF}-0.15	V	2
Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	
Reference Voltage	V_{REF}	1.15	1.25	1.35	V	3

Notes:
(1) V_{DDQ} must not exceed the level of V_{DD}.
(2) V_{IL} (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
(3) The value of V_{REF} is approxiametely equal to 0.5V_{DDQ}.

AC OPERATING CONDITIONS

(T_A = 0 to 70°C, Voltage referenced to V_{SS}= 0V)

Parameter	Symbol	Minimum	Maximum	Unit	Note
Input High (Logic 1) Voltage, DQ,DQS and DM signals	$V_{IH(AC)}$	VREF=0.31		V	
Input Low (Logic 0) Voltage, DQ,DQS and DM signals	$V_{IL(AC)}$		VREF=0.31	V	
Input Differential Voltage, CK and/CK inputs	$V_{ID(AC)}$	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and/CK inputs	$V_{IX(AC)}$	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note:
(1) VID is the magnitude of the difference between the input level on CK and the input on CK.
(2)The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS

(T_A = 0 to 70°C, Voltage referenced to V_{SS}= 0V)

Parameter	Value	Unit
Reference Voltage	V_{DDQ} x 0.5	V
Termination Voltage	V_{DDQ} x 0.5	V
AC Input High Level Voltage (V_{IH},min)	V_{REF} + 0.31	V
AC Input Low Level Voltage (V_{IL},max)	V_{REF} - 0.31	V
Input Timing Measurement Reference Level Voltage	V_{REF}	V
Output Timing Measurement Reference Level Voltage	V_{TT}	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (R_T)	50	Ω
Series Resistor (R_S)	22	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

CAPACITANCE(DTM63602)

(T_A = 25°C, f=100MHz)

Parameter	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance	A0~A11,BA0,BA1	CIN1	5	9	pF
Input Capacitance	RAS, CAS, WE	CIN2	5	9	pF
Input Capacitance	CKE0, CKE1	CIN3	5	9	pF
Input Capacitance	CS0, CS1	CIN4	5	9	pF
Input Capacitance	CK0, CK0	CIN5	5	9	pF
Input Capacitance	DM[0:7,9:16]	CIN6	14	18	pF
Data Input/Output Capacitance	DQ0~DQ63, DQS0~DQS8	CIO1	14	18	pF

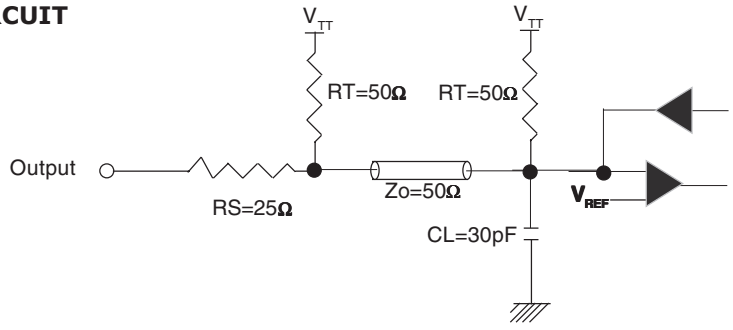
CAPACITANCE(DTM63603)

(T_A = 25°C, f=100MHz)

Parameter	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance	A0~A11,BA0,BA1	CIN1	5	9	pF
Input Capacitance	RAS, CAS, WE	CIN2	5	9	pF
Input Capacitance	CKE0, CKE1	CIN3	5	9	pF
Input Capacitance	CS0	CIN4	5	9	pF
Input Capacitance	CK0, CK0	CIN5	5	9	pF
Input Capacitance	DM[0:7,9:16]	CIN6	7	9	pF
Data Input/Output Capacitance	DQ0~DQ63, DQS0~DQS8	CIO1	7	9	pF

NOTE: 1. VDD=min. to max., VDDQ=2.3V to 2.7V, VODC=VDDQ/2, VOpeak-to-peak=0.2V
2. Pins not under test are tied tto GND.
3. These values are guaranteed by design and are tested on a sample basis only

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I

(T_A = 0 to 70°C, Voltage referenced to V_{SS}= 0V)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current	I_{LI}	-5	5	uA	1
Output Leakage Current	I_{LO}	-5	5	uA	2
Output High Voltage	V_{OH}	V_{TT} + 0.76	-	V	IOH=-15.2mA
Ouyput Low Voltage	V_{OL}	-	V_{TT}-0.76	V	IOL=+15.2mA

Note: 1. V_{IN}=0 to 3.6V, All other pins are not tested under V_{IN}=0V
2. D_{OUT} is disabled, V_{OUT}=0 to 2.7V
3. These values are device characteristics.

DC CHARACTERISTICS II(DTM63602)

(T_A = 0 to 70°C, Voltage referenced to V_{SS}= 0V)

Parameter	Symbol	Test Condition		Speed	Unit	Note
Operating Current	IDD1	Burst length=2, One bank active tRC ≥ tRC(min), I_{OL}=0mA		2238	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ V_{IL}(max),tCK=min		320	mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ V_{IH}(min),CS ≥ V_{IH}(min),tCK=min Input signals are changed one time during 2clks		640	mA	
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ V_{IL}(max), tCK=min		400	mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ V_{IH}(min),CS ≥ V_{IH}(min),tCK=min Input signals are changed one time during 2clks		800	mA	
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), I_{OL}=0mA All banks active	CL=2.5	4155	mA	
			CL=2	3357		
Auto Refresh Current	IDD5	tRC ≥ tRFC(min), All banks active		5115	mA	1,2
Self Refresh Current	IDD6	CKE ≤ 0.2V		32	mA	

NOTE: 1. IDD1, IDD4 and IDD5 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRFC)Auto Refresh Row Cycle Time) is shown at AC CHARACTERISTICS.

DC CHARACTERISTICS II(DTM63603)

(T_A = 0 to 70°C, Voltage referenced to V_{SS}= 0V)

Parameter	Symbol	Test Condition		Speed	Unit	Note
Operating Current	IDD1	Burst length=2, One bank active tRC ≥ tRC(min), I_{OL}=0mA		1120	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ V_{IL}(max),tCK=min		160	mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ V_{IH}(min),CS ≥ V_{IH}(min),tCK=min Input signals are changed one time during 2clks		320	mA	
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ V_{IL}(max), tCK=min		200	mA	
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ V_{IH}(min),CS ≥ V_{IH}(min),tCK=min Input signals are changed one time during 2clks		400	mA	
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), I_{OL}=0mA All banks active	CL=2.5	2078	mA	
			CL=2	1679		
Auto Refresh Current	IDD5	tRC ≥ tRFC(min), All banks active		2558	mA	1,2
Self Refresh Current	IDD6	CKE ≤ 0.2V		16	mA	

NOTE: 1. IDD1, IDD4 and IDD5 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRFC)Auto Refresh Row Cycle Time) is shown at AC CHARACTERISTICS.

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER		Symbol	Min	Max	Unit	Note
Row Cycle Time		tRC	65	-	ns	
Auto Refresh Row Cycle Time		tRFC	75	-	ns	
Row Active Time		tRAS	48	120K	ns	
Row Address to Column Address Delay		tRCD	20	-	ns	
Row Active to Row Active Delay		tRRD	15	-	ns	
Column Address to Column Address Delay		tCCD	1	-	CLK	
Row Precharge Time		tRP	20	-	ns	
Write Recovery Time		tWR	15	-	ns	
Last Data-In to Read Command		tDRL	1	-	CLK	
Auto Precharge Write Recovery + Precharge Time		tDAL	35	-	ns	
System Clock Cycle Time	$\overline{CAS}$ Latency = 2.5	tCK	7.5	15	ns	
	$\overline{CAS}$ Latency = 2		10	15	ns	
Clock High Level Width		tCH	0.45	0.55	CLK	
Clock Low Level Width		tCL	0.45	0.55	CLK	
Data-Out edge to Clock edge Skew		tAC	-0.75	0.75	ns	
DQS-Out edge to Clock edge skew		tDQSCK	-0.75	0.75	ns	
DQS-Out edge to Data-out edge skew		tDQSQ	-	0.5	ns	
Data-Out hold time from DQS		tQH	tHPmin -0.75ns	-	ns	1
Clock Half Period		tHP	tCH/L min	-	ns	1
Input Setup Time (fast slew rate)		tIS	0.9	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		tIH	0.9	-	ns	2,3,5,6
Input Setup Time (slow slew rate)		tIS	1.0	-	ns	2,4,5,6
Input Hold Time (slow slew rate)		tIH	1.0	-	ns	2,4,5,6
Input Pulse Width		tIPW	2.2	-	ns	6
Write DQS High Level Width		tDQSH	0.4	0.6	CLK	
Write DQS Low Level Width		tDQSL	0.4	0.6	CLK	
CLK to First Rising edge of DQS-In		tDQSS	0.75	1.25	CLK	
Data-In Setup Time to DQS-In (DQ & DM)		tDS	0.5	-	ns	7
Data-In Hold Time to DQS-In (DQ & DM)		tDH	0.5	-	ns	7

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER	Symbol	Min	Max	Unit	Note
DQ & DM Input Pulse Width	tDIPW	1.75	-	ns	
Read DQS Preamble Time	tRPRE	0.9	1.1	CLK	
Read DQS Postamble Time	tRPST	0.4	0.6	CLK	
Write DQS Preamble Setup Time	tWPRES	0-	-	CLK	
Write DQS Preamble Hold Time	tWPREH	0.25	-	CLK	
Write DQS Postamble Time	tWPST	0.4	0.6	CLK	
Mode Register Set Delay	tMRD	2	-	CLK	
Power Down Exit Time	tPDEX	10	-	ns	
Exit Self Refresh to Non-Read Command	tXSNR	75	-	ns	
Exit Self Refresh to Read Command	tXSRD	200	-	CLK	8
Average Periodic Refresh Interval	tREFI	-	15.6	us	

Note:
1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock: A0~A11, BA0~BA1, CKE, S0, S1, RAS, CAS, WE
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
5. CK,/CK slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(DQS)
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN,VOUT	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDD	-0.5 ~ 0.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	18	W
Soldering Temperature Time	TSOLDER	260 10	°C

Note:Operation at above absolute maximum rating can adversely affect device reliability

SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	S0,S1	RAS	CAS	WE	ADDR	A10/AP	BA	Note
Ambient Temperature		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	x			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	H	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	H	L	CA	L	V	1
Write with Autoprecharge									H		1,4
PrechargeAll Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge Selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

1. DM states are "Don't Care". Refer to below Write Mask Truth Table.
2.OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Registering during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after ^{t}RP period from Precharge command.
3.If a read with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+^{t}RP).
4. If a Write with Autoprecharge command is detected by memory component in CLK(n), then there will be no command presented to activated bank until CLK(n+BL/2+1+^{t}DPL+^{t}RP). Last Data-In to Precharge delay(^{t}DPL) which is also called Write Recovery Time (^{t}WR) is needed to guarantee that the last data has been completely written.
5.If 10/AP id "High" when Row Precharge command being issued, BA 0/BA1 are ignored and all banks are selected to be precharged.