

Identification

Part number: DTM60287

Performance range

100MHz (10ns@ CL=2)

Features

Burst mode operation

Auto & self refresh capability (4096 Cycles/64ms)

LVTTL compatible inputs and outputs

Single 3.3V±0.3V power supply

MRS cycle with address key programs Latency (Access from column address) Burst length (1, 2, 4 & 8 page) Data scramble (Sequential & Interleave)

Serial presence detect with EEPROM

168-pin PC100 DIMM double-sided assembly
5.250" wide by 1.70" high

Description

The Dataram DTM60287 Assembly is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The DTM60287 consists of eighteen CMOS Monolithic 16M x 8 bit Synchronous DRAMs in two TSOP-II 400MII packages, three 20-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8 pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. The DATARAM DTM60287 is a Dual in-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Pin configurations

Front side			Back side		
1 Vss	29 DQM1	57 DQ18	85 Vss	113 DQM5	141 DQ50
2 DQ0	30 CS0	58 DQ19	86 DQ32	114 CS1	142 DQ51
3 DQ1	31 DU	59 Vdd	87 DQ33	115 RAS	143 Vdd
4 DQ2	32 Vss	60 DQ20	88 DQ34	116 Vss	144 DQ52
5 DQ3	33 A0	61 NC	89 DQ35	117 A1	145 NC
6 Vdd	34 A2	62 *Vref	90 Vdd	118 A3	146 *Vref
7 DQ4	35 A4	63 *CKE1	91 DQ36	119 A5	147 REGE
8 DQ5	36 A6	64 Vss	92 DQ37	120 A7	148 Vss
9 DQ6	37 A8	65 DQ21	93 DQ38	121 A9	149 DQ53
10 DQ7	38 A10/AP	66 DQ22	94 DQ39	122 BA0	150 DQ54
11 DQ8	39 BA1	67 DQ23	95 DQ40	123 A11	151 DQ55
12 Vss	40 Vdd	68 Vss	96 Vss	124 Vdd	152 Vss
13 DQ9	41 Vdd	69 DQ24	97 DQ41	125 *CLK1	153 DQ56
14 DQ10	42 CLK0	70 DQ25	98 DQ42	126 *A12	154 DQ57
15 DQ11	43 Vss	71 DQ26	99 DQ43	127 Vss	155 DQ58
16 DQ12	44 DU	72 DQ27	100 DQ44	128 CKE0	156 DQ59
17 DQ13	45 CS2	73 Vdd	101 DQ45	129 CS3	157 Vdd
18 Vdd	46 DQM2	74 DQ28	102 Vdd	130 DQM6	158 DQ60
19 DQ14	47 DQM3	75 DQ29	103 DQ46	131 DQM7	159 DQ61
20 DQ15	48 DU	76 DQ30	104 DQ47	132 *A13	160 DQ62
21 CB0	49 Vdd	77 DQ31	105 CB4	133 Vdd	161 DQ63
22 CB1	50 NC	78 Vss	106 CB5	134 NC	162 Vss
23 Vss	51 NC	79 *CLK2	107 Vss	135 NC	163 *CLK3
24 NC	52 CB2	80 NC	108 NC	136 CB6	164 NC
25 NC	53 DB3	81 WP	109 NC	137 CB7	165 **SA0
26 Vdd	54 Vss	82 **SDA	110 Vdd	138 Vss	166 **SA1
27 WE	55 DQ16	83 **SCL	111 CAS	139 DQ48	167 **SA2
28 DQM0	56 DQ17	84 Vdd	112 DQM4	140 DQ49	168 Vdd

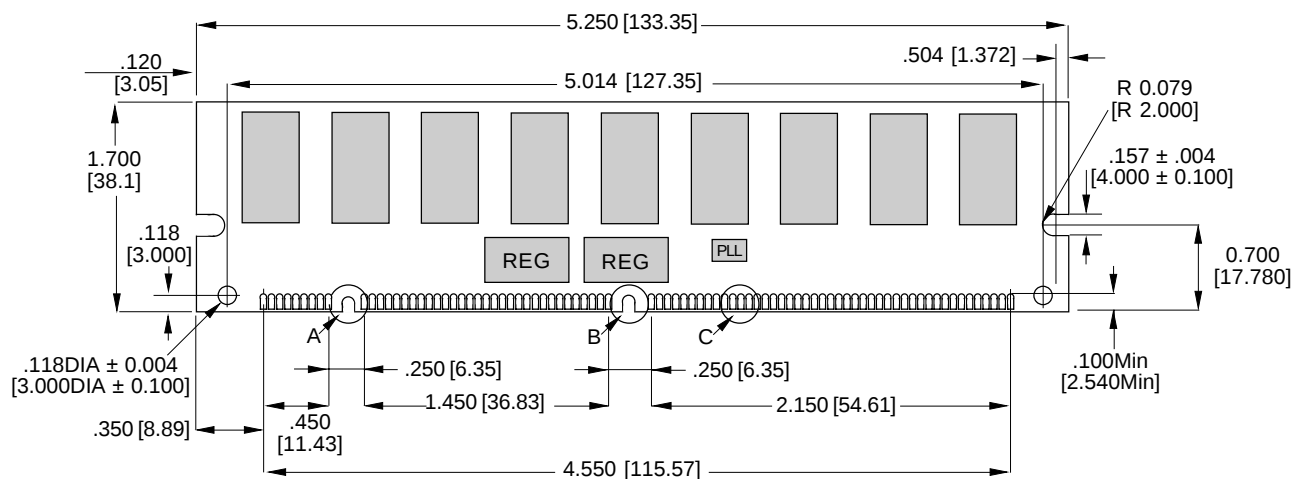
Pin names

Pin name	Function
A0-A11	Address input (Multiplexed)
BA0-BA1	Select bank
DQ0-DQ63	Data input/output
CB0-CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0-CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0-7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
Vref	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0-2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

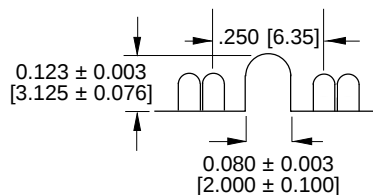
* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

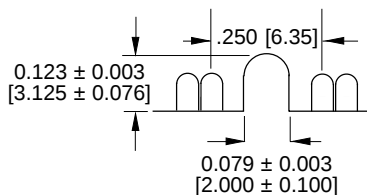
Front view



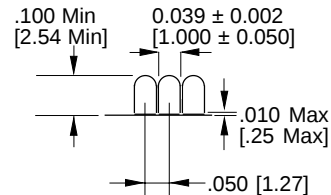
Detail A



Detail B

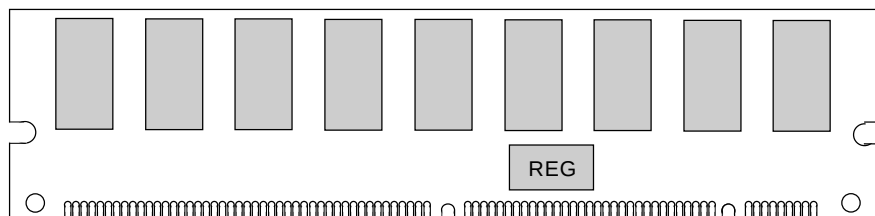


Detail C



Units: Inches (Millimeters)

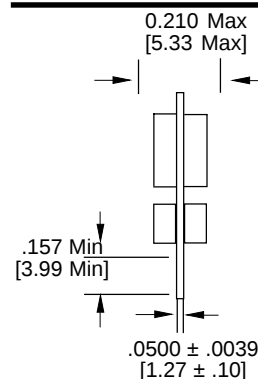
Back view

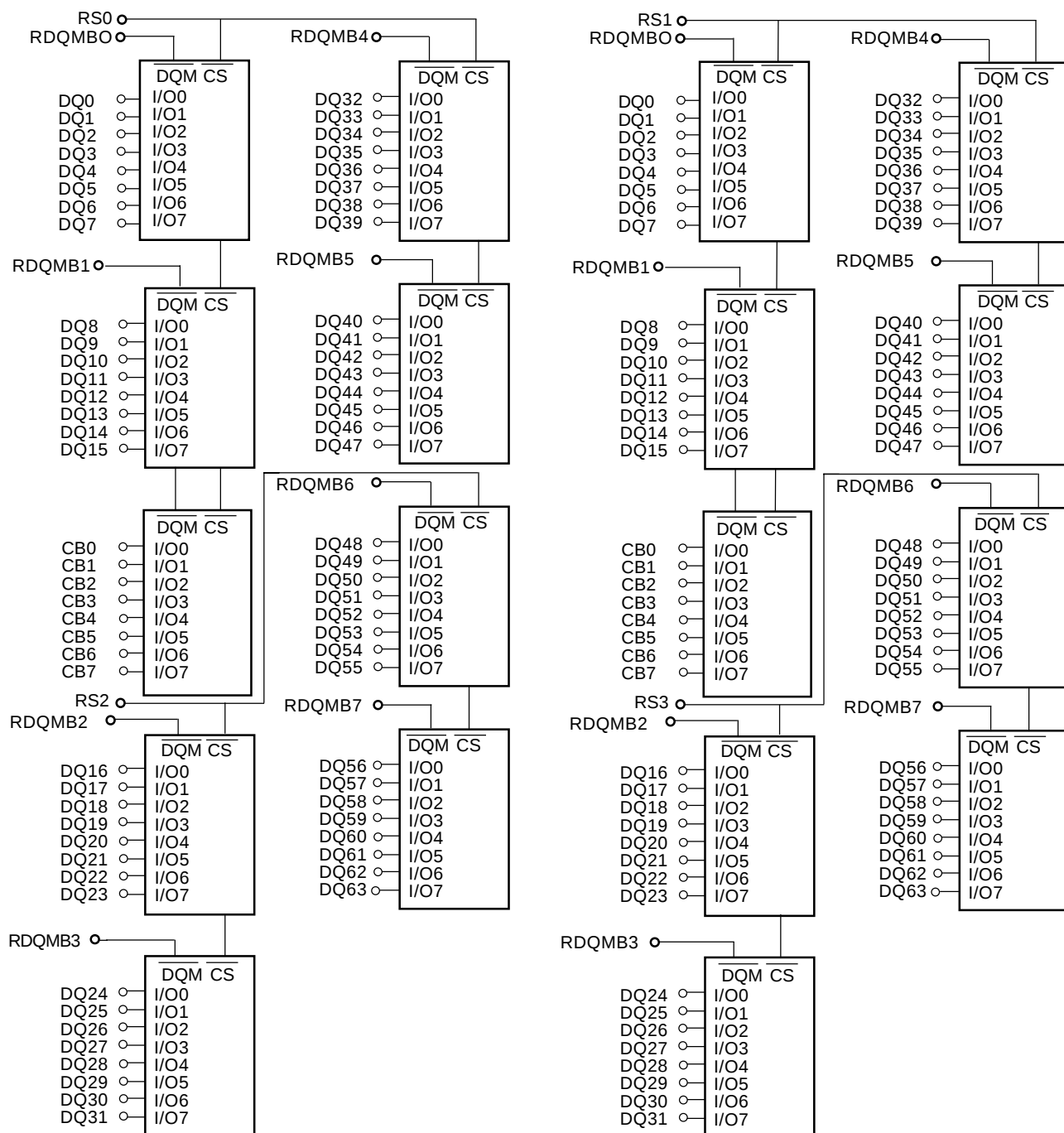


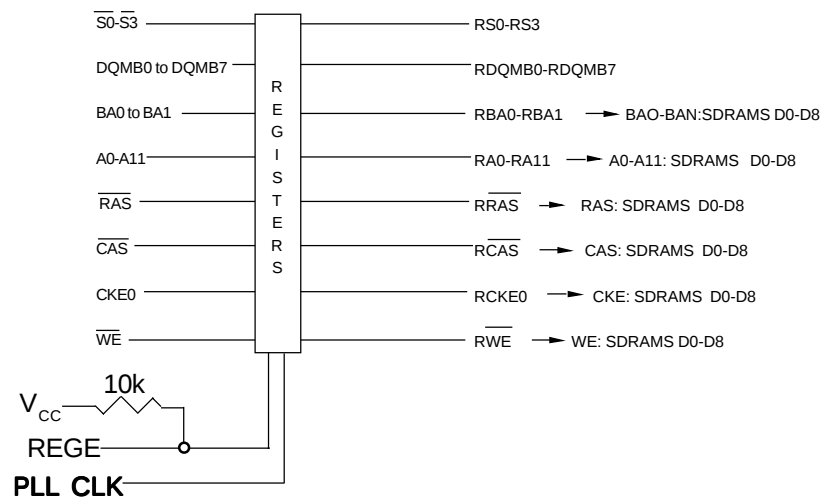
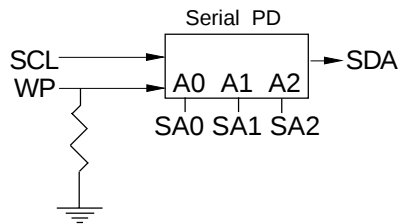
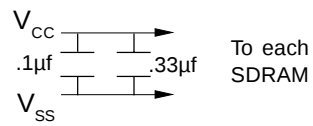
Notes

Tolerances on all dimensions except where otherwise indicated are ±.005 [.13].
The used device is 16Mx8 SDRAM, TSOP
All dimensions are expressed: inches [millimeters].

Side view







Absolute maximum ratings

	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 to +4.6	V
Storage temperature	T_{stg}	-55 to +150	°C
Power dissipation	P_D	27	W
Short-circuit output current	I_{OS}	50	mA

Note:

Permanent damage to the device may occur if absolute maximum ratings are exceeded. Operation should be restricted to the conditions detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC operating conditions and characteristics

(Voltage referenced to $V_{SS} = 0V$; $T_A = 0$ to $70^\circ C$)

	Symbol	Minimum	Typical	Maximum	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	$V_{DDQ} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	$I_{OH} = -2mA$
Output low voltage	V_{OL}	-	-	0.8	V	$I_{OL} = 2mA$
Input leakage current (Inputs)	I_{IL}	-3	-	3	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	3.0	uA	3.4

Notes:

(1) V_{IH} (max) = 5.6V AC. The overshoot voltage duration is $\leq 3ns$.

(2) V_{IL} (min) = -2.0V AC. The undershoot voltage duration is $\leq 3ns$.

(3) Any input $OV \leq V_{IN} \leq V_{DDQ}$

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

(4) Dout is disabled, $OV \leq V_{OUT} \leq V_{DDQ}$

Capacitance ($V_{DD} = 3.3V$, $T_A = 23^\circ C$, $f = 1MHz$, $V_{REF} = 1.4V \pm 200mV$)

	Symbol	Minimum	Maximum	Unit
Input capacitance (A0-A11)	C_{IN1}	-	15	pF
Input capacitance (RAS, CAS, WE)	C_{IN2}	-	15	pF
Input capacitance (CKE0)	C_{IN3}	-	15	pF
Input capacitance (CLK0)	C_{IN4}	-	35	pF
Input capacitance (CS0-CS3)	C_{IN5}	-	15	pF
Input capacitance (DQM0-DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0-BA1)	C_{IN7}	-	15	pF
Input/Output capacitance (DQ0-DQ63)	C_{OUT}	-	17	pF
Input/Output capacitance (CB0-CB7)	C_{OUT1}	-	17	pF

DC characteristics (Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C)

	Symbol	Test Condition	CAS	Max	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length=1 $t_{RC} \geq t_{RC}(\text{min})$ $I_{OL}=0 \text{ mA}$	-	1,560	mA	1
Precharge standby current in power-down mode	I_{CC2P}	$\text{CKE} \leq V_{IL}(\text{max}), t_{CC}=15\text{ns}$	-	22	mA	3
	I_{CC2PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max}), t_{CC}=15\text{ns} \infty$	-	22	mA	3
Precharge standby current in non power-down mode	I_{CC2N}	$\text{CKE} \geq V_{IH}(\text{min}), \overline{\text{CS}} \geq V_{IH}(\text{min}), t_{CC}=15\text{ns}$ Input signals are changed one time during 30ns	-	280	mA	3
	I_{CC2NS}	$\text{CKE} \geq V_{IH}(\text{min}), \text{CLK} \geq V_{IL}(\text{max}), t_{CC} = \infty$ Input signals are stable	-	130	mA	3
Active standby current in power-down mode	I_{CC3P}	$\text{CKE} \leq V_{IL}(\text{max}), t_{CC}=15\text{ns}$	-	90	mA	3
	I_{CC3PS}	$\text{CKE} \& \text{CLK} \leq V_{IL}(\text{max}), t_{CC}= \infty$	-	90	mA	3
Active standby current in non power-down mode	I_{CC3N}	$\text{CKE} \geq V_{IH}(\text{min}), \overline{\text{CS}} \geq V_{IH}(\text{min}), t_{CC}=15\text{ns}$ Input signals are changed one time during 30ns	-	550	mA	3
	I_{CC3NS}	$\text{CKE} \geq V_{IH}(\text{min}), \text{CLK} \geq V_{IL}(\text{max}), t_{CC} = \infty$ Input signals are stable	-	375	mA	3
Operating current (Burst mode)	I_{CC4}	$I_{OL}=0\text{mA}$ Page Burst 2 Blanks activated $t_{CCD}=2\text{CLK}$	3	1,600	mA	1
			2	1,600		
Refresh current	I_{CC5}	$t_{RC}=t_{RC}(\text{min})$	-	3,750	mA	2
Self refresh current	I_{CC6}	$\text{CKE} \leq 0.2\text{V}$	-	25	mA	3

Notes:

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs.

AC operating test conditions ($V_{DD}=3.3V \pm 0.3V$, $T_A=0$ to $70^{\circ}C$)

	Value	Unit
AC input levels (V_{ih}/V_{il})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f=1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 1	

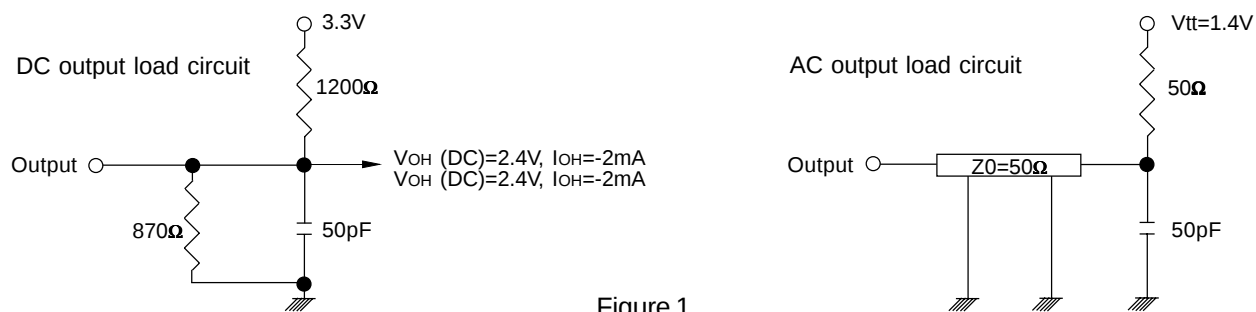


Figure 1

Operating AC parameter (AC operating conditions unless otherwise noted)

	Symbol	Time	Unit	Note
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
	$t_{RAS}(\max)$	100	ns	
Row cycle time	$t_{RC}(\min)$	70	ns	1
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to row precharge	$t_{RDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

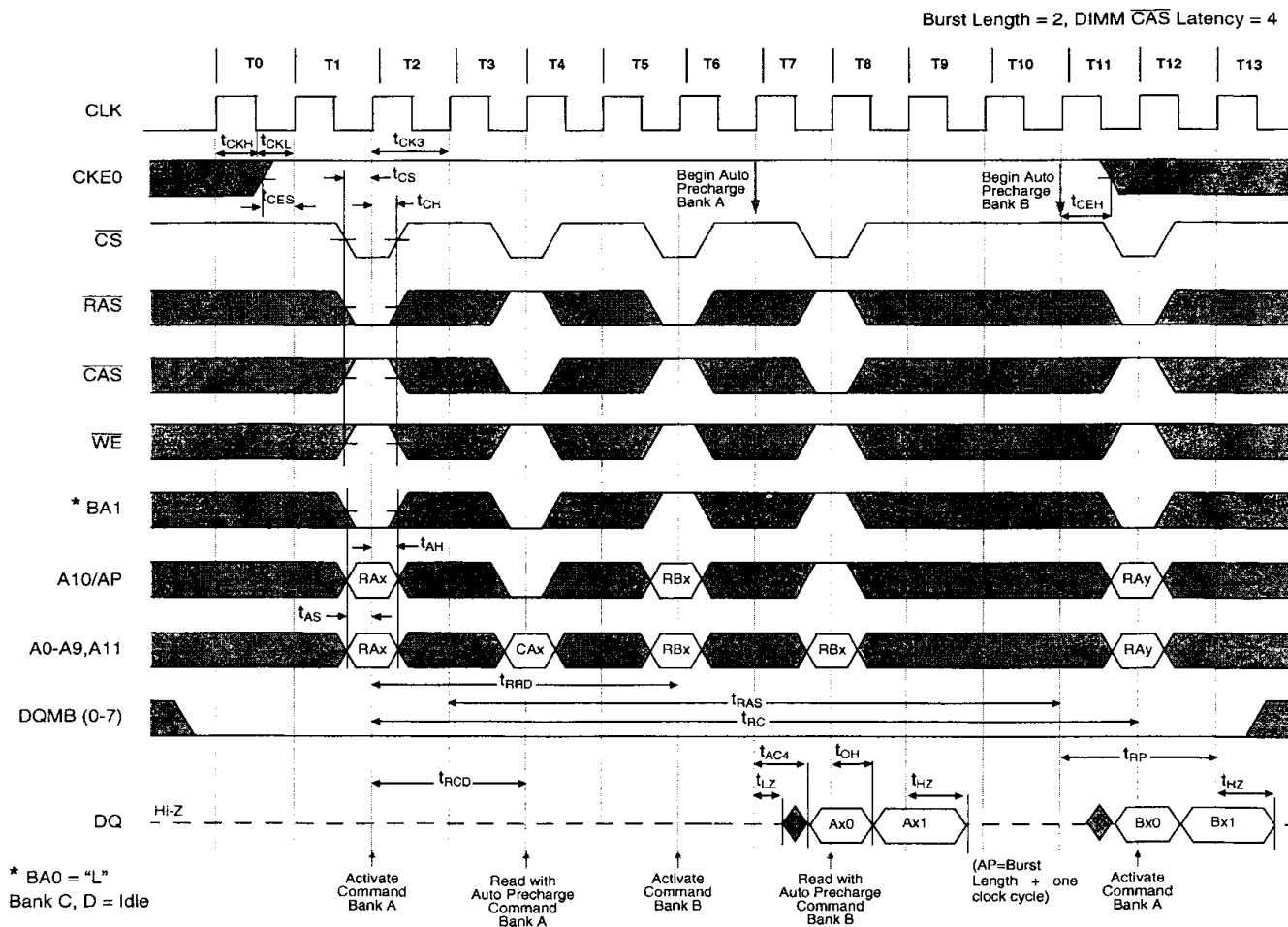
- Notes:**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
 2. Minimum delay is required to complete write in Reg. DIMM (1 CLK earlier than Unbuff. DIMM)
 3. All parts allow every cycle column address change.
 4. In case of row precharge interrupt, auto precharge and read burst stop.

AC characteristics (AC operating conditions unless otherwise noted)

	CAS	Symbol	Minimum	Maximum	Unit	Note
CLK cycle time	CAS latency=3	tCK	10	1000	ns	1
	CAS latency=2		10			
CLK to valid output delay	CAS latency=3	tAC		6	ns	1,2
	CAS latency=2			6		
Output data hold time	CAS latency=3	t _{OH}	3		ns	1,2
	CAS latency=2		3			
CLK high pulse width		tCKH	3		ns	3
CLK low pulse width		tCKL	3		ns	3
Input setup time		tDS	2		ns	3
Input hold time		tDH	1		ns	3
CLK to output in Low-Z		tLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tHZ		6	ns	1
	CAS latency=2			6		

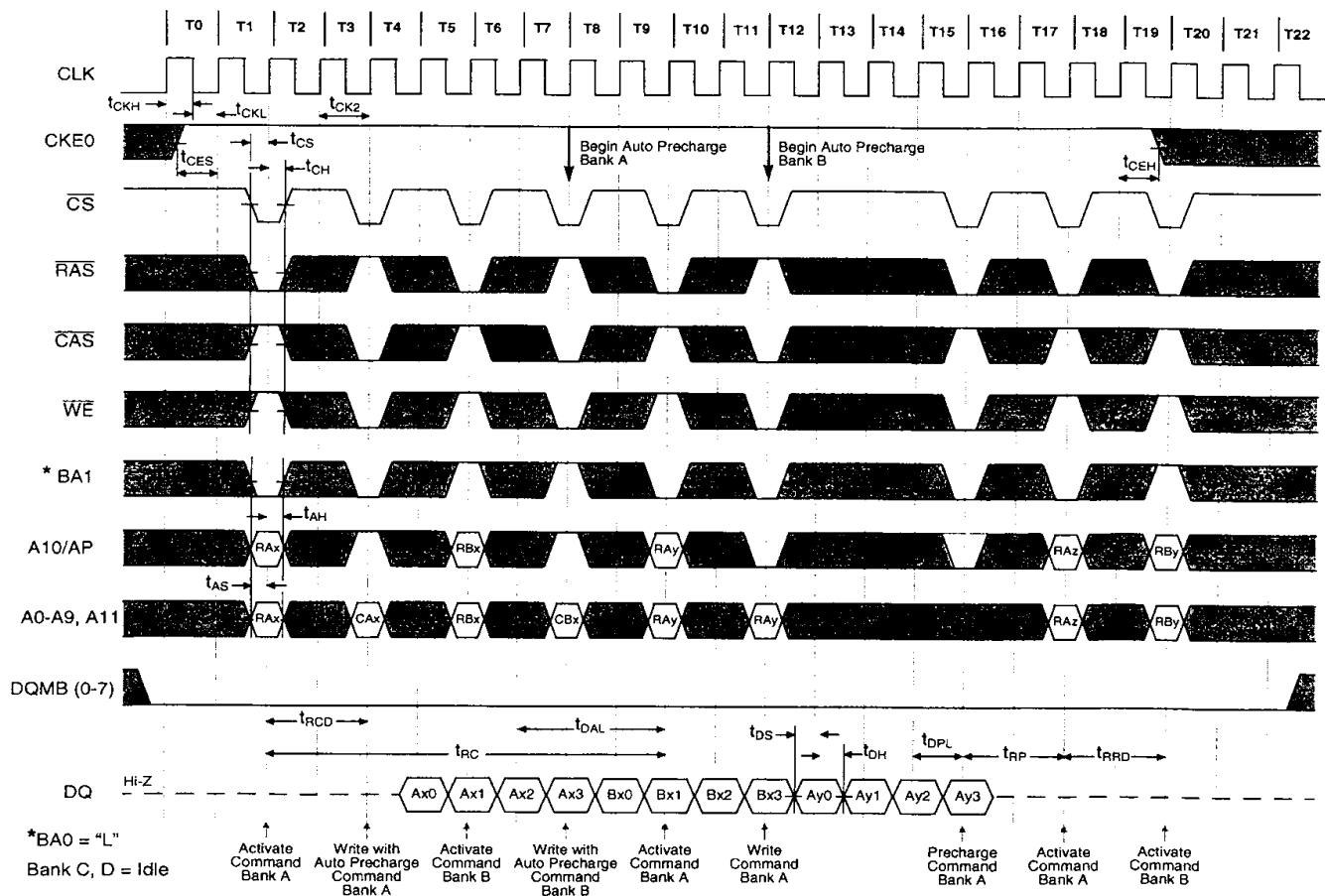
- Notes:**
- Parameters depend on programmed CAS latency.
 - If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
 - Assumed input rise and fall time (tr & tf)=1ns.
- If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1] ns should be added to the parameter.

AC Parameters for Read Timing



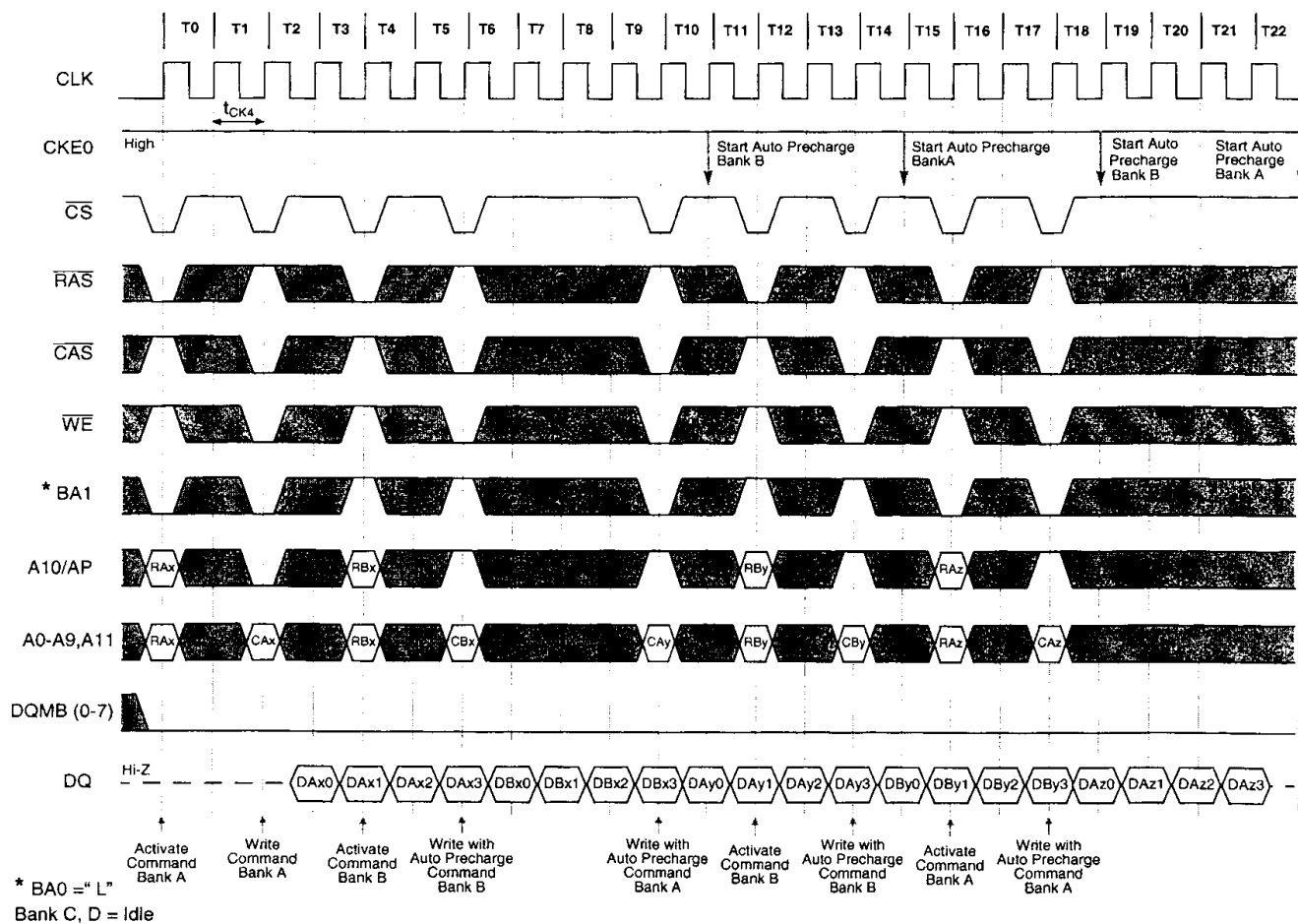
AC Parameters for Write Timing

Burst Length = 4, $\overline{\text{CAS}}$ Latency = 2

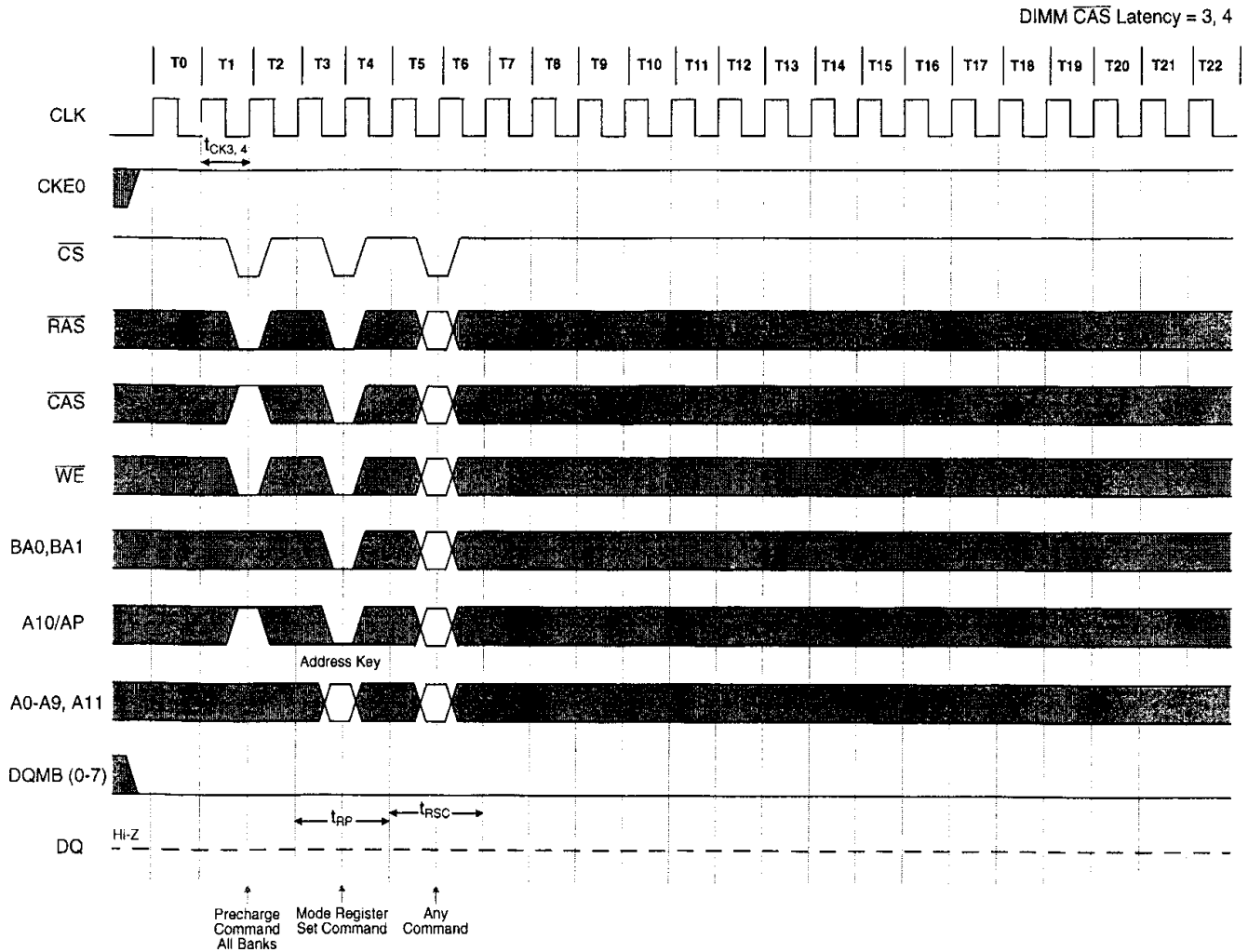


Auto Precharge After Write Burst

Burst Length = 4, DIMM $\overline{\text{CAS}}$ Latency = 4

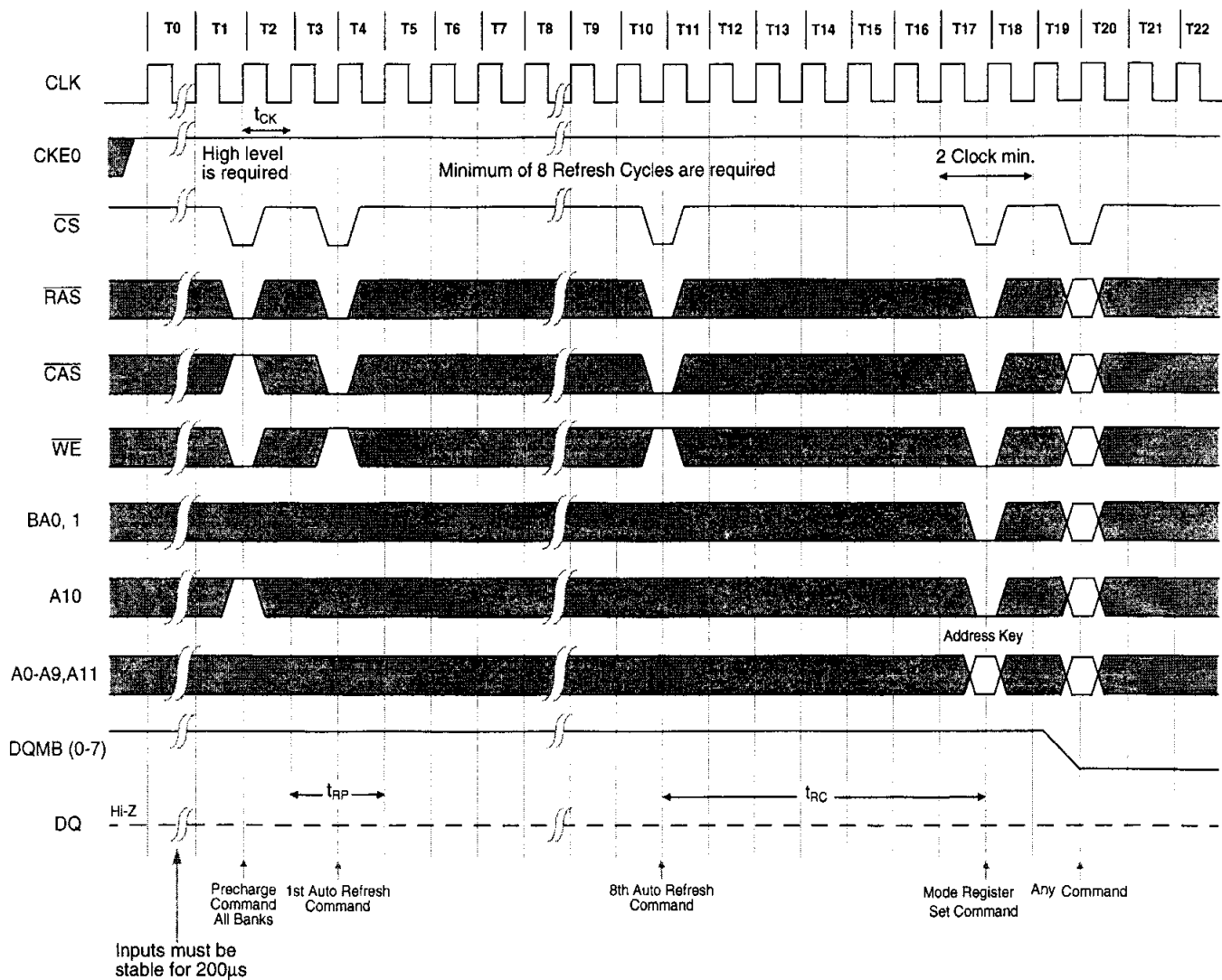


Mode Register Set



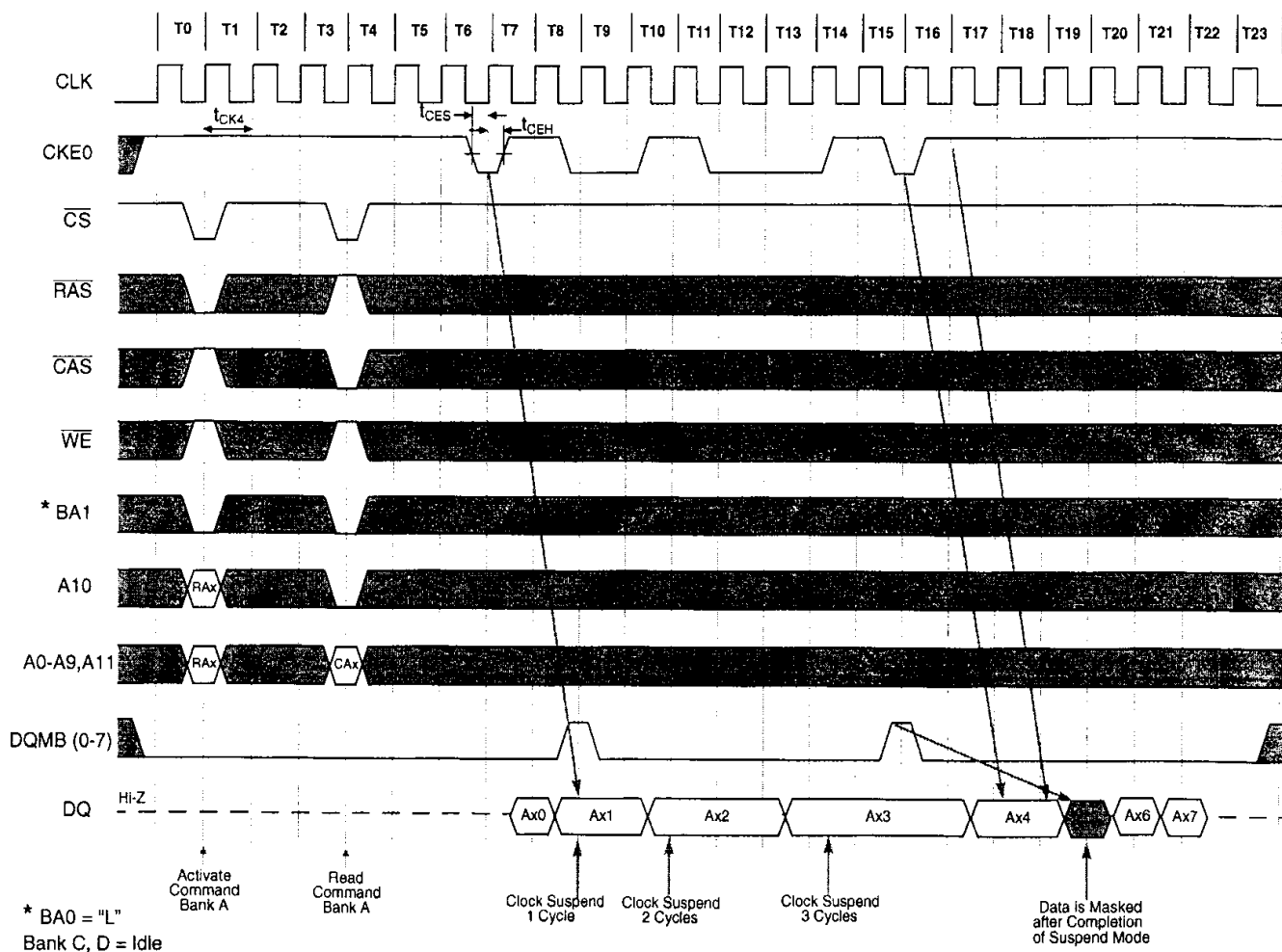
Power on Sequence and Auto Refresh (CBR)

DIMM $\overline{\text{CAS}}$ Latency = 4

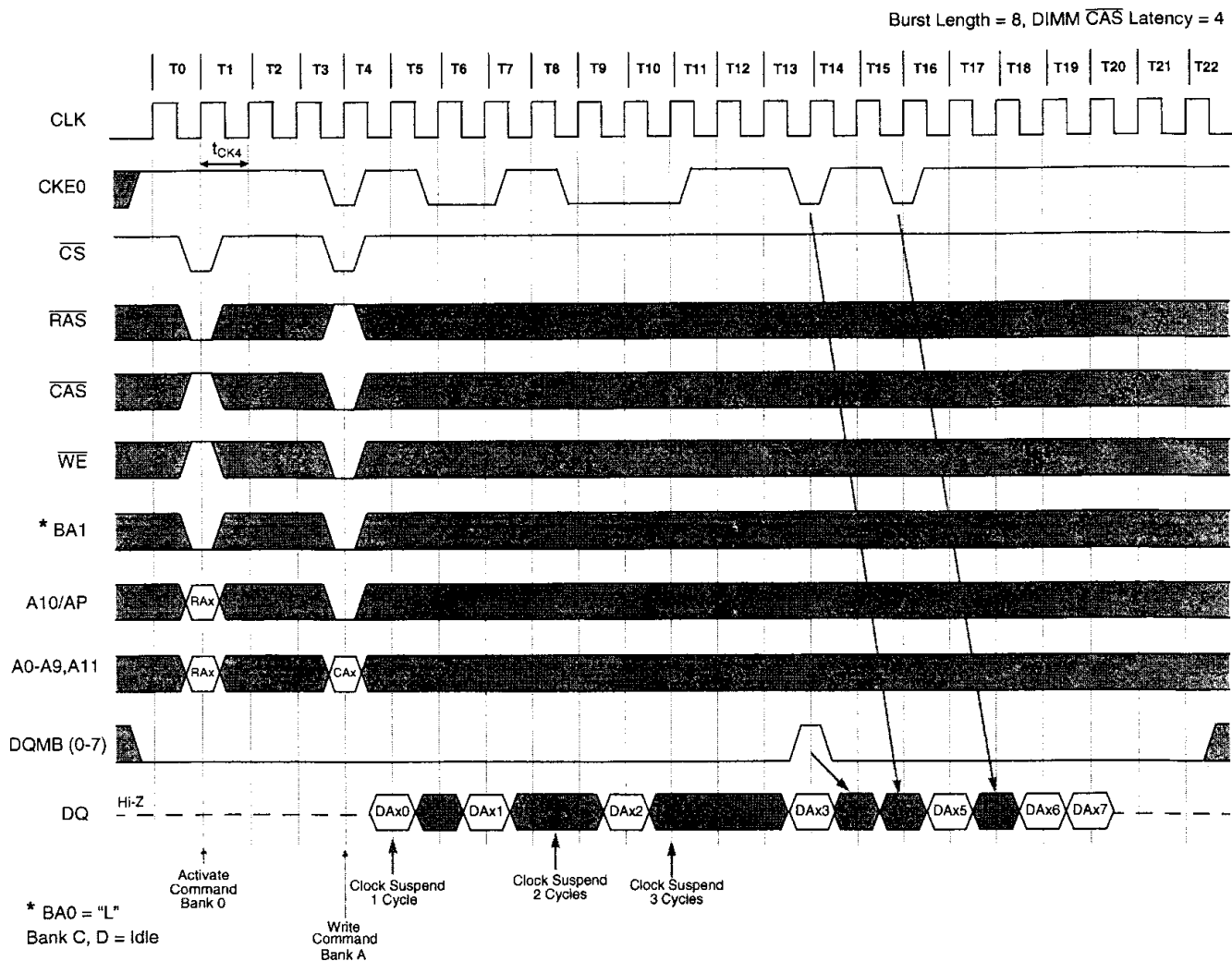


Clock Suspension / DQMB During Burst Read

Burst Length = 8, DIMM CAS Latency = 4

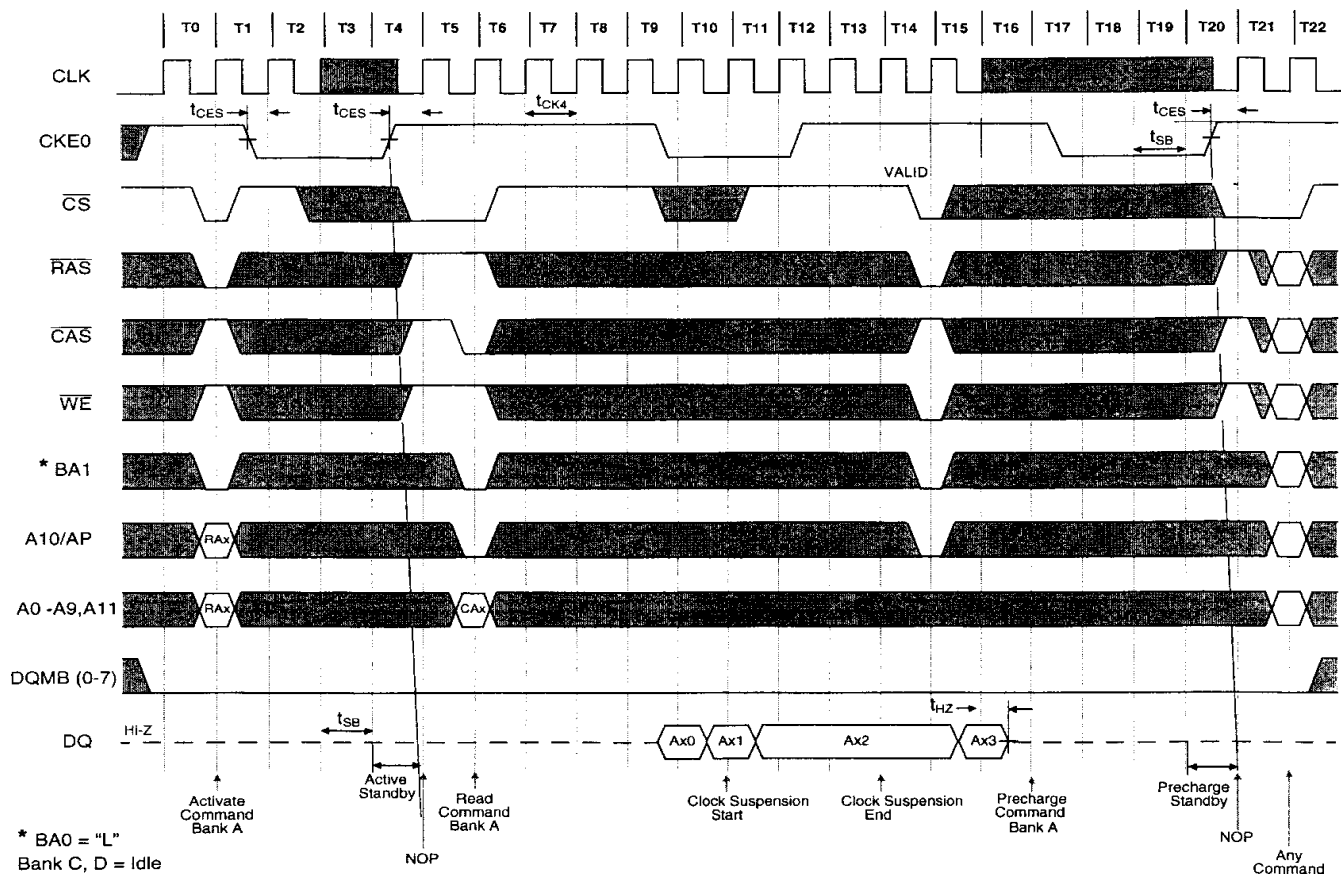


Clock Suspension / DQMB During Burst Write

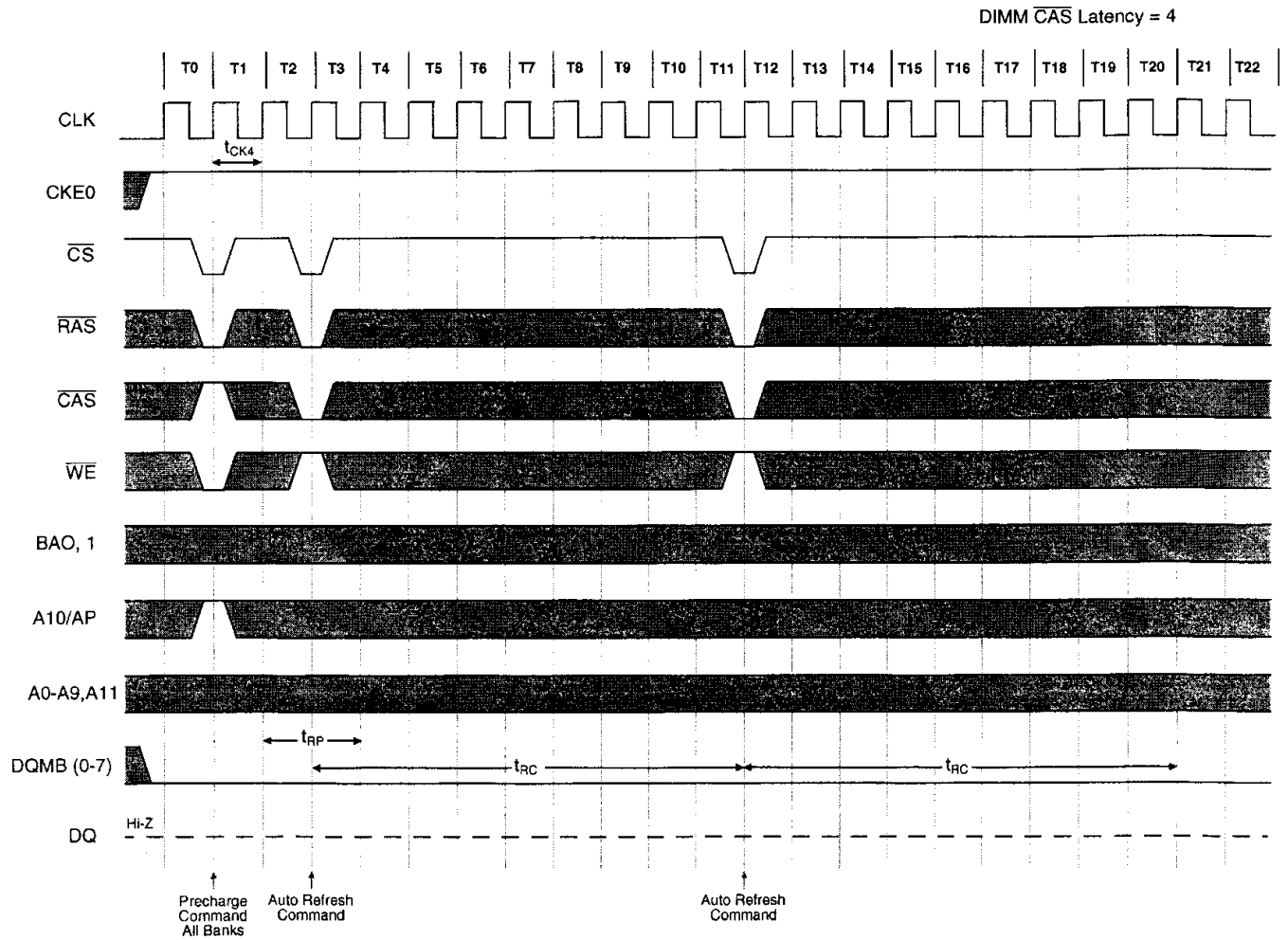


Power Down Mode and Clock Suspend

Burst Length = 4, DIMM $\overline{\text{CAS}}$ Latency = 4

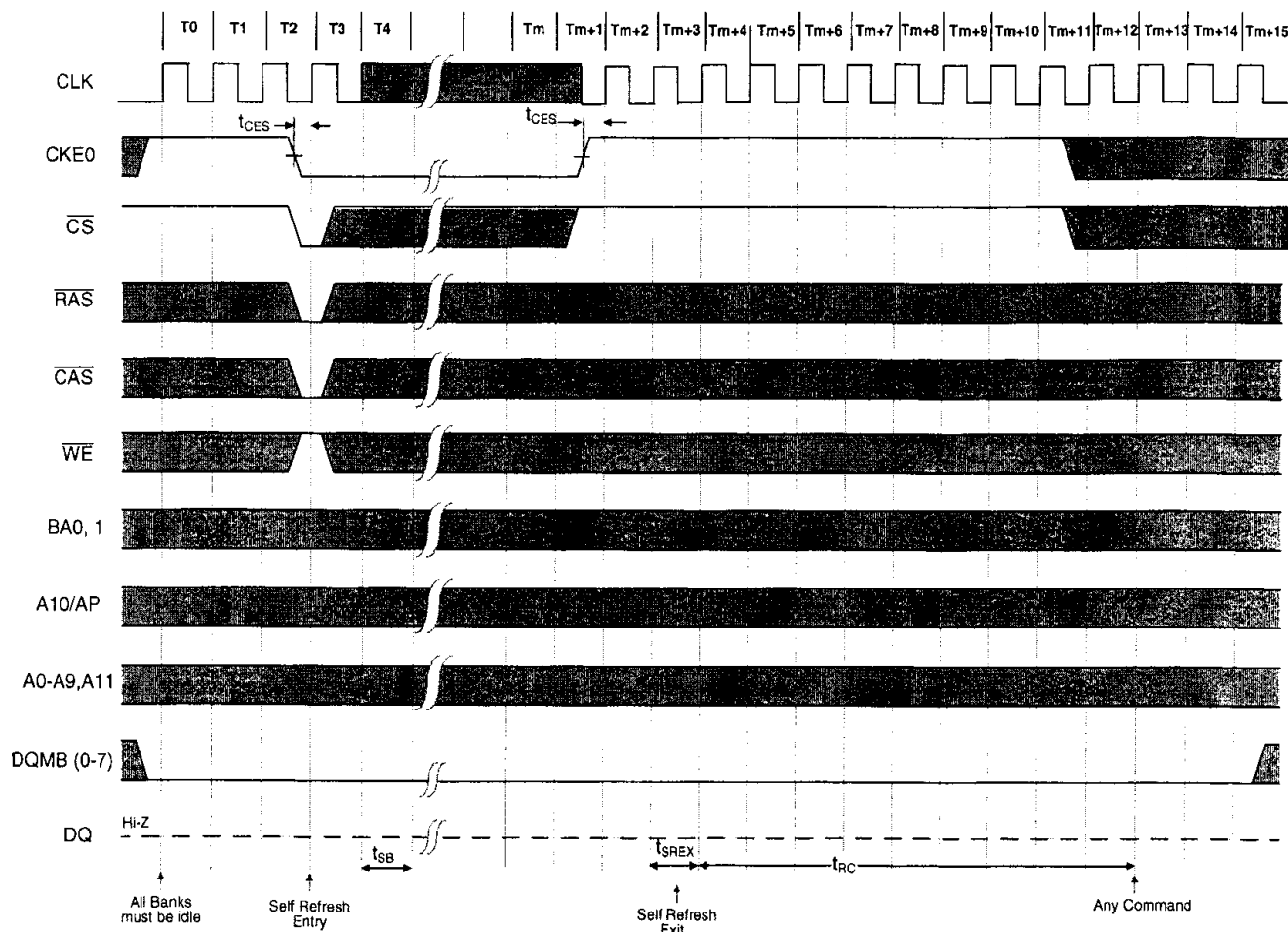


Auto Refresh (CBR)



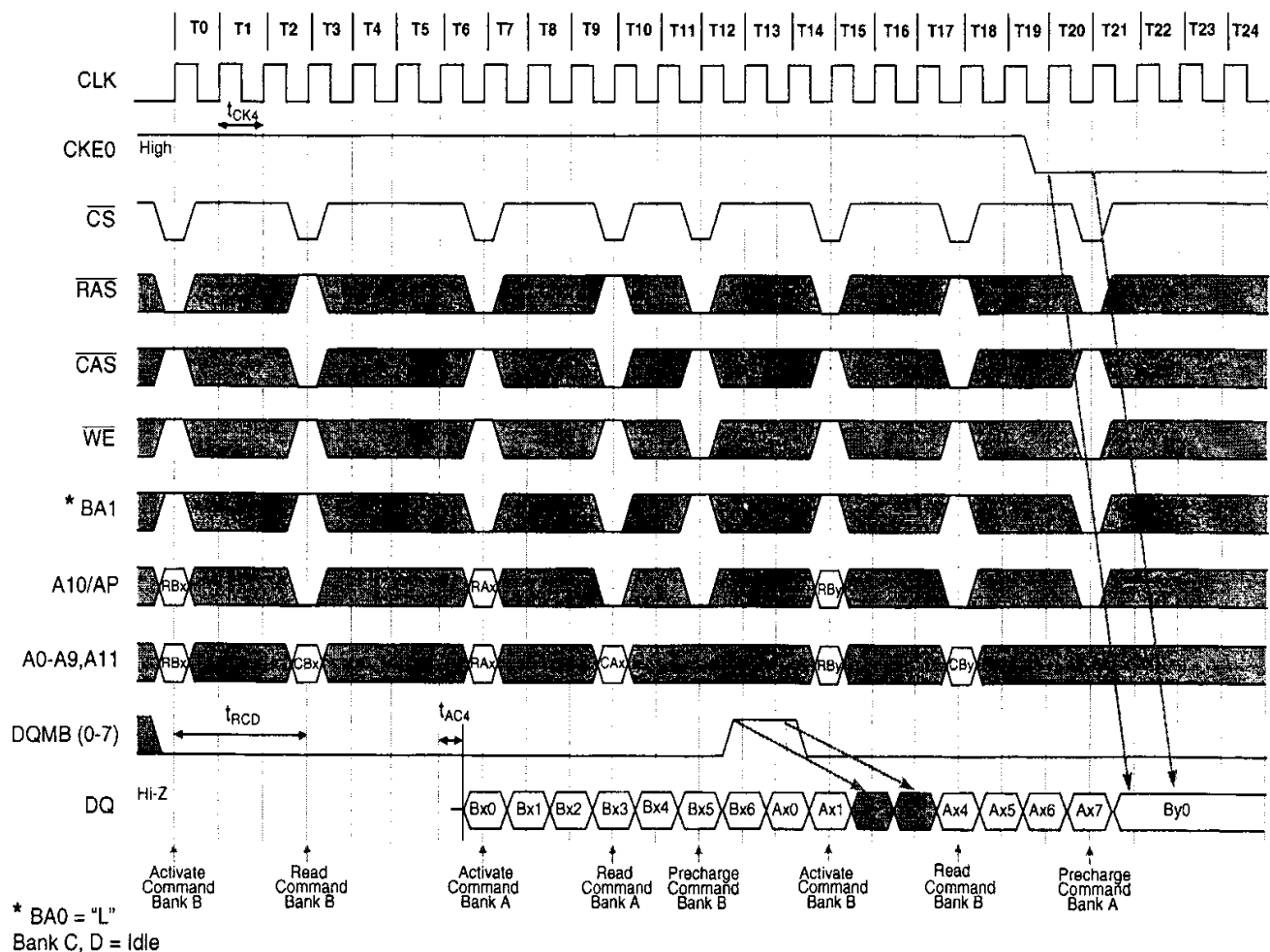
Self Refresh (Entry and Exit)

Note: The CK0 signal must be reestablished prior to DKE0 returning high.

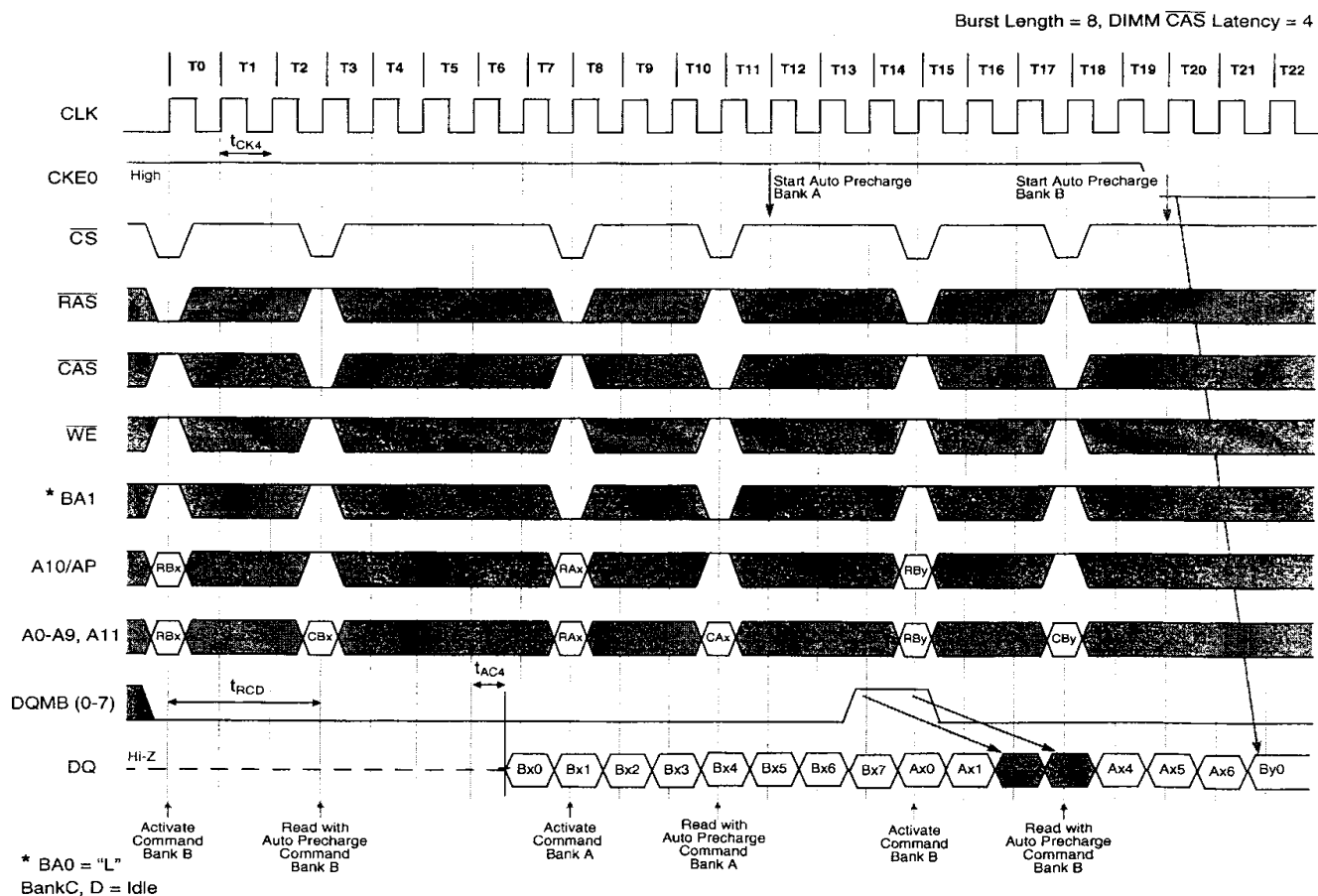


Random Row Read (Interleaving Banks) with Precharge

Burst Length = 8, DIMM $\overline{\text{CAS}}$ Latency = 4

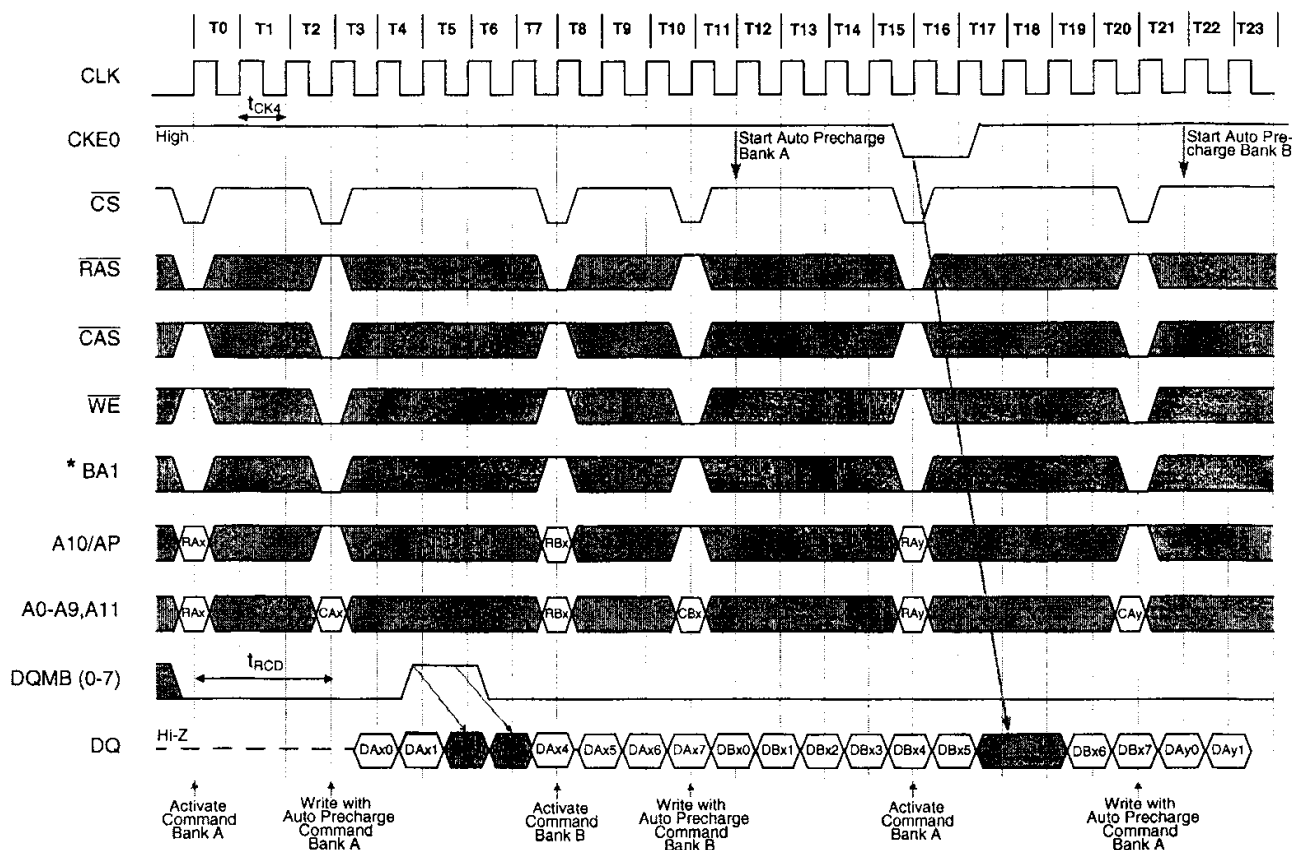


Random Row Read (Interleaving Banks) with Auto-Precharge



Random Row Write (Interleaving Banks) with Auto-Precharge

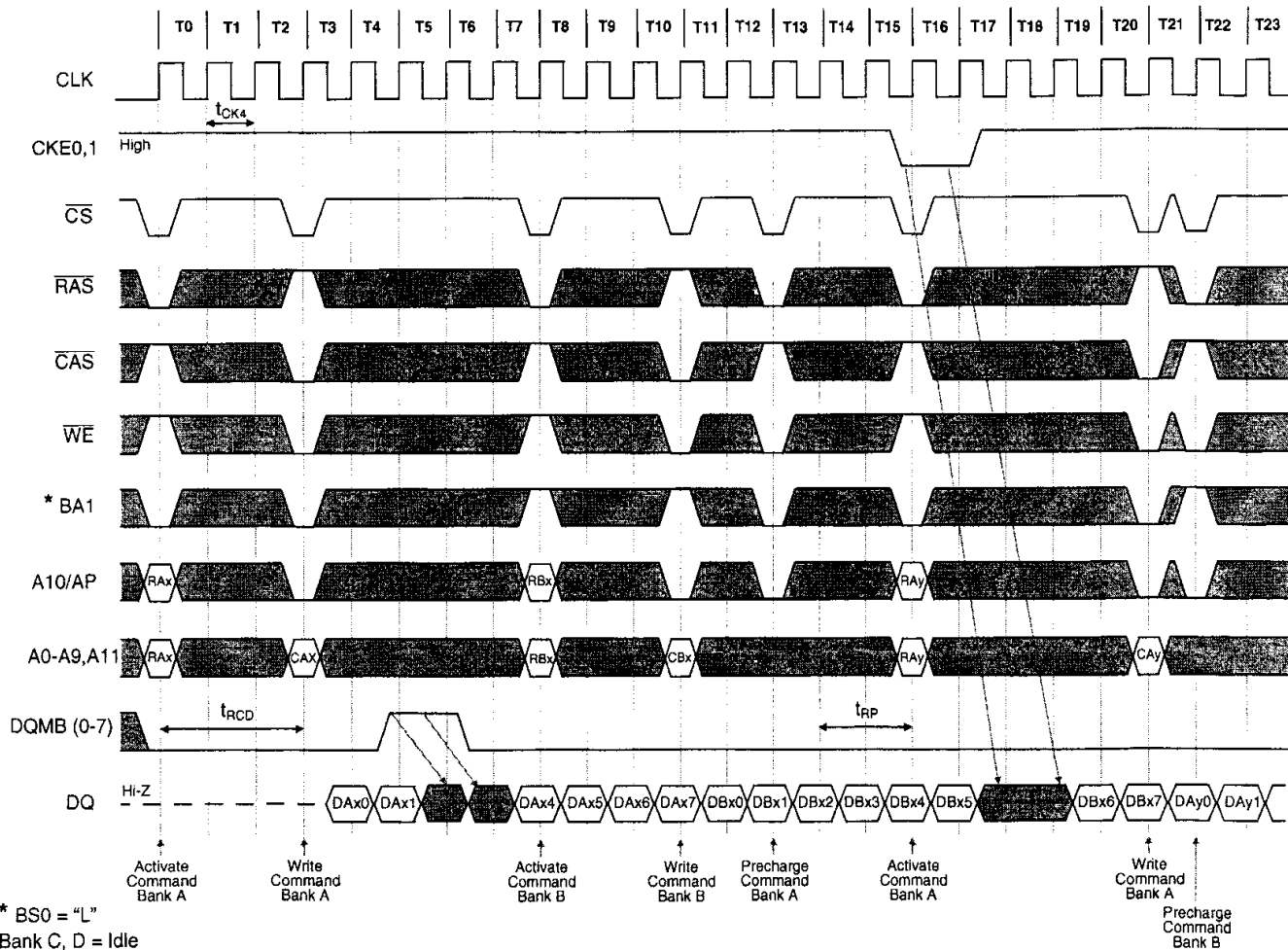
Burst Length = 8, DIMM CAS Latency = 4



* BA0 = "L"
Bank C, D = Idle

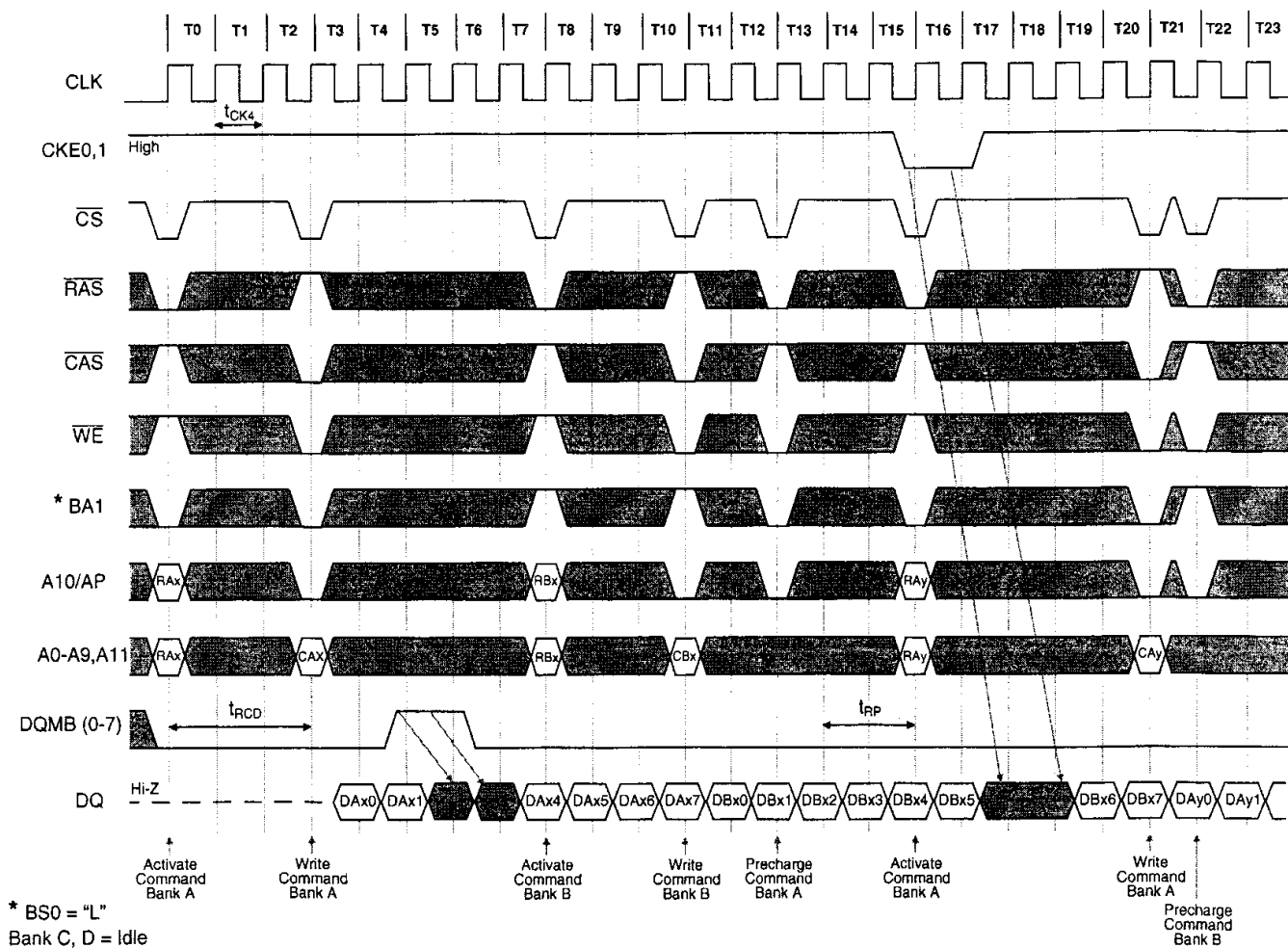
Random Row Write (Interleaving Banks) with Precharge

Burst Length = 8, DIMM $\overline{\text{CAS}}$ Latency = 4

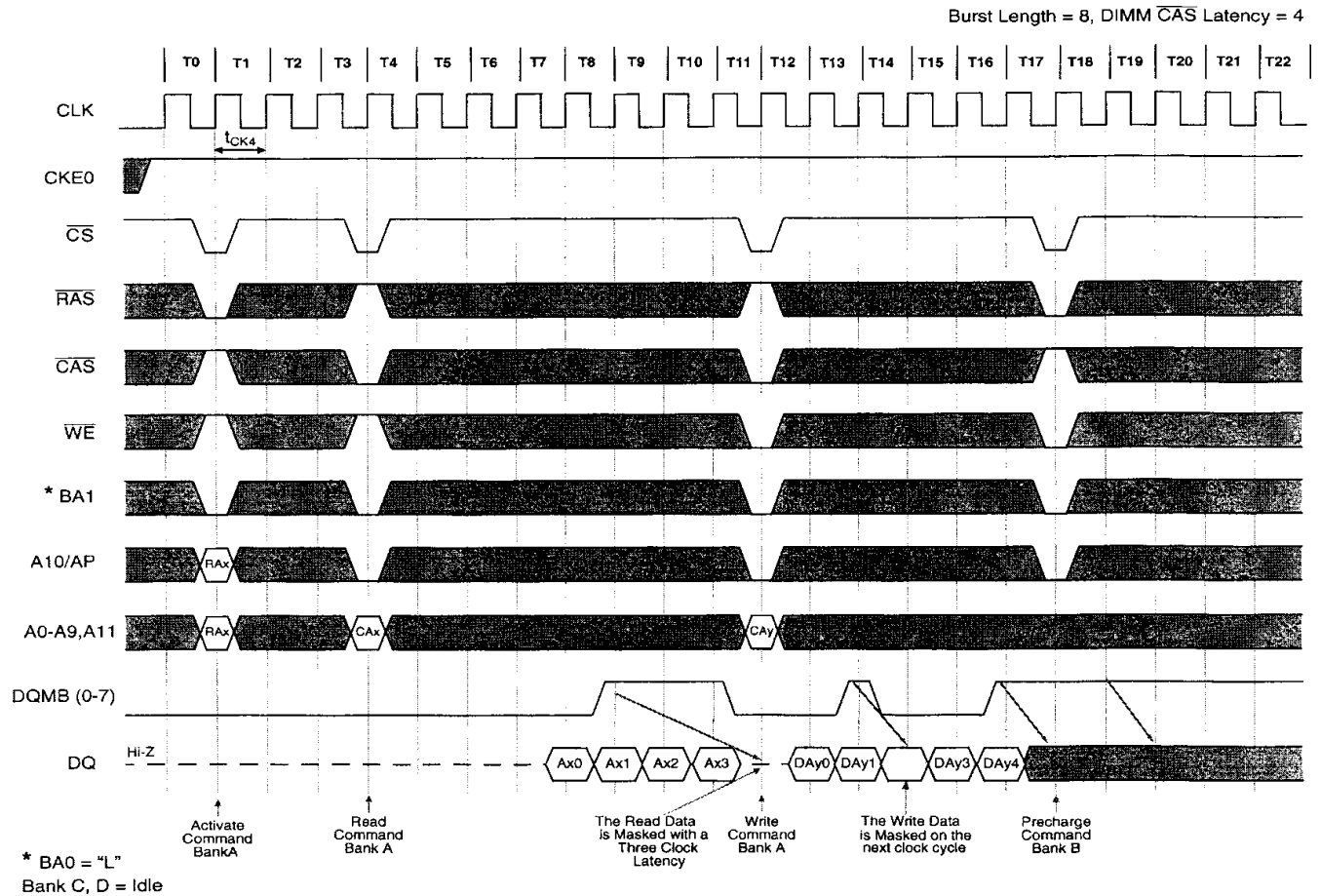


Random Row Write (Interleaving Banks) with Precharge

Burst Length = 8, DIMM $\overline{\text{CAS}}$ Latency = 4

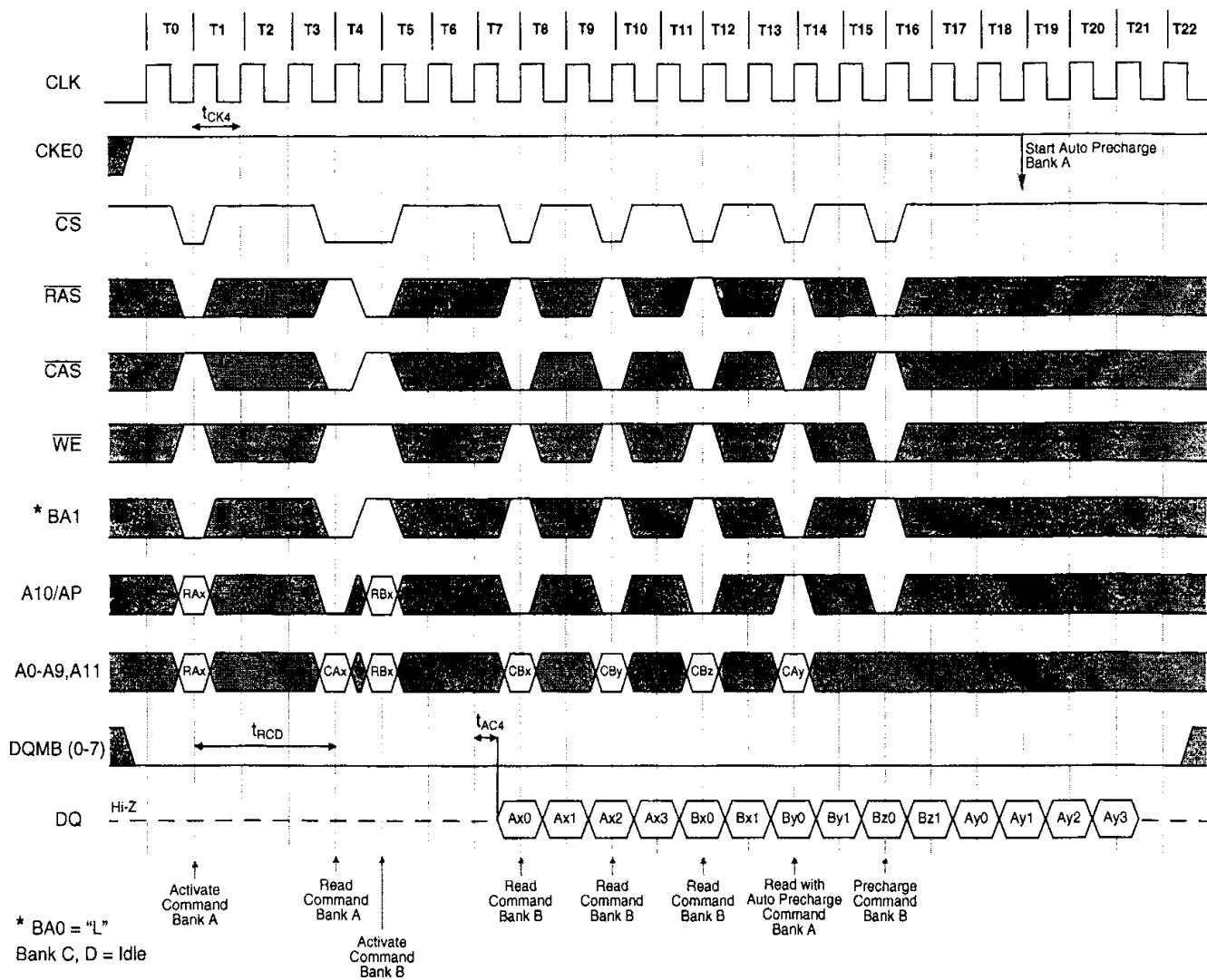


Read / Write Cycle



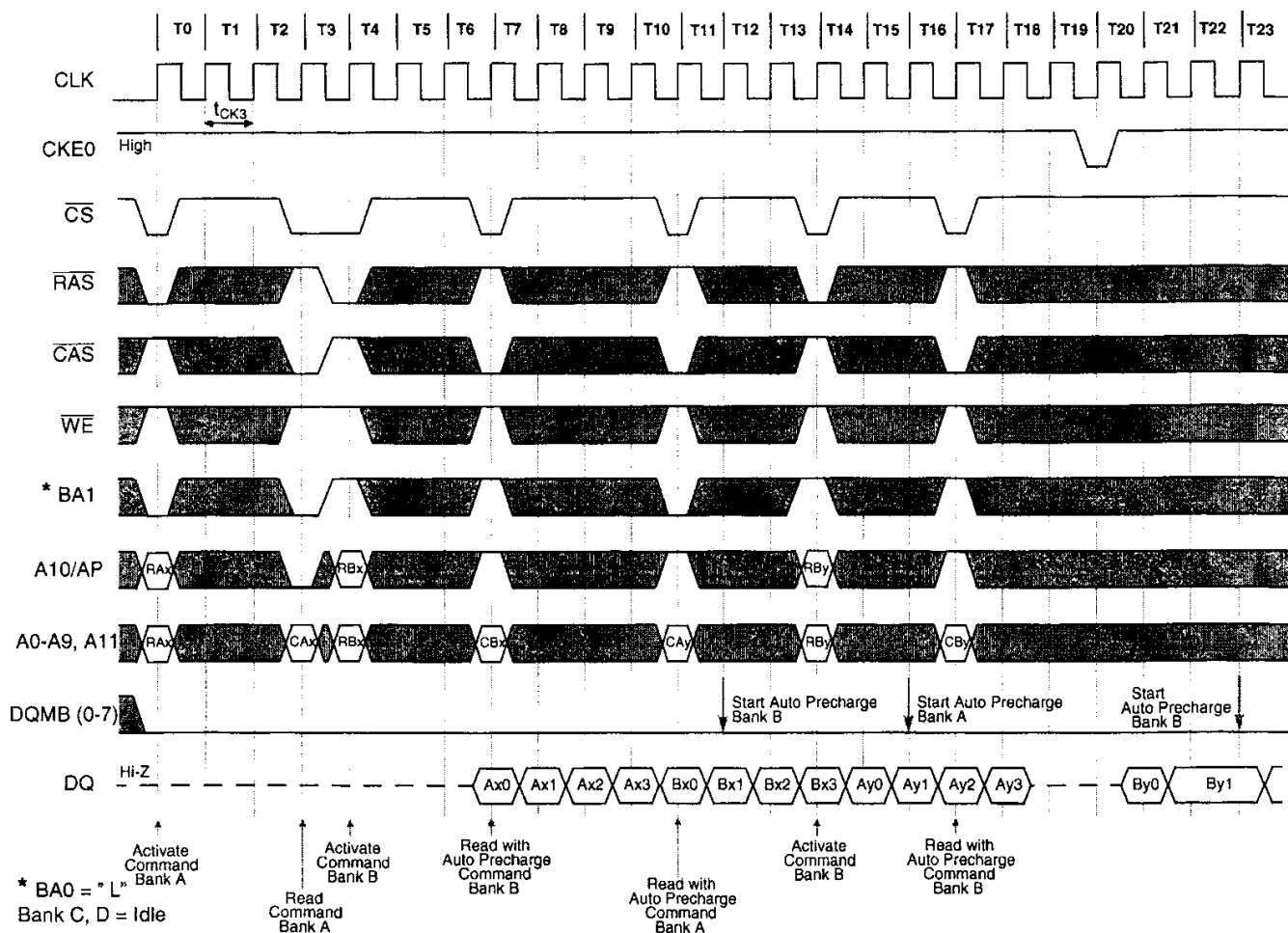
Interleaved Column Read Cycle

Burst Length = 4, DIMM $\overline{\text{CAS}}$ Latency = 4



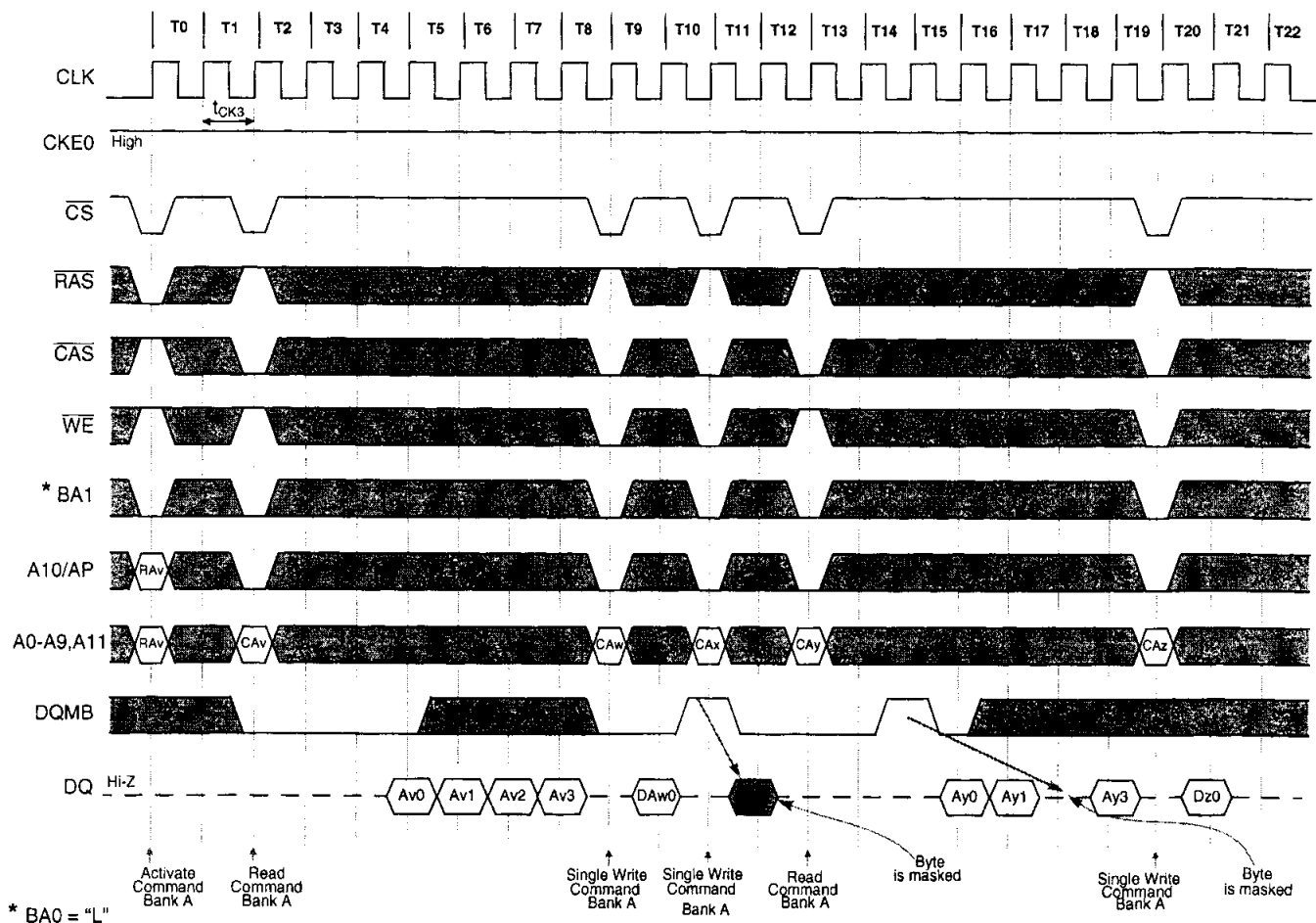
Auto Precharge After Read Burst

Burst Length = 4, DIMM $\overline{\text{CAS}}$ Latency = 4



Burst Read and Single Write Operation‡

Burst Length = 4, DIMM $\overline{\text{CAS}}$ Latency = 3



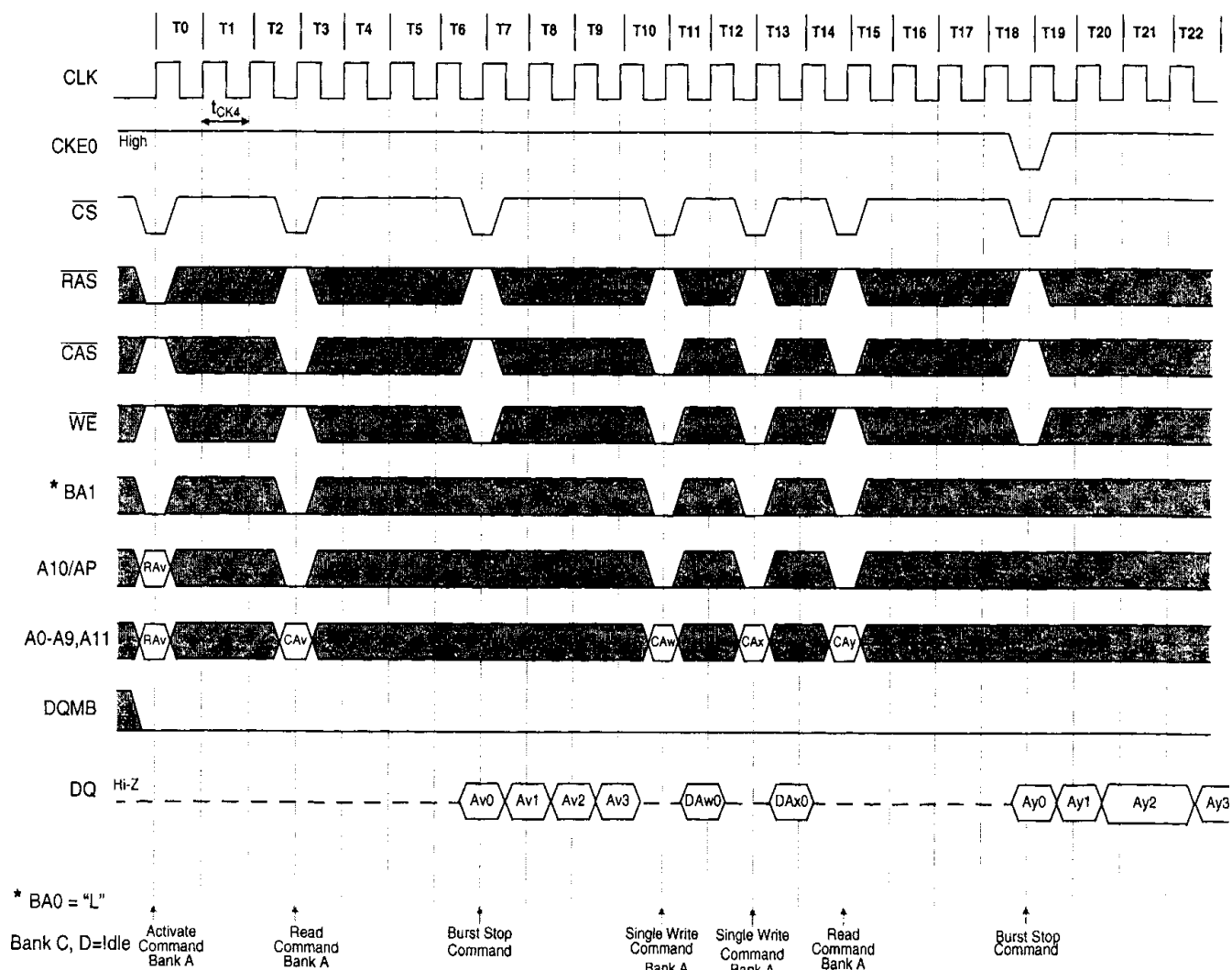
* BA0 = "L"

Bank C, D = Idle

‡ Note that the Single Write Operation is possible through programming of the Mode Register.

Full Page Burst Read and Single Write Operation‡

Burst Length = Full Page, DIMM $\overline{\text{CAS}}$ Latency = 4



‡ Note that Single Write Operation is possible through programming of the Mode Register.