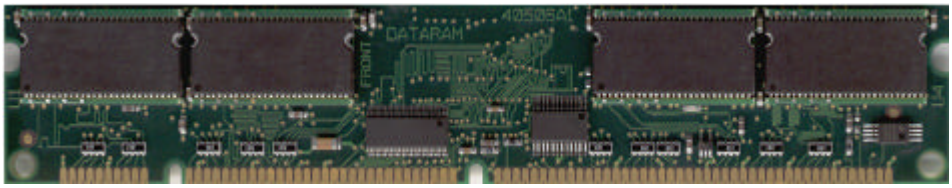
DTM60188

256MB-32Mx72, 168-Pin Registered PC133 SDRAM DIMM



Identification

32Mx72 PC133

Performance Range

133MHz (7.5ns@ CL=3)

Features

- Burst mode operation
- Auto and self refresh capability (4096 Cycles/64 ms)
- LVTTL compatible inputs and outputs
- Single 3.3V?0.3V power supply
- MRS cycle with address key programs Latency (Access from column address), Burst length (1, 2, 4 and 8), Data scramble (Sequential and Interleave)
- Serial presence detect with EEPROM
- 168-pin PC133 DIMM assembly 5.250” wide by 1.00” high

Description

The Dataram DTM60188 Assembly is a 32M bit x 72 Synchronous Dynamic RAM high-density memory module. The DTM60188 consists of nine stacked 32M x 8 bit Synchronous DRAMs in a TSOP-II 400MII package, two 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock, and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect. The assembly is in a standard 168-pin wide form factor, but is only one inch high—ideal for inclusion into low profile applications such as 1U servers. The memory module is configured as one physical bank of DRAMs, and each DRAM is comprised of four internal banks of memory locations. Each specific memory location is further addressed by 12 row lines (A0-A11), and 11 column lines (A0-9, A11).

Pin Configurations

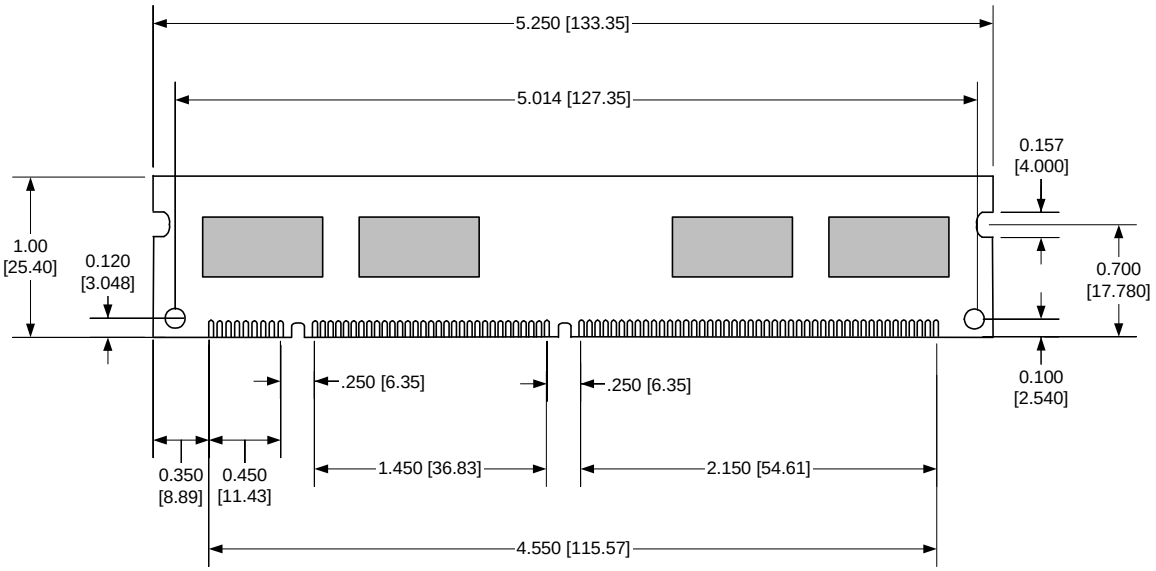
Front side						Back side					
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	*$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	$\overline{RAS}$	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*Vref	90	Vdd	118	A3	146	*Vref
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vdd	101	DQ45	129	$\overline{S3}$	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	**WP	109	NC	137	CB7	165	**SA0
26	Vdd	54	Vss	82	**SDA	110	Vdd	138	Vss	166	**SA1
27	$\overline{WE}$	55	DQ16	83	**SCL	111	$\overline{CAS}$	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

Pin Names

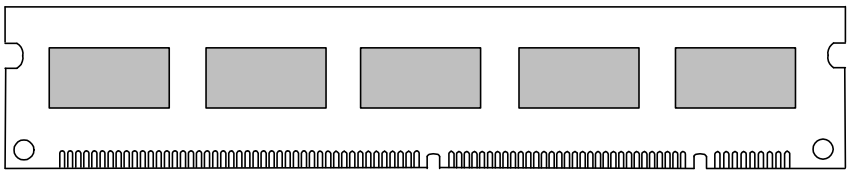
Pin name	Function
A0-A13	Address input (Multiplexed)
BA0-BA1	Select bank
DQ0-DQ63	Data input/output
CB0-CB7	Check bit (Data-in/data-out)
CK0-3	Clock input
CKE0	Clock enable input
$\overline{S0}$-$\overline{S3}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DQM0-7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
*Vref	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0-2	Address in EEPROM
DU	Don’t use
NC	No connection
WP	Write protection

*These pins are not used in this module.
**These pins should be NC in the system, which does not support SPD.

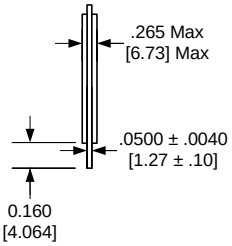
Front View

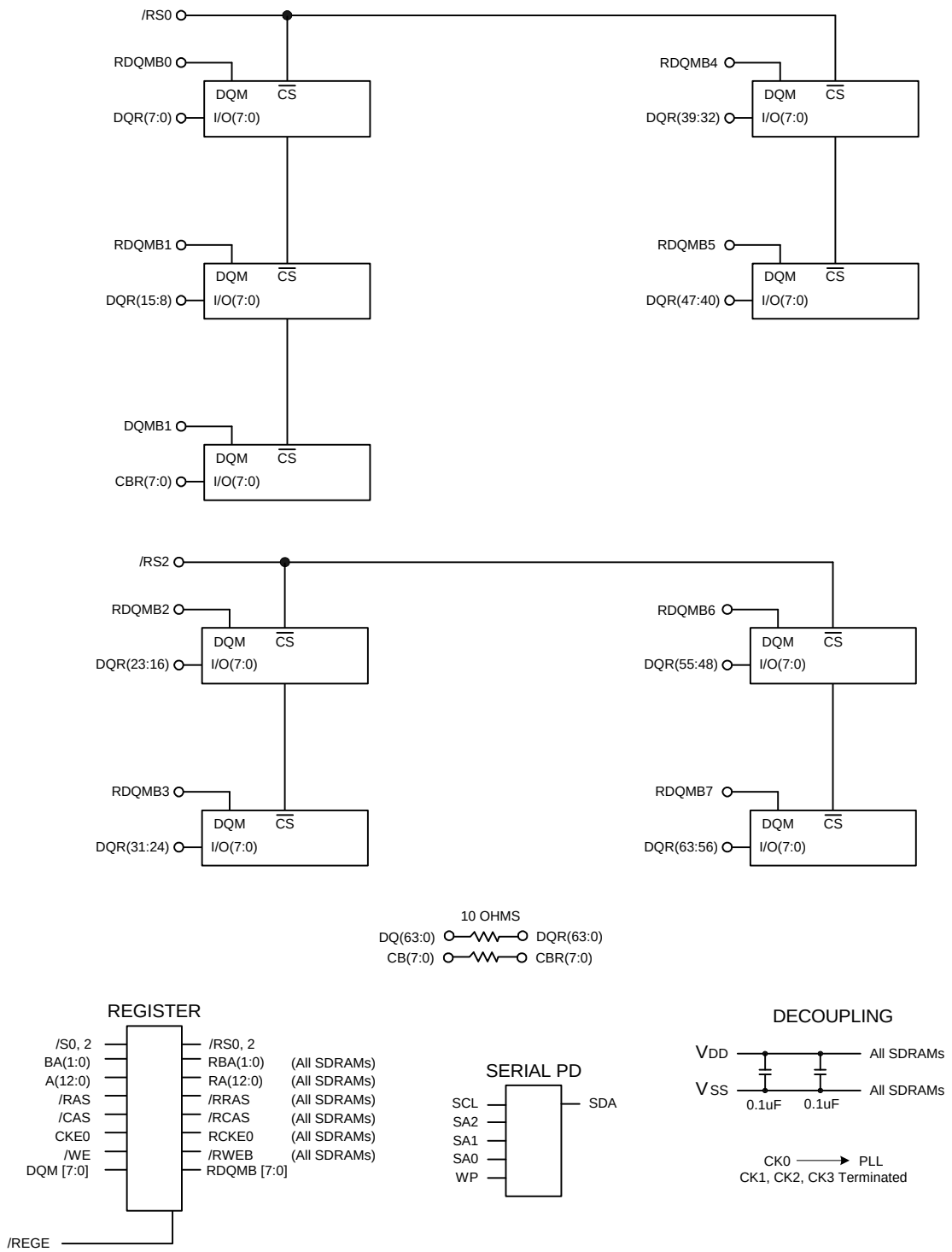


Back View



Side View




/RS0
RDQMB0
DQR(7:0)
DQM
CS
I/O(7:0)
RDQMB4
DQR(39:32)
RDQMB1
DQR(15:8)
RDQMB5
DQR(47:40)
DQMB1
CBR(7:0)
/RS2
RDQMB2
DQR(23:16)
RDQMB6
DQR(55:48)
RDQMB3
DQR(31:24)
RDQMB7
DQR(63:56)
10 OHMS
DQ(63:0)
DQR(63:0)
CB(7:0)
CBR(7:0)
REGISTER
/S0, 2
BA(1:0)
A(12:0)
/RAS
/CAS
CKE0
/WE
DQM [7:0]
/RS0, 2
RBA(1:0)
RA(12:0)
/RRAS
/RCAS
RCKE0
/RWEB
RDQMB [7:0]
(All SDRAMs)
/REGE
SERIAL PD
SCL
SA2
SA1
SA0
WP
SDA
DECOUPLING
VDD
VSS
All SDRAMs
0.1uF
0.1uF
CK0
PLL
CK1, CK2, CK3 Terminated

Absolute Maximum Ratings

	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3 to V_{DD}+0.3	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	-55 to +150	?C
Power dissipation	P_D	5	W
Short-circuit output current	I_{OS}	50	MA

NOTE:

Permanent damage to the device may occur if absolute maximum ratings are exceeded. Operation should be restricted to the conditions detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect relaibility.

DC Operating Conditions and Characteristics (Voltage referenced to V_{SS} = OV; T_A = 0 to 70?C)

	Symbol	Minimum	Typical	Maximum	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-9	-	9	uA	3
Input leakage current (I/O pins)	I_{IL}	-1.5	-	1.5	uA	3,4

NOTES:

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ? 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ? 3ns.
3. Any input OV ? V_{IN} ? V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, OV ? V_{OUT} ? V_{DDQ}.

Capacitance (V_{DD} = 3.3V, T_A = 23?C, f = 1MHz, V_{REF} = 1.4V ± 200mV)

	Symbol	Maximum (x72)	Unit
Address (A0-A11, BA0-BA1)	C_{ADD}	19	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN}	19	pF
CKE (CKE0)	C_{CKE}	19	pF
Clock (CK0)	C_{CLK}	20.5	pF
CS ($\overline{S0}$, $\overline{S2}$)	C_{CS}	12	pF
DQM (DQM0-DQM7)	C_{DQM}	8	pF
DQ (DQ0-DQ63)	C_{OUT1}	6	pF
CB (CB0-CB7)	C_{OUT2}	6	pF

DC Characteristics (Recommended operating condition unless otherwise noted, T_A = 0 to 70?C)

	Symbol	Test Condition	Maximum	Unit	Notes
Operating current (Active mode)	I_{DD1}	Burst length = 2 t_{RC} = t_{RC}(min) I_{OL} = 0 mA	2,980	mA	1, 3
Precharge standby current in power-down mode	$I_{DD2}P$	CKE ? V_{IL} (max), t_{CC}=15ns	37	mA	3
Precharge standby current in non power-down mode	$I_{DD2}N$	CKE ? V_{IH} (min), CS ? V_{IH} (min), t_{CC}=15ns Input signals are changed one time during 30ns	730		3
Active standby current in power-down mode	$I_{DD3}P$	CKE ? V_{IL} (max), t_{CC}=15ns	185	mA	
Active standby current in non power-down mode	$I_{DD3}N$	CKE ? V_{IH} (min), CS ? V_{IH} (min), t_{CC}=15ns Input signals are changed one time during 30ns	905	mA	3
Operating current (Burst mode)	I_{DD4}	IOL=0mA Page Burst 2 Blanks activated t_{CCD}=2CLK	1,850	mA	1, 3
Refresh current	I_{DD5}	t_{RC} = t_{RC} (min)	4,140	mA	2, 3
Self Refresh current	I_{DD6}	CKE ? 0.2V	27	mA	3

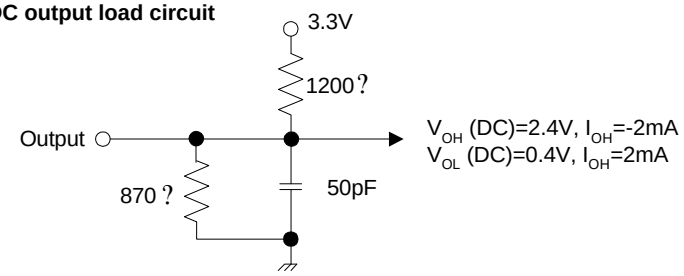
NOTES:

1. Measured with outputs open
2. Refresh period is 64ms
3. Maximum

AC Operating Test Conditions (V_{DD} = 3.3V ? 0.3V, T_A = 0 to 70?C)

	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Figure 1	

DC output load circuit



AC output load circuit

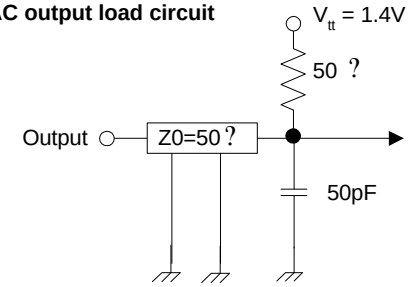


Figure 1

Operating AC Parameter (AC operating conditions unless otherwise noted)

	Symbol	Time	Unit	Note
Row active to row active delay	t_{RRD} (min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD} (min)	20	ns	1
Row precharge time	t_{RP} (min)	20	ns	1
Row active time	t_{RAS} (min)	45	ns	1
	t_{RAS} (max)	100	us	
Row cycle time	t_{RC} (min)	66	ns	1
Last data in to new col. address delay	t_{CDL} (min)	1	CLK	2
Last data in to row precharge	t_{RDL} (min)	2	CLK	2
Last data in to burst stop	t_{BDL} (min)	1	CLK	2
Col. address to col. address delay	t_{CCD} (min)	1	CLK	

NOTES:

1. The minimum number of clock cycles is determined by dividing the minimum time required by the clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.

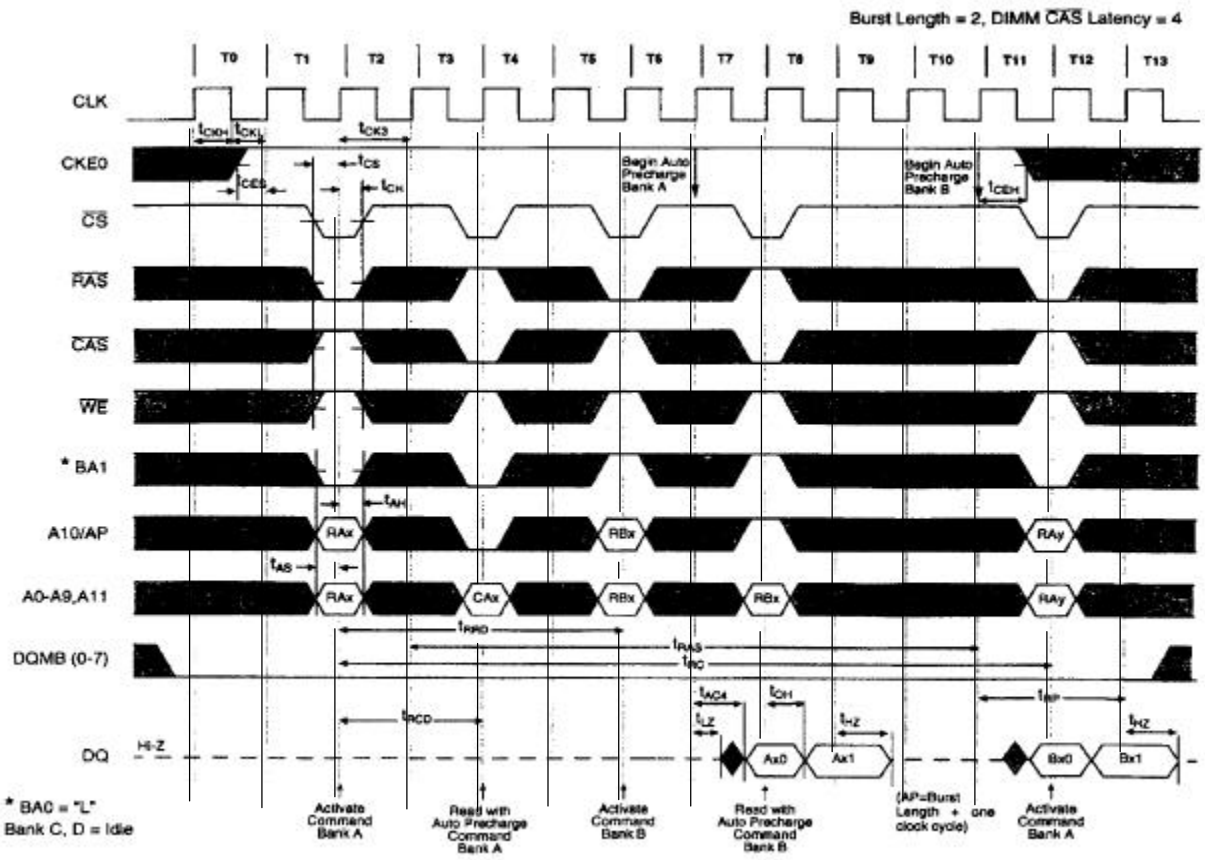
AC Characteristics (AC operating conditions unless otherwise noted)

	CAS	Symbol	Minimum	Maximum	Unit	Notes
CLK cycle time	CAS latency = 3	t_{CK}	7.5		ns	1
	CAS latency = 2	t_{CK}	10.0			
CLK to valid output delay	CAS latency = 3	t_{AC}		5.4	ns	1, 2
	CAS latency = 2	t_{AC}		6		
Output data hold time		t_{OH}	2.7		ns	1, 2
CLK high pulse width		t_{CKH}	2.5		ns	3
CLK low pulse width		t_{CKL}	2.5		ns	3
Input setup time		t_{DS}	1.5		ns	3
Input hold time		t_{DH}	0.8		ns	3
CLK to output in Low-Z		t_{LZ}	1		ns	2
CLK to output in Hi-Z	CAS latency = 3	t_{HZ}		5.4	ns	1
	CAS latency = 2	t_{HZ}		7		

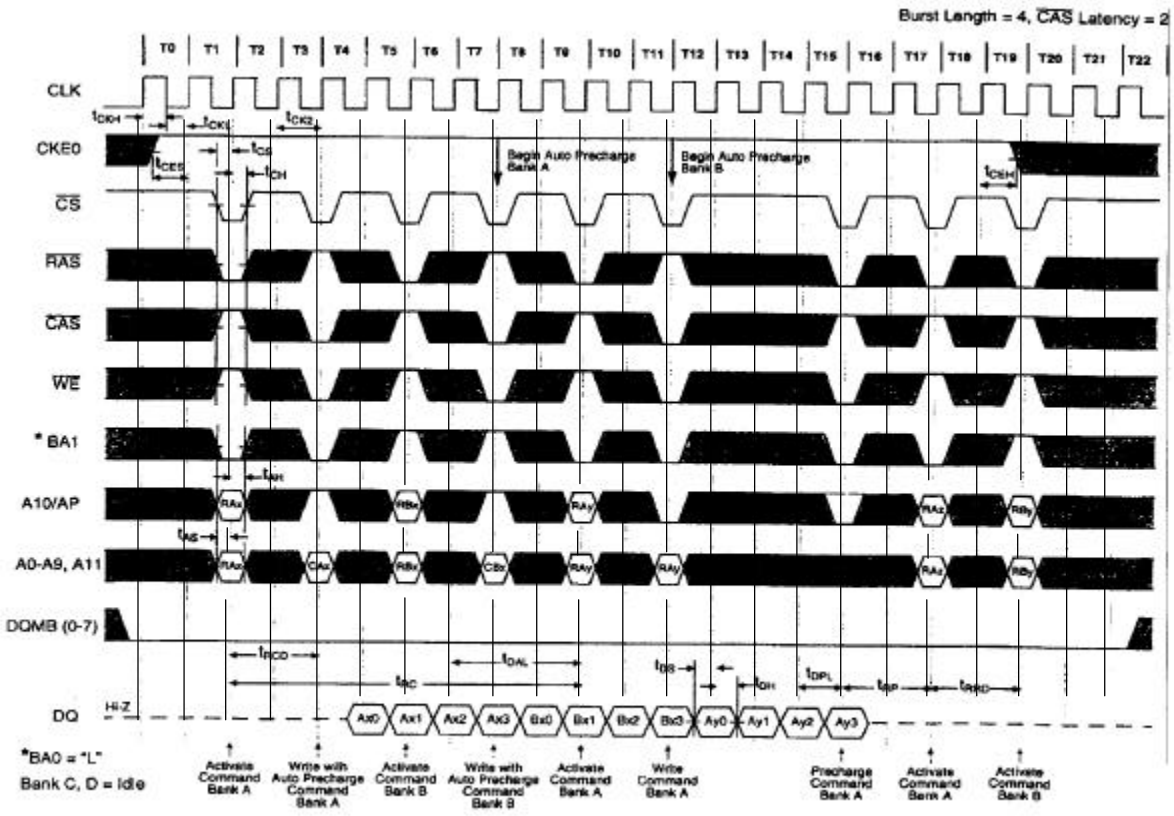
NOTES:

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr and tf) = 1ns.
   If tr and tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.

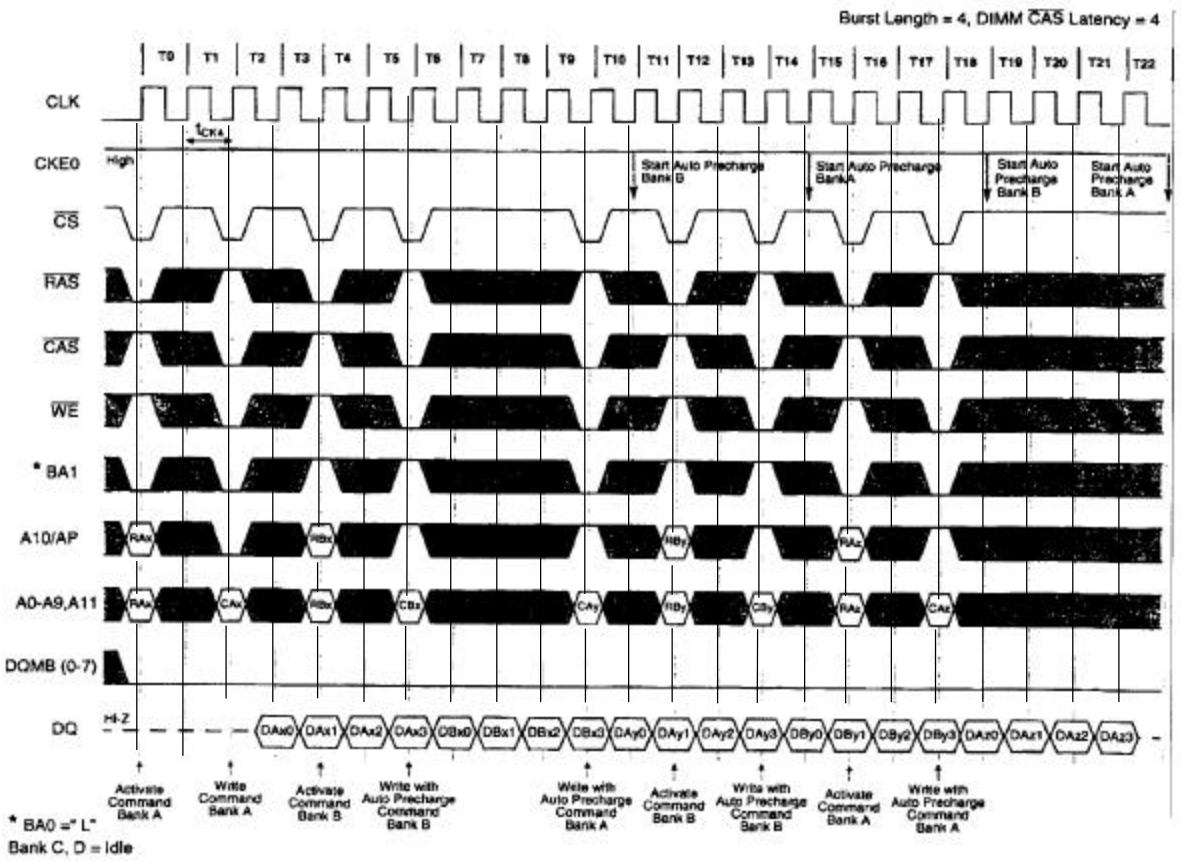
AC Parameters for Read Timing



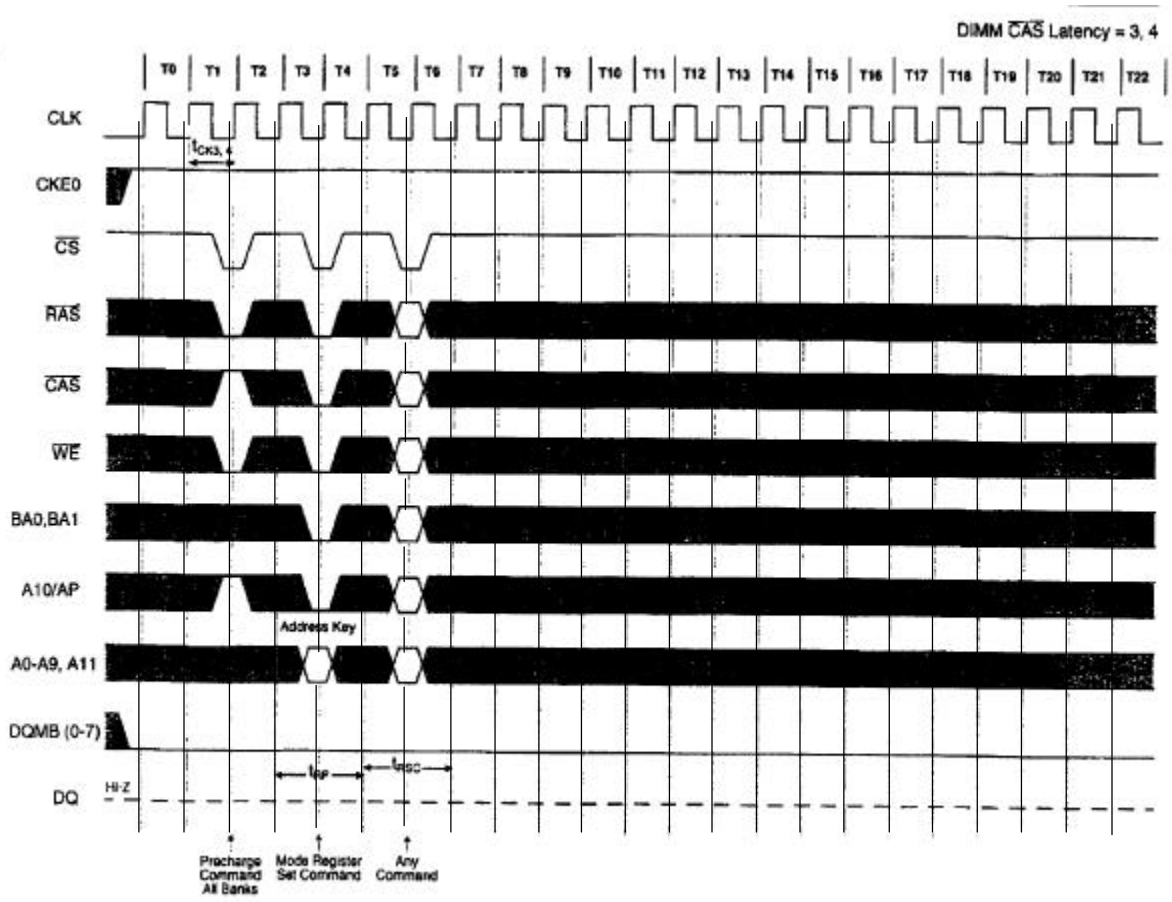
AC Parameters for Write Timing



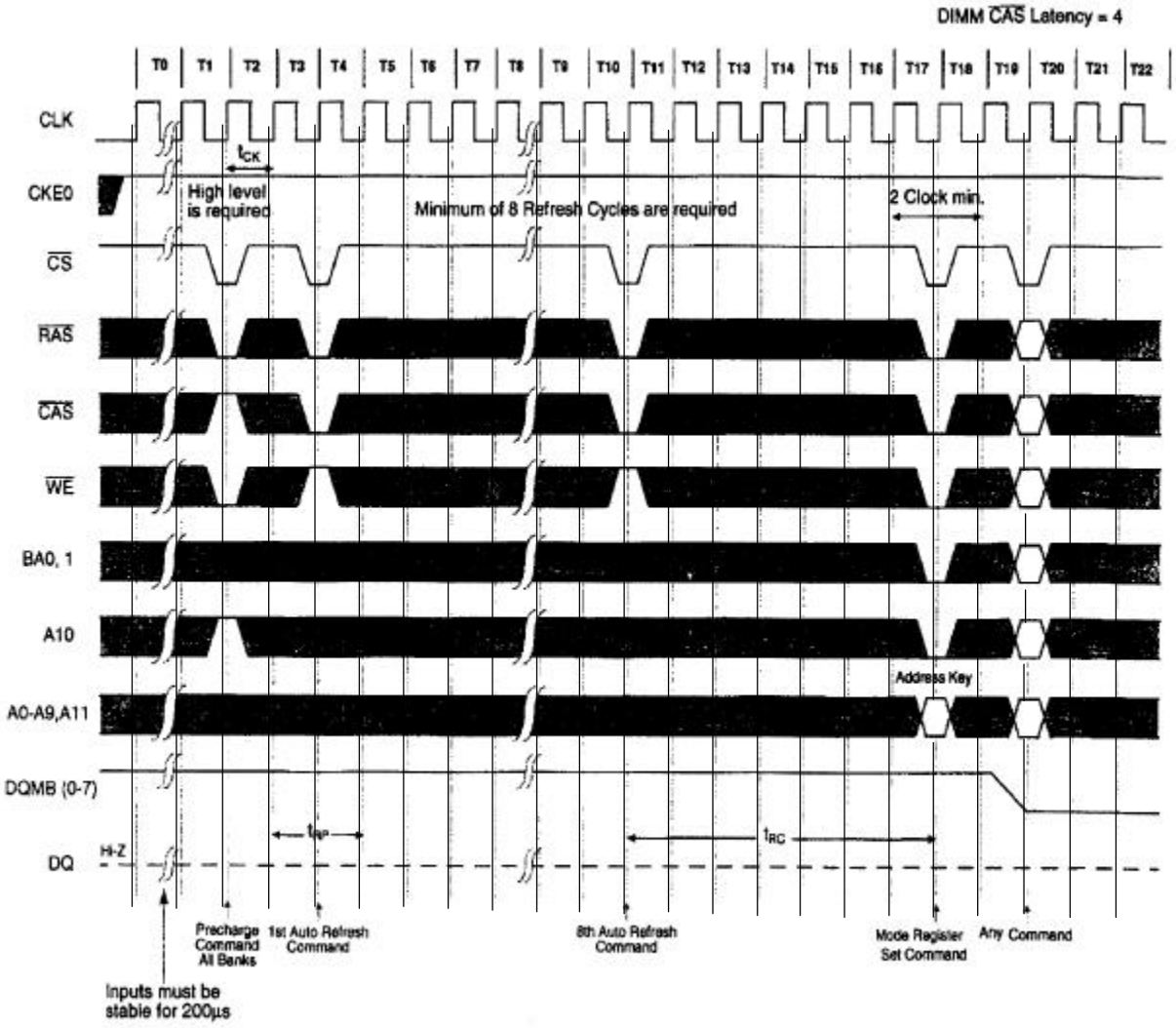
Auto Precharge After Write Burst



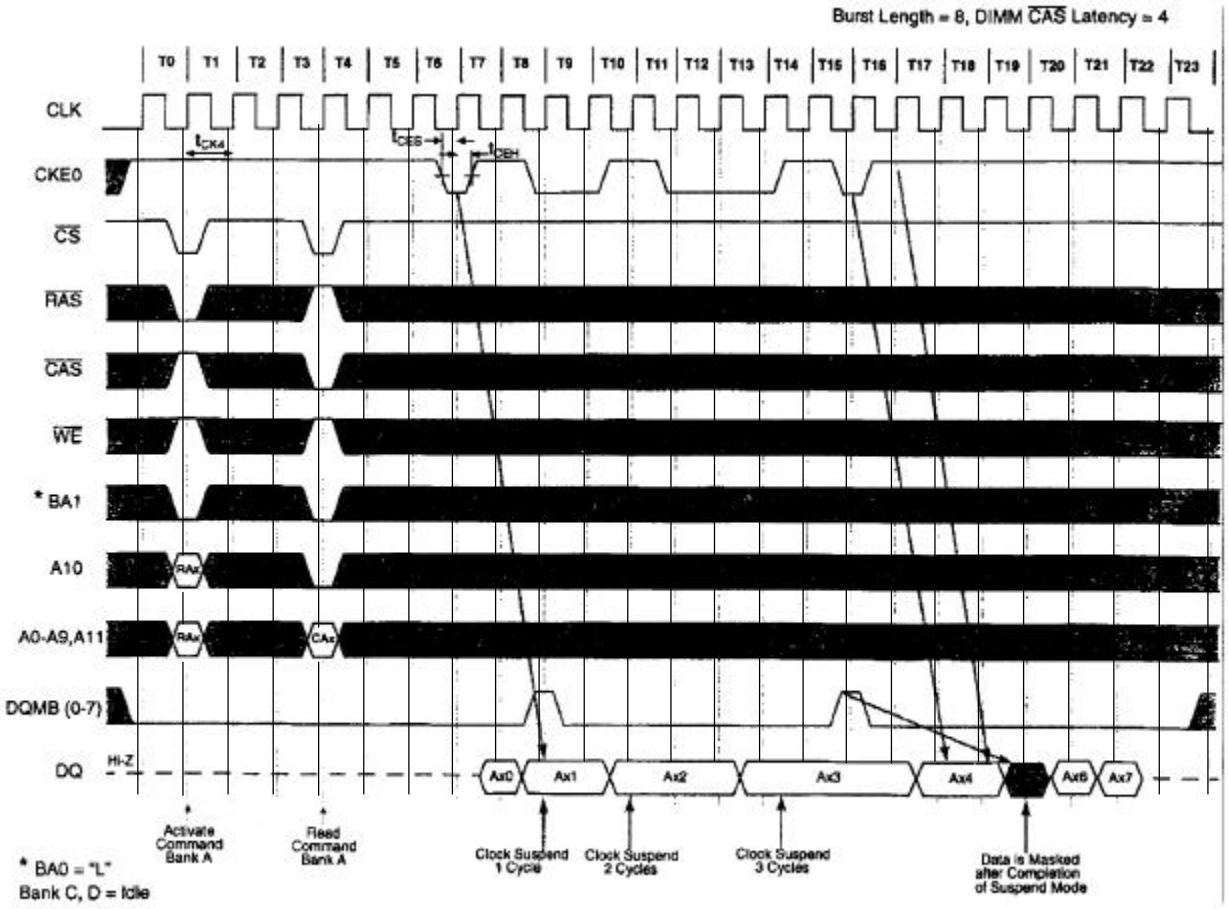
Mode Register Set



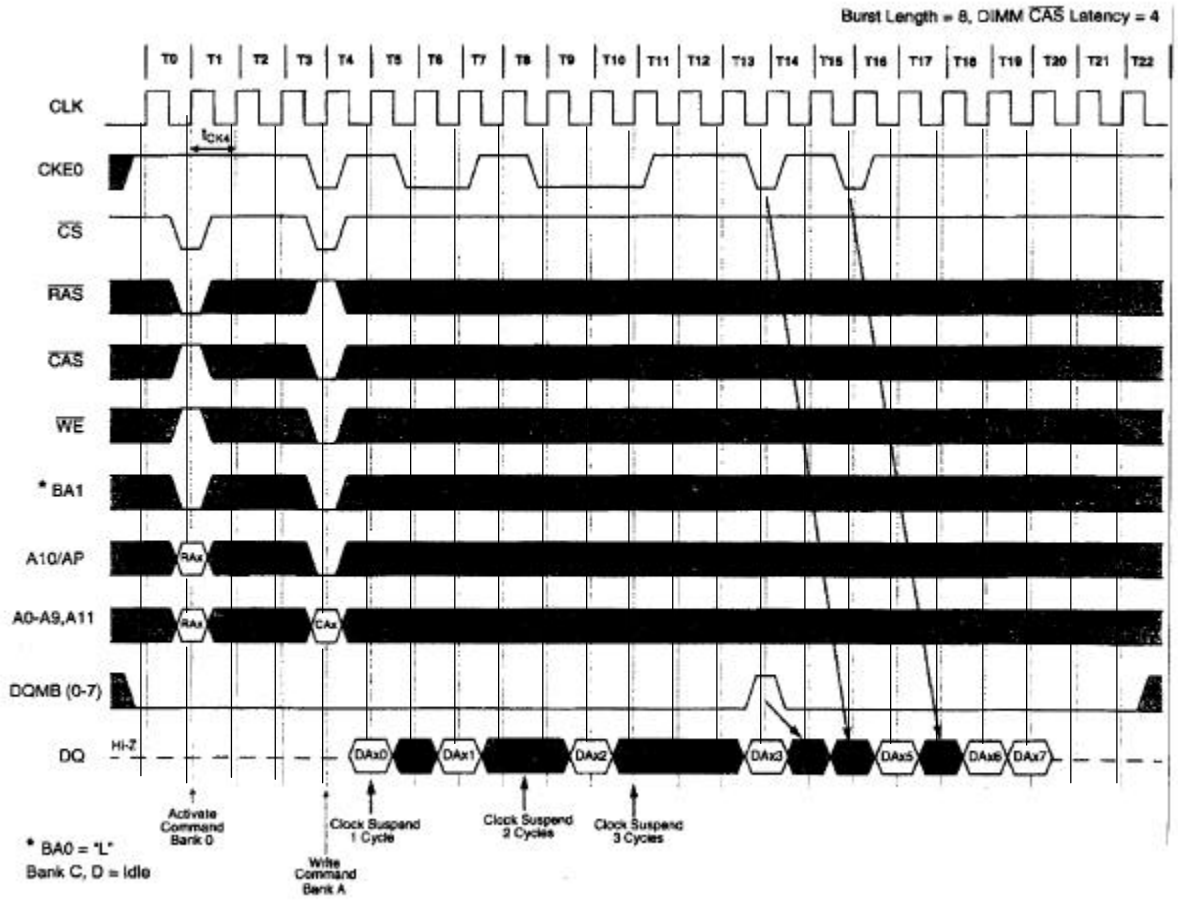
Power On Sequence and Auto Refresh (CBR)



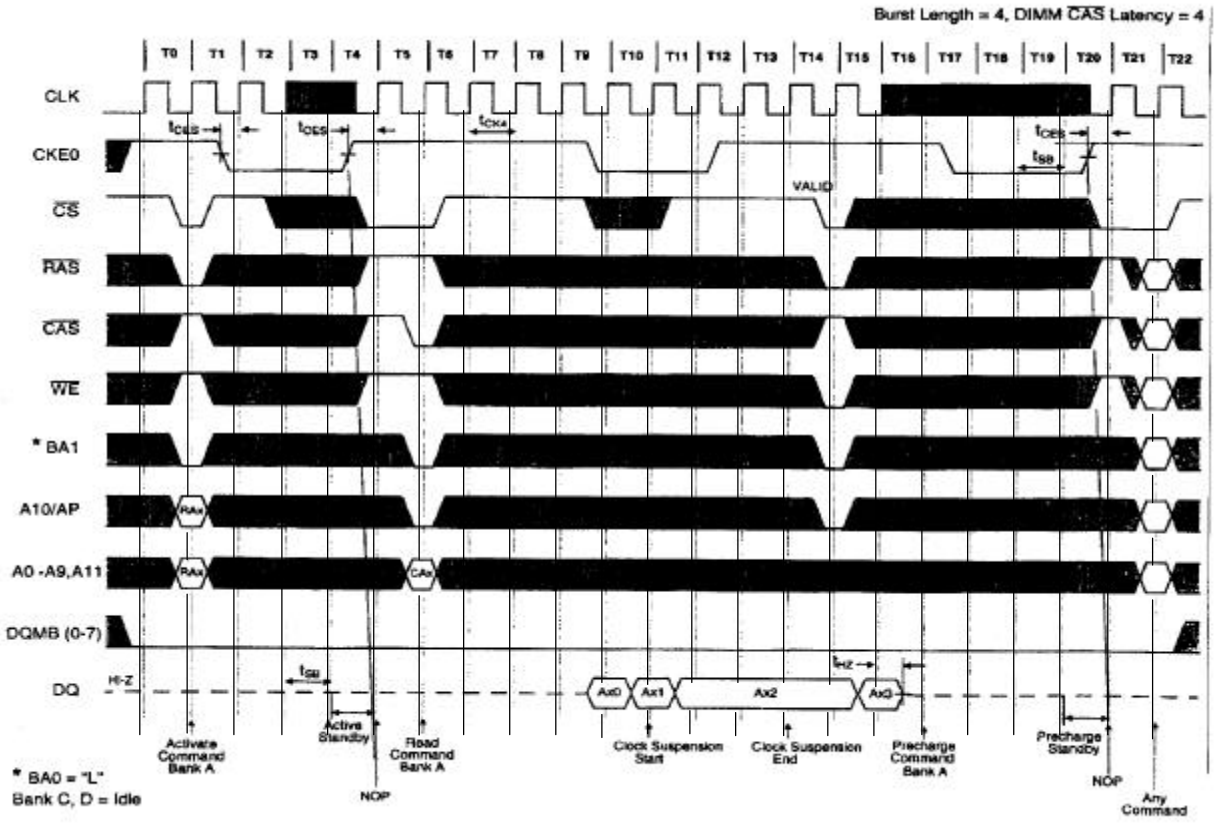
Clock Suspension/DQMB During Burst Read



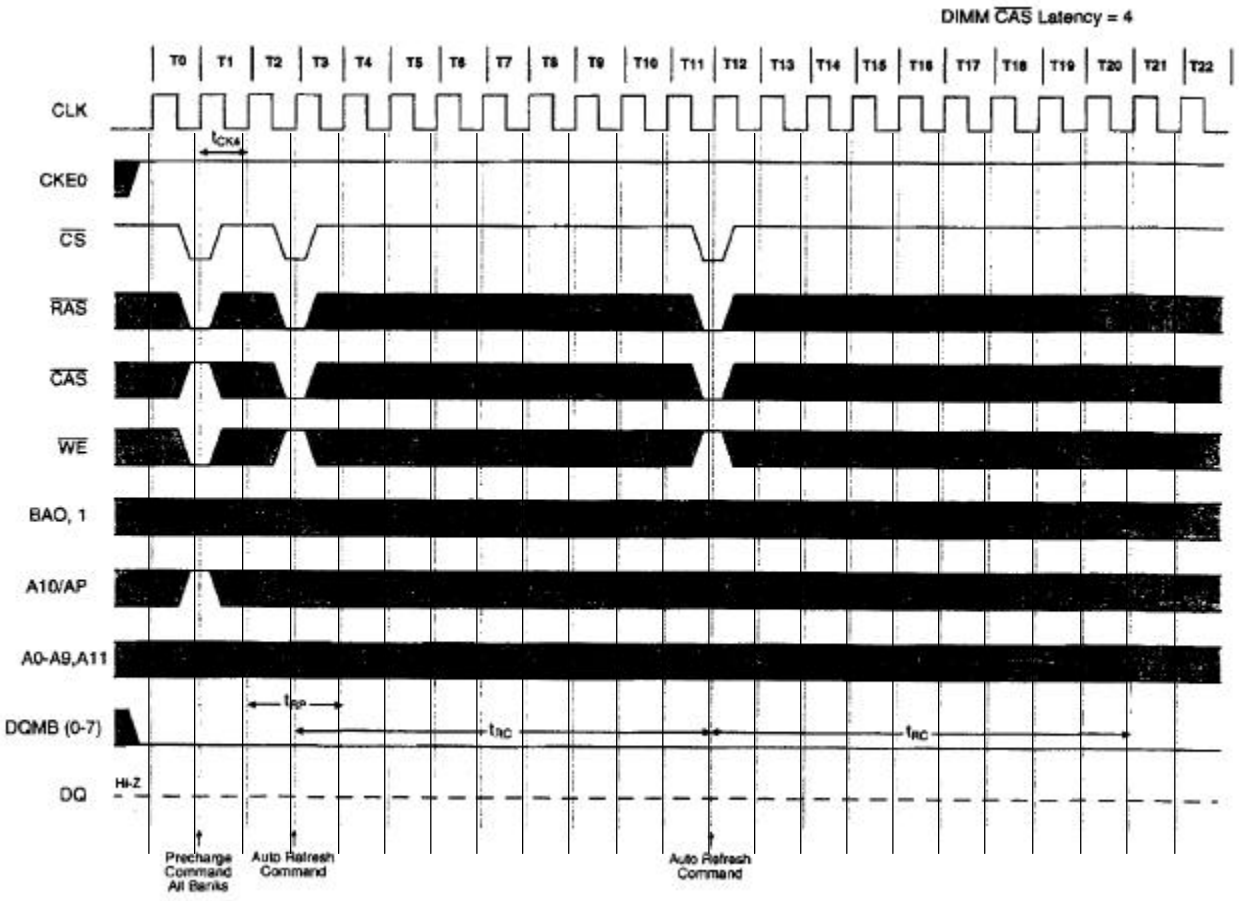
Clock Suspension/DQMB During Burst Write



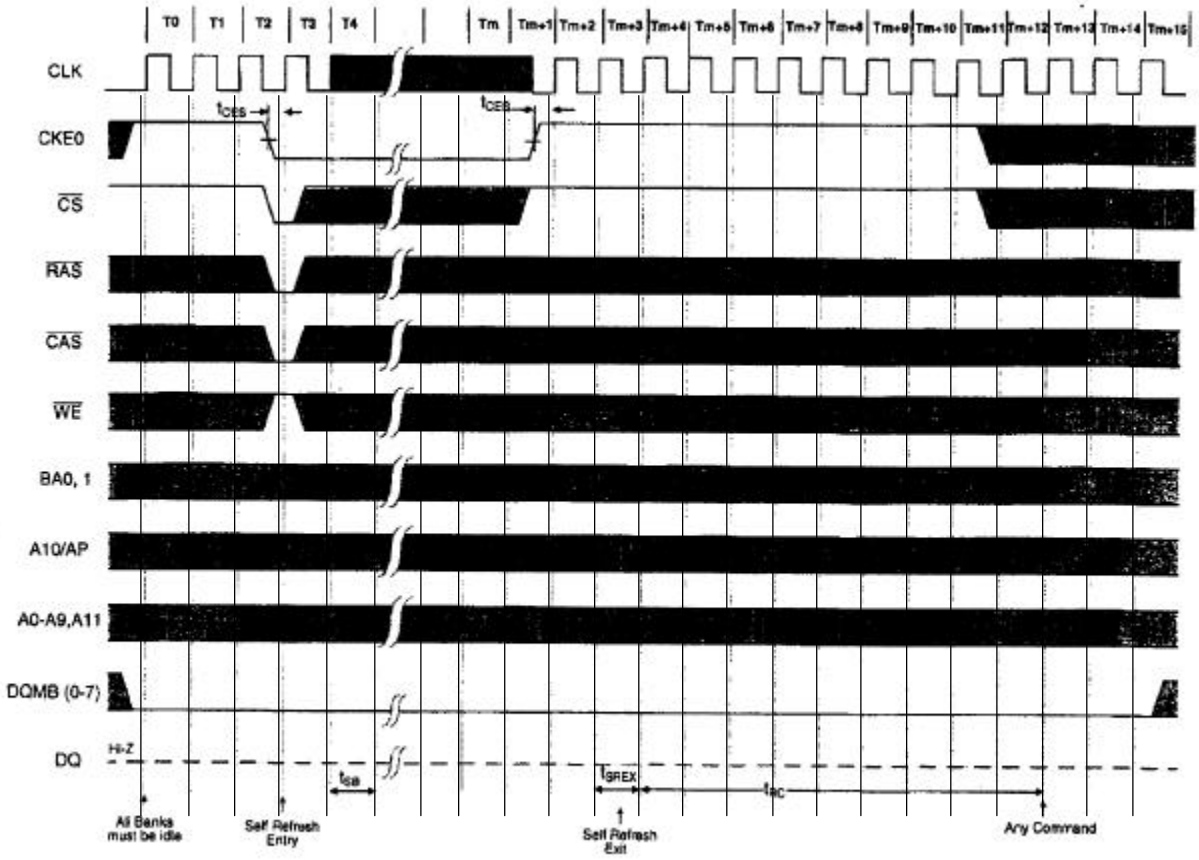
Power Down Mode and Clock Suspend



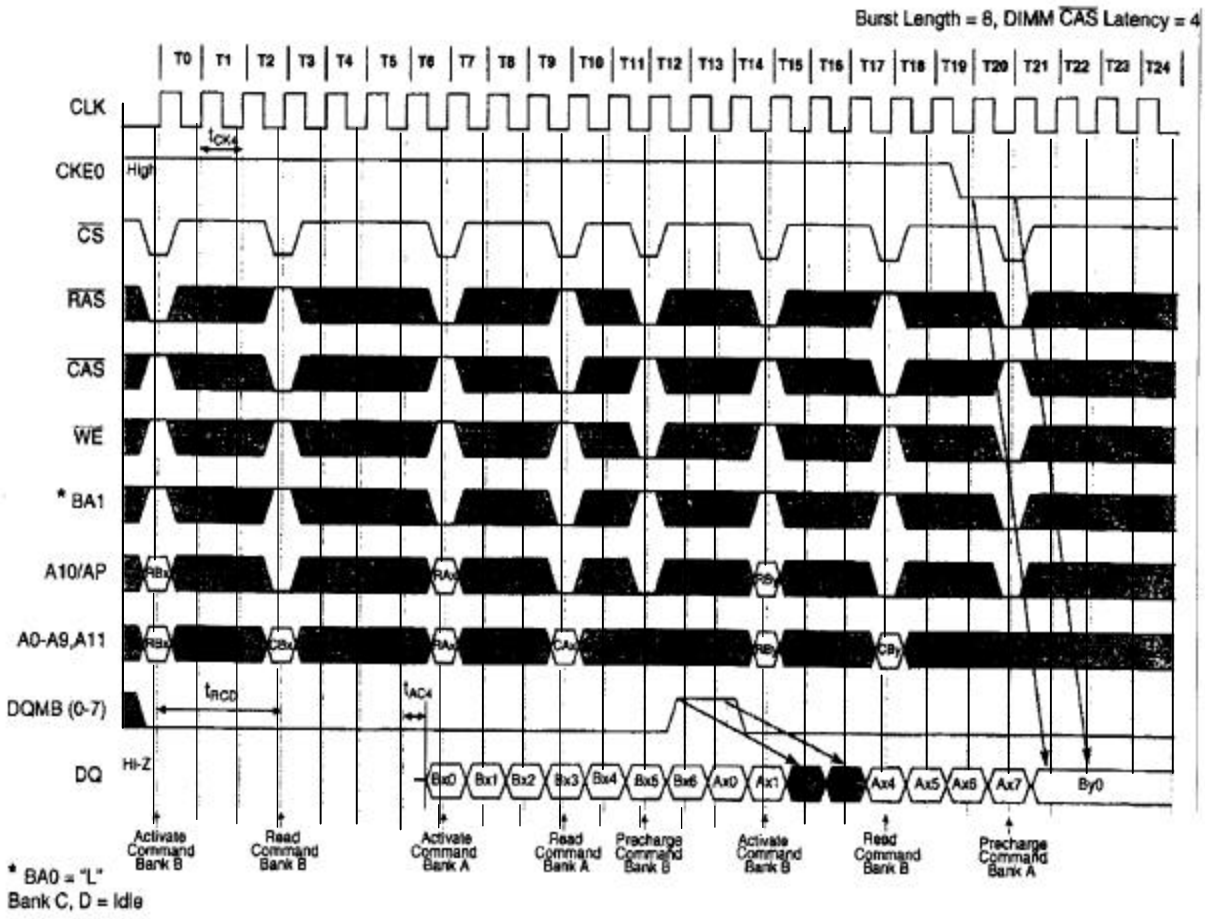
Auto Refresh (CBR)



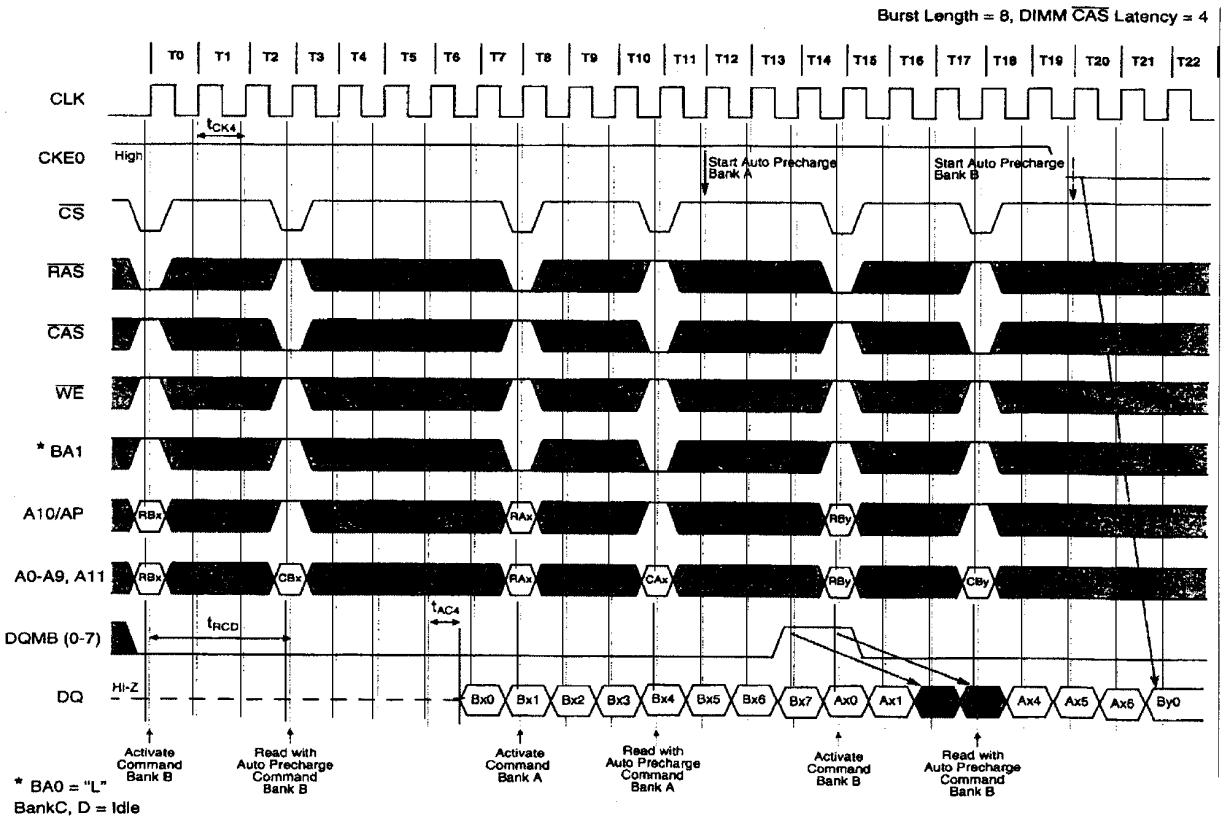
Self Refresh (Entry and Exit)
Note: The CK0 signal must be reestablished prior to DKE0 returning high.



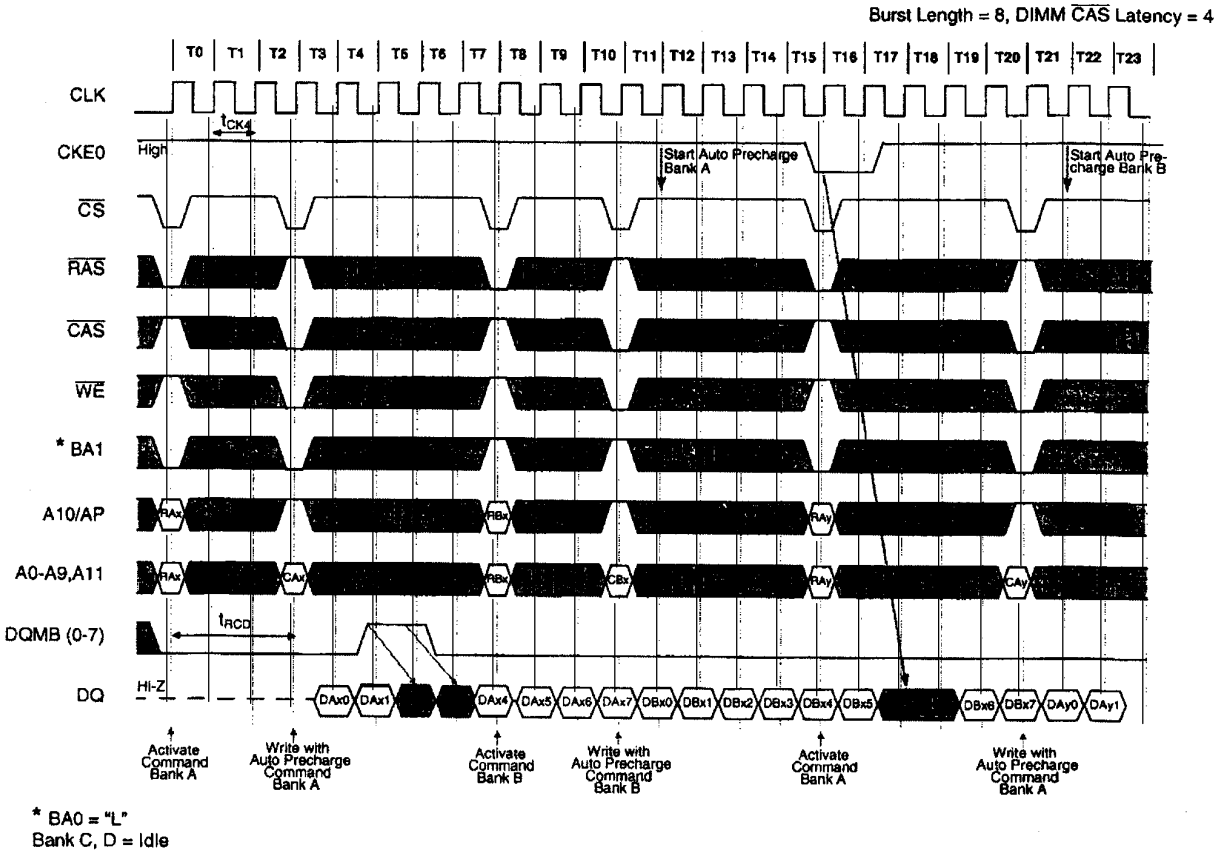
Random Row Read (Interleaving Banks) with Precharge



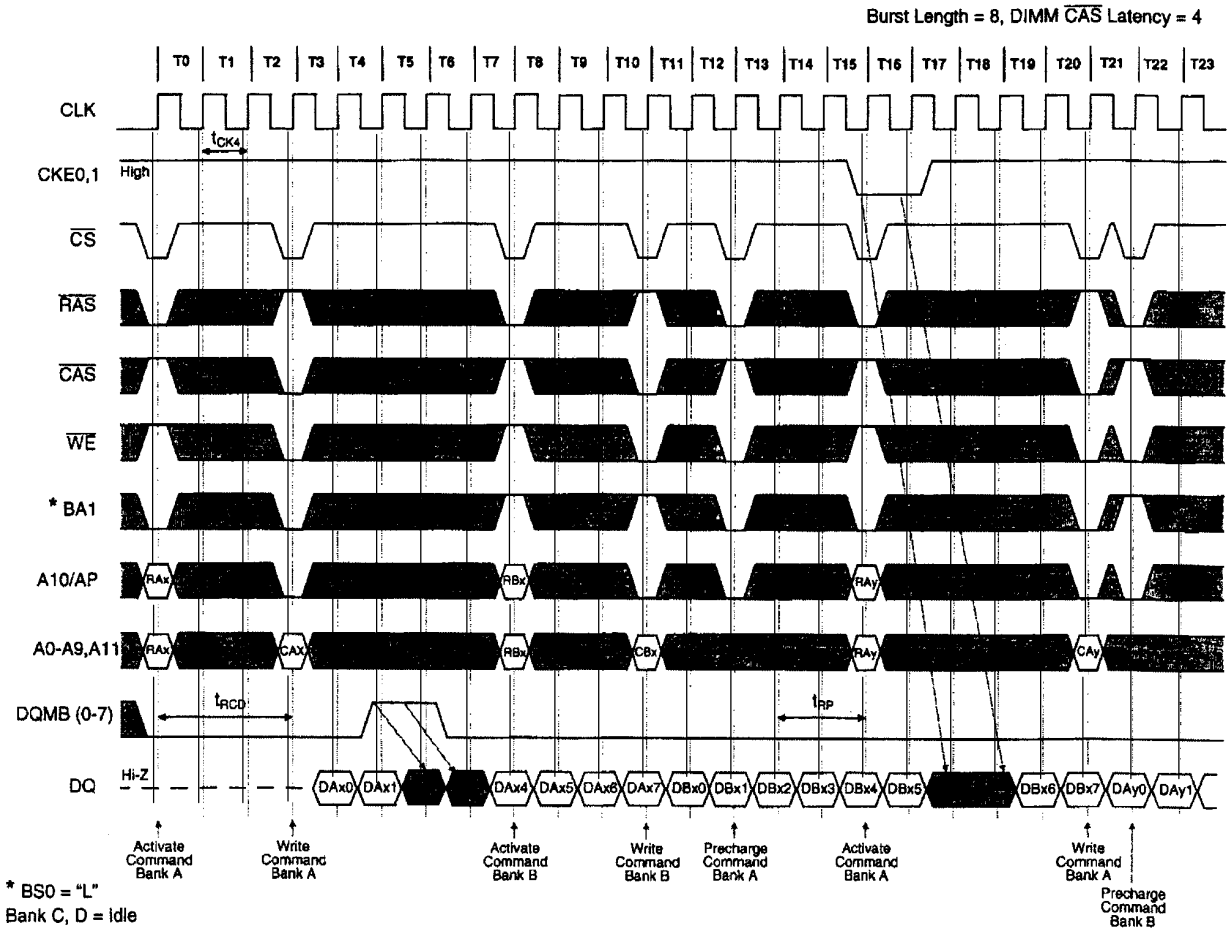
Random Row Read (Interleaving Banks) with Auto-Precharge



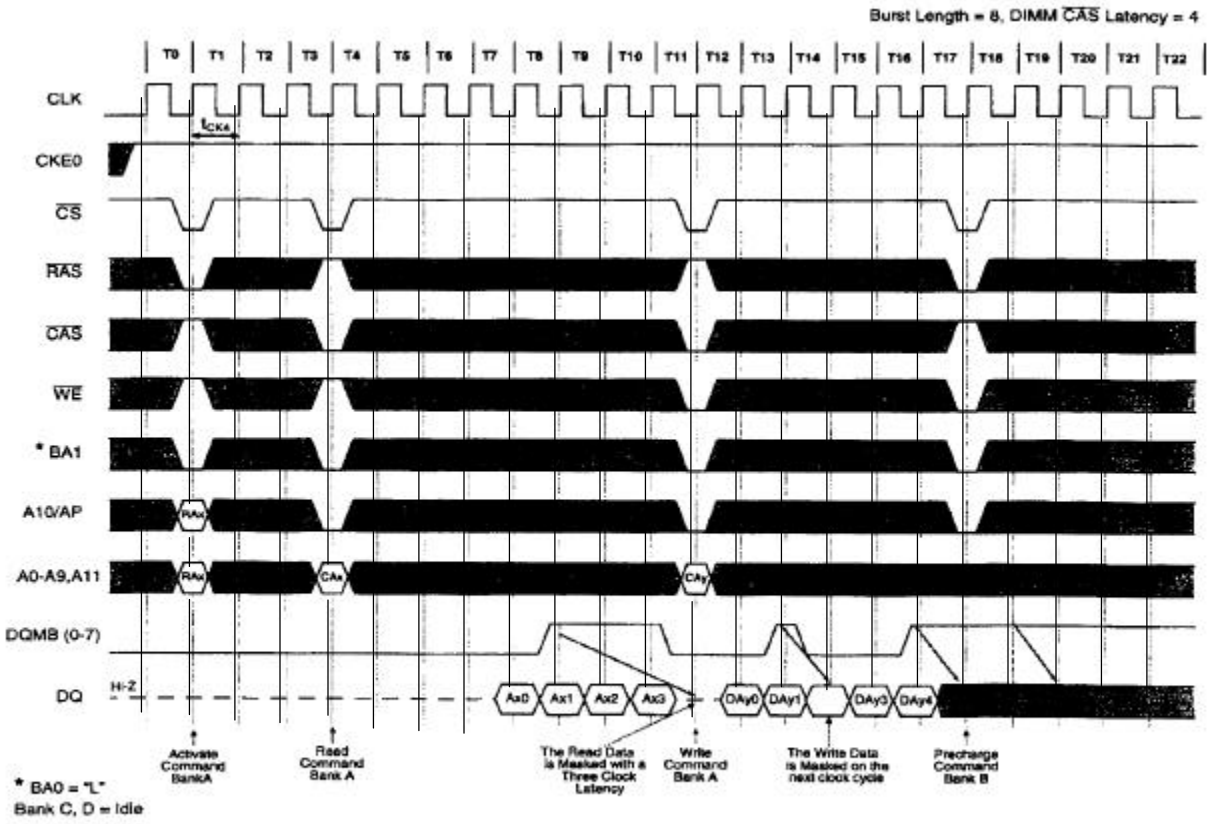
Random Row Write (Interleaving Banks) with Auto-Precharge



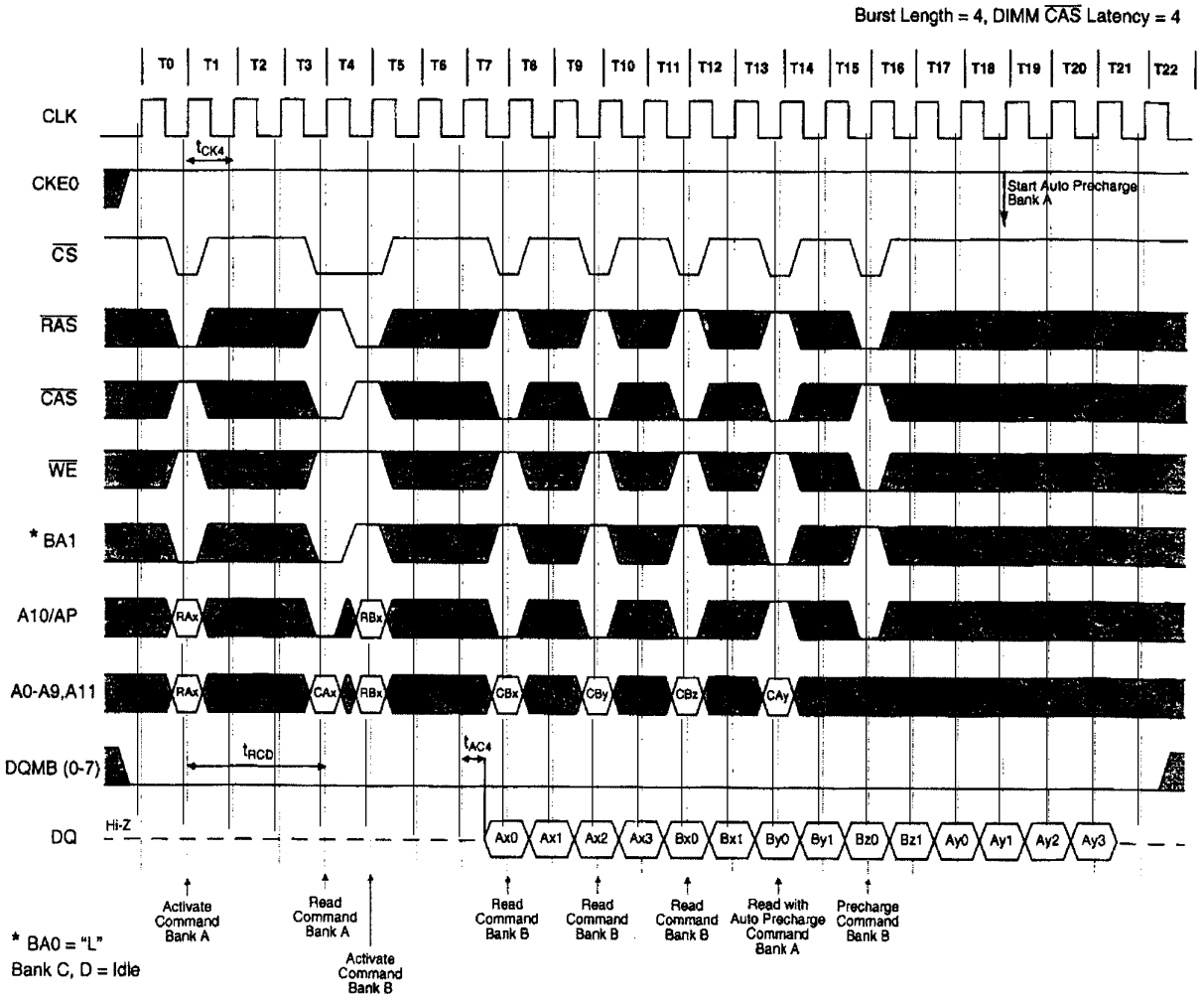
Random Row Write (Interleaving Banks) with Precharge



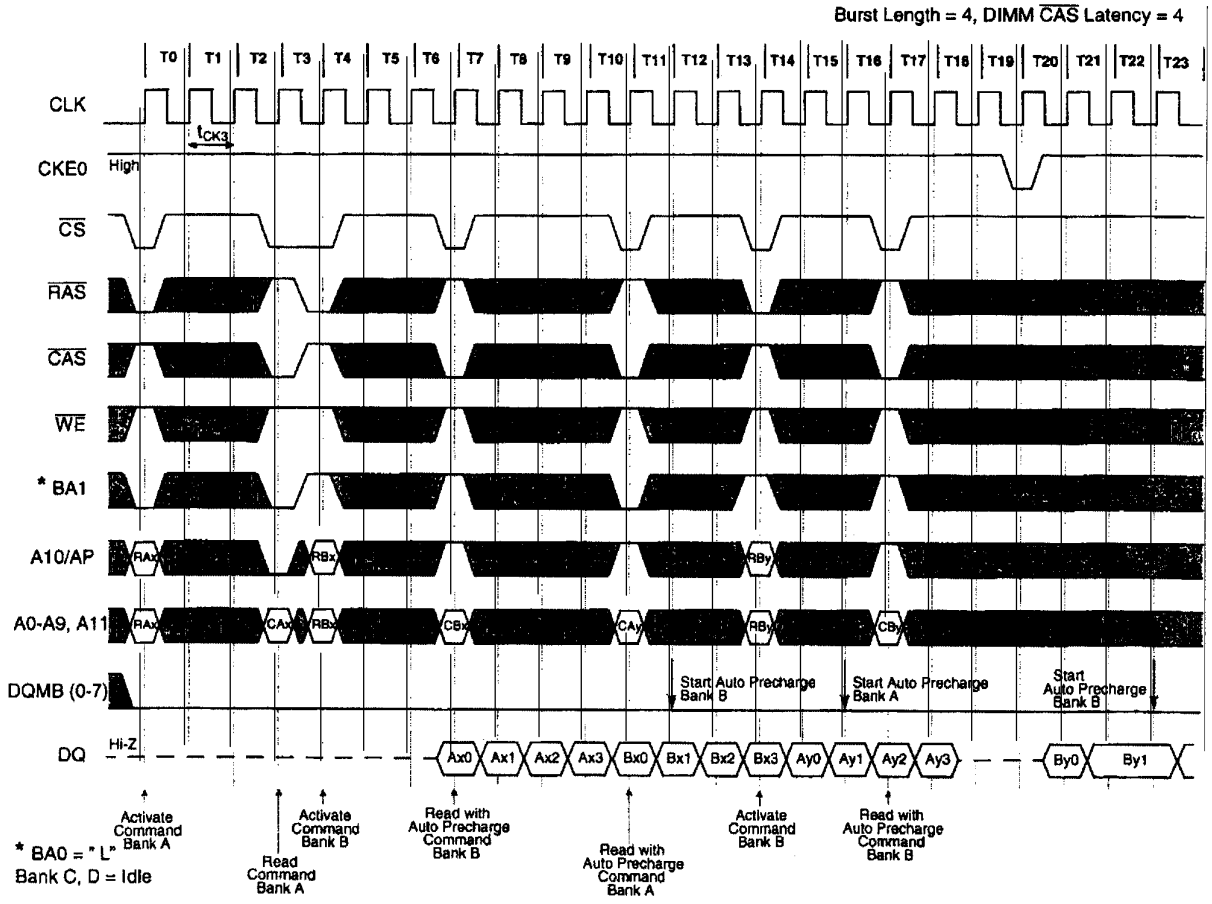
Read/Write Cycle



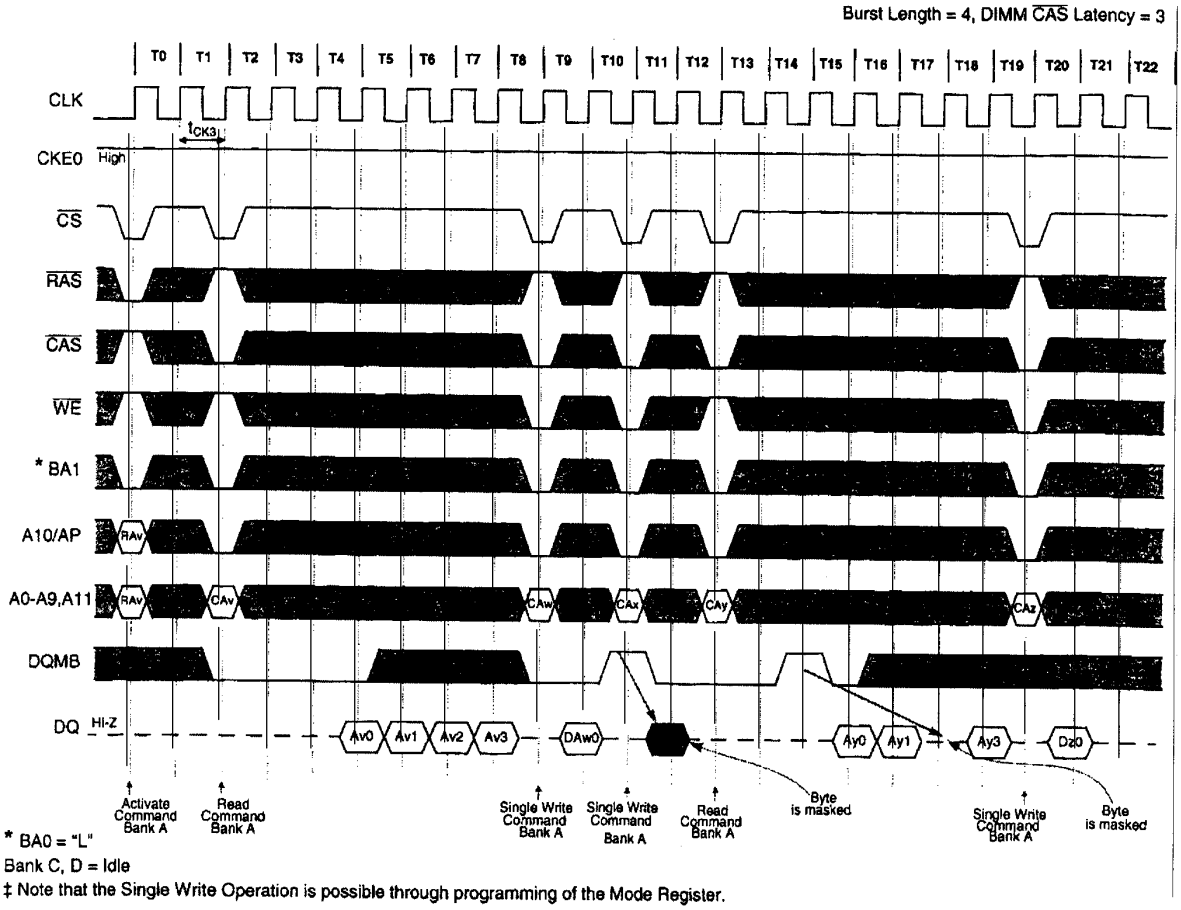
Interleaved Column Read Cycle



Auto-Precharge After Read Burst

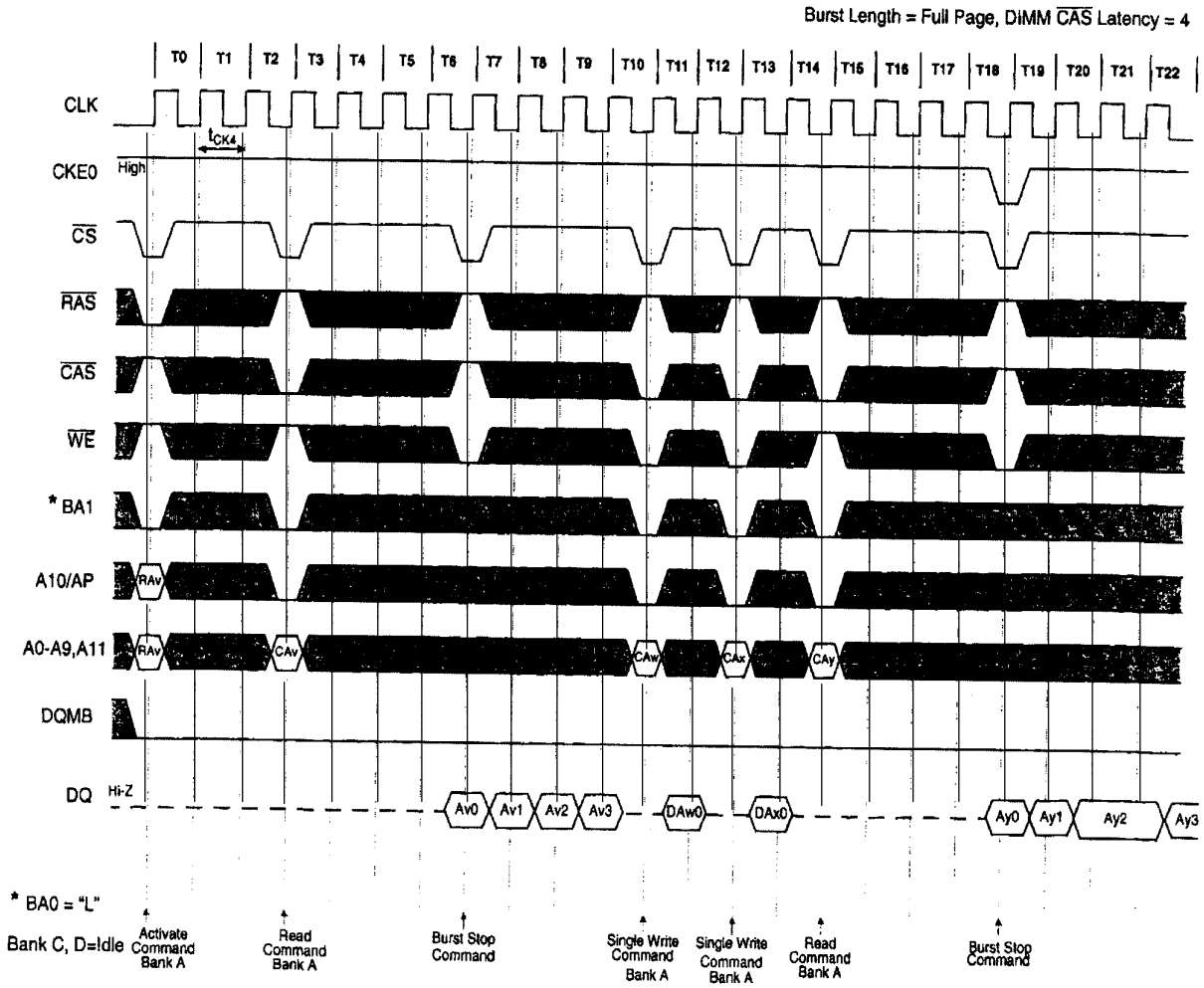


Burst Read and Single Write Operation‡



* BA0 = "L"
Bank C, D = Idle
‡ Note that the Single Write Operation is possible through programming of the Mode Register.

Full Page Burst Read and Single Write Operation‡



‡ Note that Single Write Operation is possible through programming of the Mode Register.