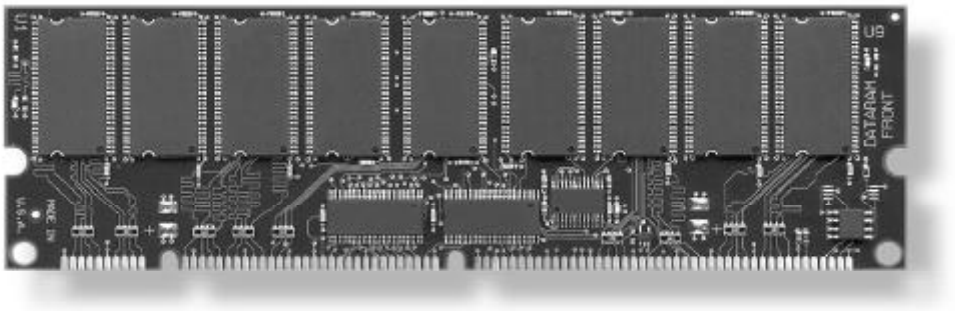
DTM60179

128MB-16M x 72, 168-Pin Registered PC133 SDRAM DIMM



Identification

Part Number:DTM60179

Performance range

133MHz (7.5ns@ CL=2)

Features

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- MRS cycle with address key programs Latency (Access from column address) Burst length (1, 2, 4 & 8 page) Data scramble (Sequential & Interleave)
- Serial presence detect with EEPROM
- 168-pin PC133 DIMM double-sided assembly 5.250" wide by 1.70" high

Description

The Dataram DTM60179 is a registered 16Mx72 Synchronous Dynamic RAM high density memory module. The DTM60179 consists of eight monolithic 16Mx8bit and two monolithic 16Mx4bit SDRAMS in two TSOP-II 400Mil packages, respectively. Three 18-bit Drive ICs for input control, one PLL for clock, and one 2K EEPROM for Serial Presence Detect are installed on a 168-pin glass-epoxy substrate. Sychronous design allows for precise cycle control with the use of a system clock. The DTM60179 is a Dual in-line Memory Module intended for mounting into a 168-pin connector socket. Each module is addressed by 12 row lines, 10 column ines, 2 bank addresses and is organized as one physical bank.

Pin configurations

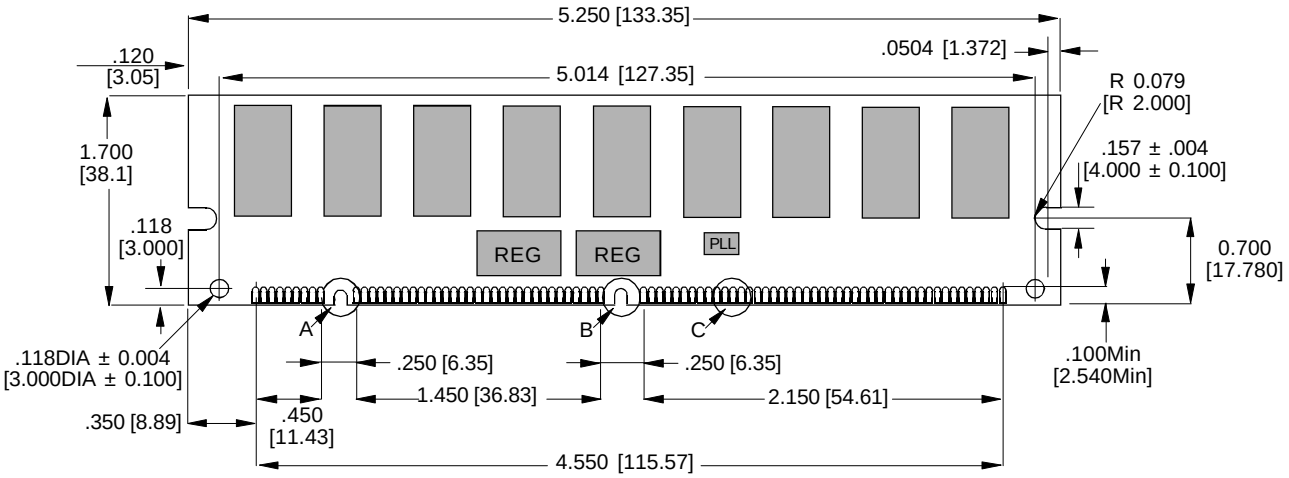
Front side						Back side					
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	Vdd	87	DQ33	115	RAS	143	Vdd
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vdd	34	A2	62	*Vref	90	Vdd	118	A3	146	*Vref
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	Vdd	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	Vdd	101	DQ45	129	*CS3	157	Vdd
18	Vdd	46	DQM2	74	DQ28	102	Vdd	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vdd	77	DQ31	105	CB4	133	Vdd	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vdd	54	Vss	82	SDA	110	Vdd	138	Vss	166	SA1
27	WE	55	DQ16	83	SCL	111	CAS	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	Vdd	112	DQM4	140	DQ49	168	Vdd

Pin names

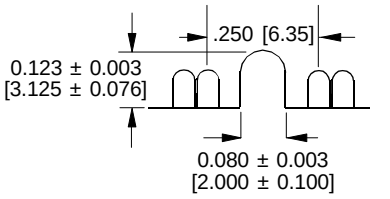
Pin name	Function
A0-A11	Address input (Multiplexed)
BA0-BA1	Select bank
DQ0-DQ63	Data input/output
CB0-CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0-CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0-DQM7	DQM
Vdd	Power supply (3.3V)
Vss	Ground
Vref	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
DU	Don't use
NC	No connection
WP	Write protection

* These pins are not used in this module.

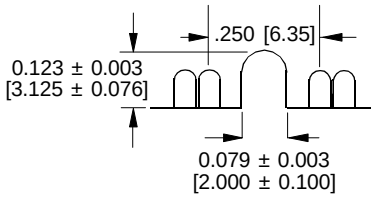
Front view



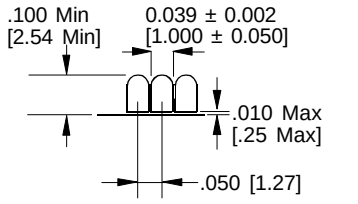
Detail A



Detail B

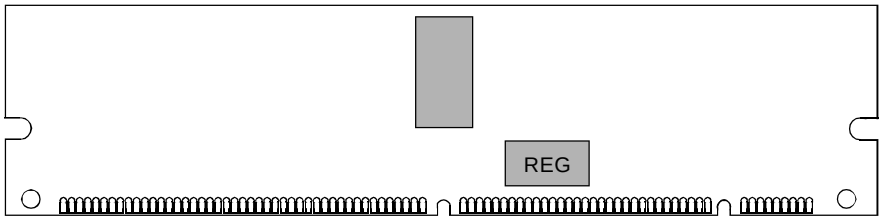


Detail C

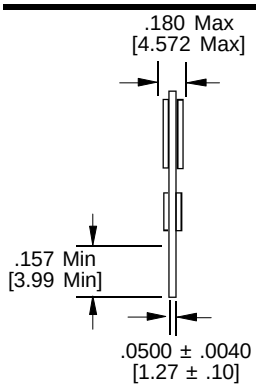


Units: Inches (Millimeters)

Back view



Side view

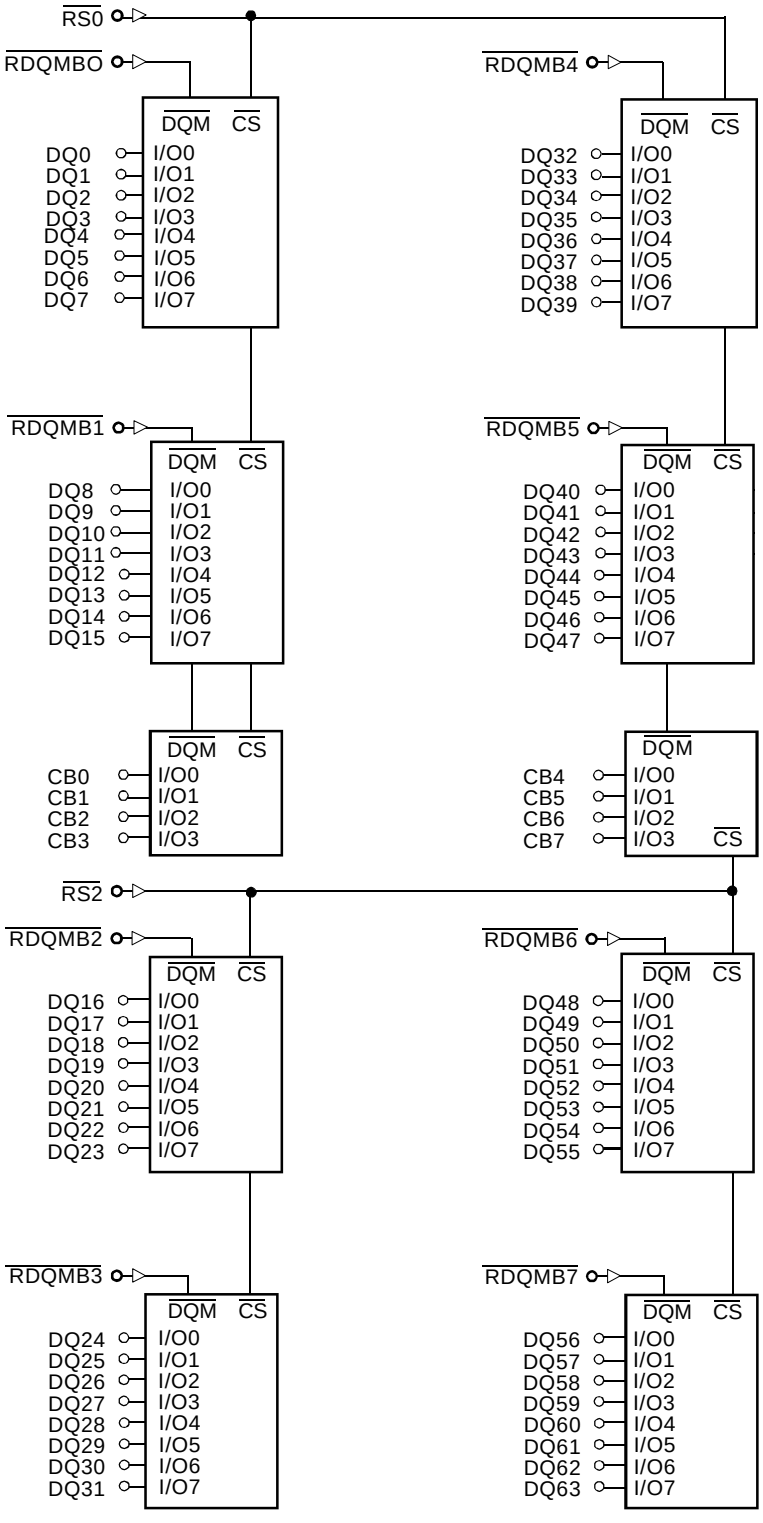


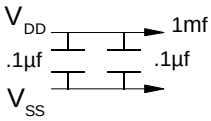
Notes

Tolerances on all dimensions except where otherwise indicated are ±.005 [.13].

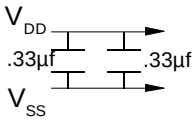
The used device is 32Mx4 SDRAM, TSOP

All dimensions are expressed: inches [millimeters].


RS0
RDQMBO
DQM CS
DQ0 I/O0
DQ1 I/O1
DQ2 I/O2
DQ3 I/O3
DQ4 I/O4
DQ5 I/O5
DQ6 I/O6
DQ7 I/O7
RDQMB4
DQ32 I/O0
DQ33 I/O1
DQ34 I/O2
DQ35 I/O3
DQ36 I/O4
DQ37 I/O5
DQ38 I/O6
DQ39 I/O7
RDQMB1
DQ8 I/O0
DQ9 I/O1
DQ10 I/O2
DQ11 I/O3
DQ12 I/O4
DQ13 I/O5
DQ14 I/O6
DQ15 I/O7
RDQMB5
DQ40 I/O0
DQ41 I/O1
DQ42 I/O2
DQ43 I/O3
DQ44 I/O4
DQ45 I/O5
DQ46 I/O6
DQ47 I/O7
CB0 I/O0
CB1 I/O1
CB2 I/O2
CB3 I/O3
DQM
CB4 I/O0
CB5 I/O1
CB6 I/O2
CB7 I/O3 CS
RS2
RDQMB2
DQ16 I/O0
DQ17 I/O1
DQ18 I/O2
DQ19 I/O3
DQ20 I/O4
DQ21 I/O5
DQ22 I/O6
DQ23 I/O7
RDQMB6
DQ48 I/O0
DQ49 I/O1
DQ50 I/O2
DQ51 I/O3
DQ52 I/O4
DQ53 I/O5
DQ54 I/O6
DQ55 I/O7
RDQMB3
DQ24 I/O0
DQ25 I/O1
DQ26 I/O2
DQ27 I/O3
DQ28 I/O4
DQ29 I/O5
DQ30 I/O6
DQ31 I/O7
RDQMB7
DQ56 I/O0
DQ57 I/O1
DQ58 I/O2
DQ59 I/O3
DQ60 I/O4
DQ61 I/O5
DQ62 I/O6
DQ63 I/O7
CK0 → PLL
CLK1, CK2, CK3 → Termination



To all x8 SDRAMS



To all x4 SDRAMS