DVxcel MPEG-2 Video CODEC

## Advanced MPEG-2 Video and System CODEC for Consumer Applications

Overview

The DVxcel™ MPEG-2 Video CODEC from C-Cube Microsystems is a high-quality single-chip digital video processing solution ideal for consumer digital recordable products. DVxcel is an MPEG-2 video and system encoder and decoder which also has the capability to simultaneously encode and decode MPEG-2 video, enabling low-cost Digital Video Recorder (DVR) applications.

DVxcel, the latest in the DVx family of CODECs, is based on C-Cube's fourth generation video processor architecture. DVxcel has been optimized, both in hardware design and functionality for high quality, low-cost digital consumer recordable applications. Using C-Cube's proven PerfectView™ encoding algorithm, DVxcel delivers the highest quality video encoding of any consumer-based solution.

Capabilities

- Real-time MPEG-2 ML@MP video and system encoding
- Simultaneous encode and decode of MPEG-2 video streams with audio synchronization
- Single-pass, variable bitrate (VBR) and constant bitrate (CBR) encoding
- Multiple, programmable horizontal resolutions
- On-chip Program Stream multiplexing of compressed or uncompressed audio
- On-chip DVD-VR Real-time Read/Write (RTRW) system level formatting
- MPEG-2 ML@MP video and system decoding

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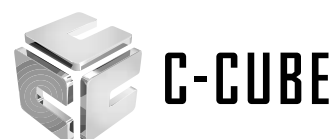
TARGET APPLICATIONS

DVxcel offers significant design advantages for the following applications:

Digital Video Recorder (DVR)

DVxcel can be the core of a low-cost DVR application that has the ability to pause, fast-forward, rewind, and instant-replay live broadcast television. DVxcel simultaneously encodes and decodes video while also ensuring audio/video synchronization. Coupled with an embedded processor, DVxcel can enable a two-chip solution to provide a complete digital video time-shifting application.

DVD/Optical Recorder

Coupled with a DVD decoder (such as C-Cube's ZiVA-4), DVxcel can provide the MPEG-2 video and system encoder portions of a DVD/optical recorder. DVxcel's on-chip MPEG-2 Program Stream multiplexing and

DVD-VR RTRW format generation provide a clean and efficient system design for DVD/optical recorders, while the DVD decoder ensures compatibility with playback of existing content.

Digital-VHS Recorder (D-VHS)

With its high-quality MPEG-2 video and system encode and decode capabilities, and with its optimized host and bit-stream port design, DVxcel is the ideal solution for D-VHS recorders.

Personal TV Functions

DVxcel's programmable architecture can enable advanced personal TV features. While encoding video, Vertical Blanking Interval (VBI) data can be captured and decoded by the CODEC to provide additional digital content information such as closed caption data and electronic programming guide data.
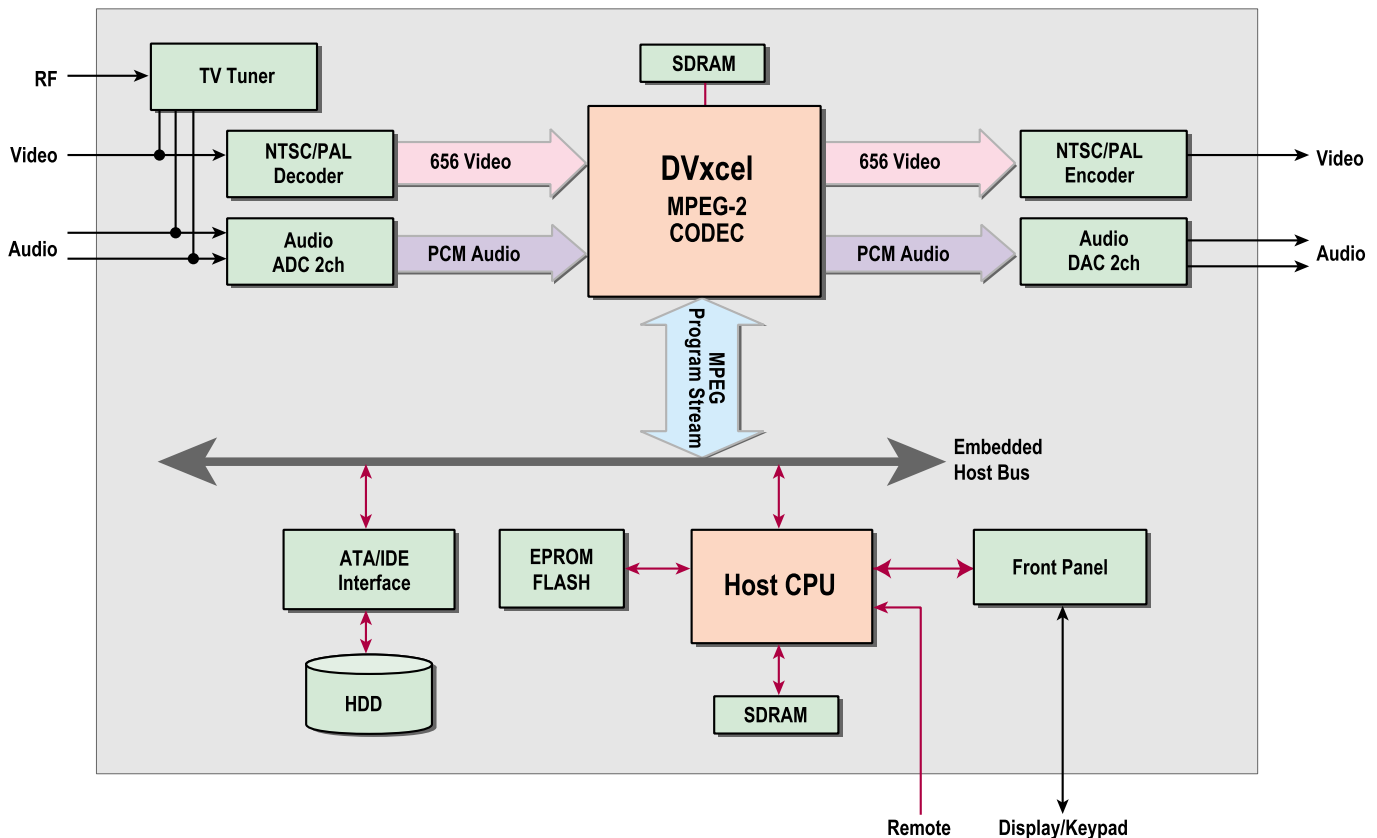
DVxcel Digital Video Recorder (DVR) System Block Diagram
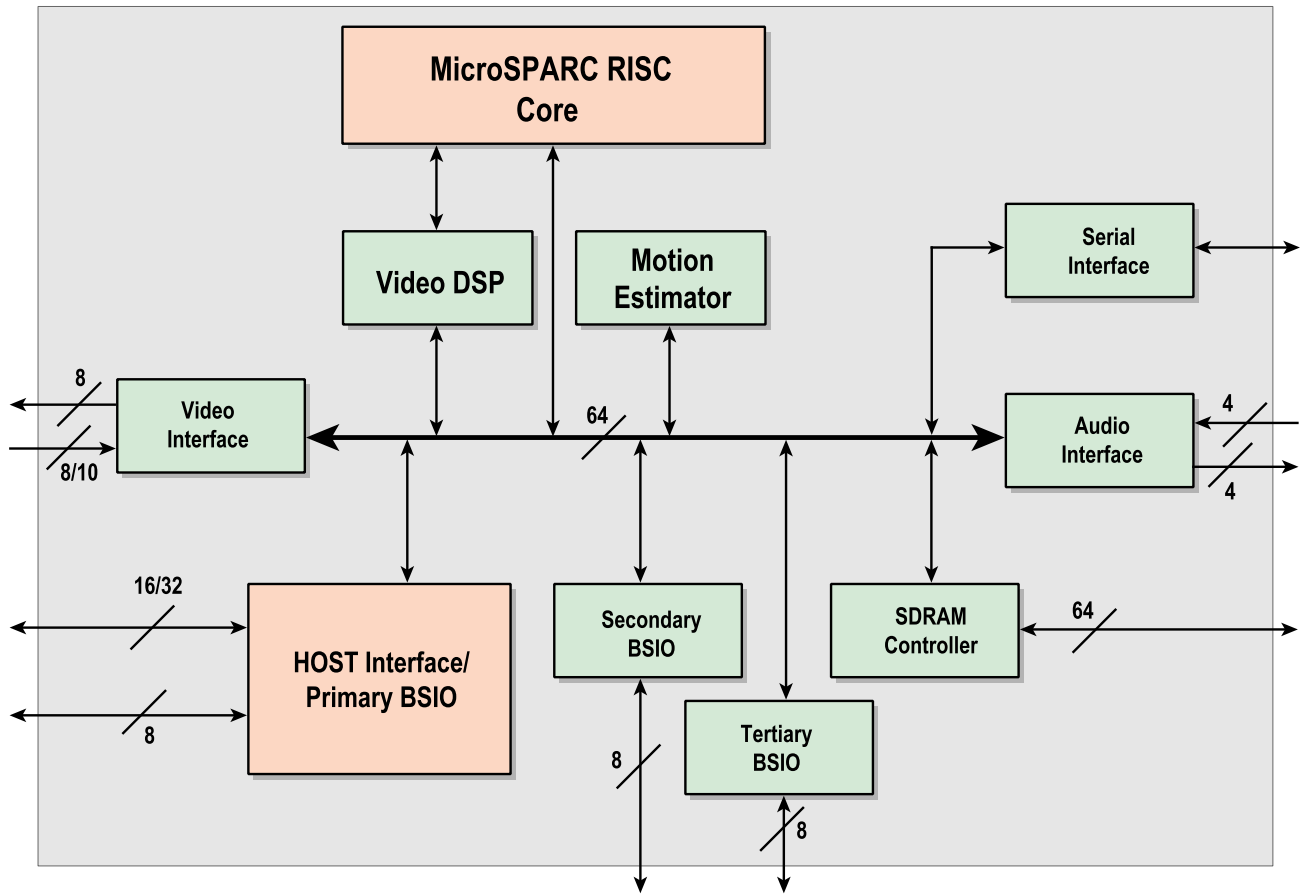
DVxcel Internal Block Diagram

DEVICE FEATURES

Optimized for embedded designs, DVxcel features the following hardware interfaces:

- Flexible 16/32-bit host interface
- Host DMA target or primary 8-bit hardware I/O port for bitstream data transfers
- Secondary 8-bit hardware port for bitstream transfers
- Tertiary 8-bit hardware port for bitstream transfers
- 8- or 10-bit ITU-656 video input port
- 8-bit ITU-656 video output port
- Serial audio interfaces for audio capture and playback

DVxcel is based around a 110MHz micro-SPARC RISC core and includes special hardware to implement:

- Video compression pre-processing
- Motion estimation and compensation
- DCTs and IDCTs
- Variable-length encoding and decoding
- High-quality video scaling and compositing

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Video	Standards	NTSC, PAL, ITU-R BT.656
	Input Dithering	10-bit
	Output	Single-stream at 27 MHz
MPEG-2	Resolutions	Horizontal: 720, 704, 544, 480, 352 Vertical: 480 (NTSC), 576 (PAL)
	Encoding	ML@MP, VBR and CBR
	GOP Structure	I, IP, or IBP
	Bit Rate	1.8 to 10 Mbps
	System	Program Stream multiplexing of video Elementary Stream with audio Elementary Stream (DVD-VR compliant)
Audio	Ports	Four stereo input, four stereo output
	Interface	I2S and other serial interfaces
	Format	16-, 24-, or 32-bit at 32, 44.1, or 48 kHz
System	Host Interface	Flexible host interface with I-Mode, M-Mode, Wait, and DTACK
	Access Transfer	16-bit or 32-bit PIO 16-bit or 32-bit target DMA Three, 8-bit hardware-controlled bitstream ports
Memory	Configuration	8 Mbytes of external SDRAM
	Controller	On-chip, 64-bit-wide SDRAM interface
	Peak Bandwidth	880 Mbyte/s
Physical	Input Voltages	3.3 V I/O, 2.0 V Core
	System Clock	110 MHz
	Packaging	308-pin Ball Grid Array
	Operating Power	< 1.8 W @ VDDQ = 2.0 V typical
JTAG	Compliance	IEEE 1149.1 compliance for boundary scan testing

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