d010000
256X32, Mux 4, Drive 3, Non-Pipelined
High-Speed Single-Port Synchronous SRAM

Features

- Precise Optimization for Infineon's C9DD1 0.20µm Embedded DRAM Process
- Fast Access Time (1.90ns at typical process, 2.50V, 25˚C)
- Fast Cycle Time (1.54ns at typical process, 2.50V, 25˚C)
- Extremely High Density (area is 0.62mm^2)
- Universal Test Interface™
- Completely Static Operation
- Optional Output Register (Pipeline)
- Near-Zero Hold Time (Data, Address, and Control Inputs)
- Selectable Frequency
- Selectable Output Drive Strengths (3X and 12X)

Memory Description

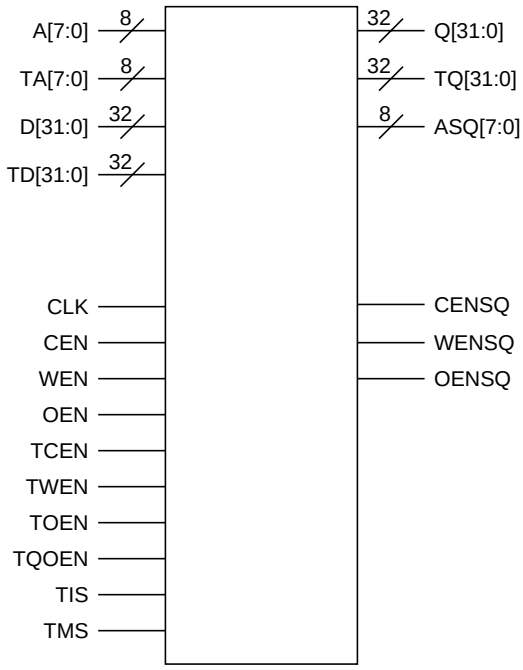
The 256X32 SRAM is a high-performance, synchronous single-port, 256-word by 32-bit memory designed to take full advantage of Infineon's C9DD1 0.20µm embedded DRAM process.

The SRAM's storage array is composed of six-transistor cells and all memory circuitry is fully static. The SRAM operates at a voltage of 2.5V ± 10% and a junction temperature range of -25˚C to +110˚C.

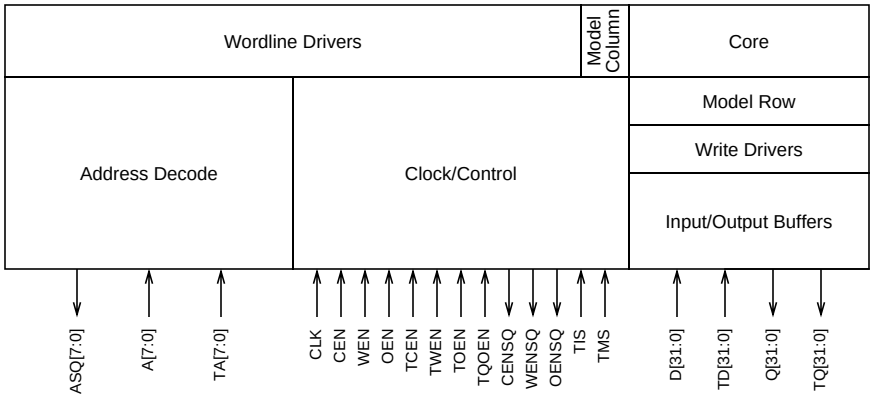
Pin Description

Pin	Description
A[7:0]	Addresses (A[0] = LSB)
D[31:0]	Data Inputs (D[0] = LSB)
CLK	Clock Input
CEN	Chip Enable
WEN	Write Enable
OEN	Output Enable
Q[31:0]	Data Outputs (Q[0] = LSB)
TA[7:0]	Test Addresses
TD[31:0]	Test Data Inputs
TCEN	Test Chip Enable
TWEN	Test Write Enable
TOEN	Test Output Drive Enable
TQOEN	Test Data Output Drive Enable
TIS	Test Input Select
TMS	Test Mode Select
TQ[31:0]	Test Data Outputs
ASQ[7:0]	Address Scan Register Outputs
CENSQ	Chip Enable Scan Register Output
WENSQ	Write Enable Scan Register Output
OENSQ	Output Enable Scan Register Output

Symbol



SRAM Block Diagram



SRAM Timing: Mission Mode

Typical Process, 2.50 Volts, 25˚C

Parameter	Symbol	Min (ns)	Max (ns)	Parameter	Symbol	Min (ns)	Max (ns)
Cycle time	t_{cyc}	1.54		Data setup	t_{ds}	0.54	
Access time*‡	t_{a}		1.90	Data hold	t_{dh}	0.00	
Address setup	t_{as}	0.63		Output enable to hi-Z	t_{hz}		1.00
Address hold	t_{ah}	0.00		Output enable active*	t_{lz}		1.12
Chip enable setup	t_{cs}	0.55		Output hold*	t_{oh}	1.63	
Chip enable hold	t_{ch}	0.00		Clock high	t_{ckh}	0.19	
Write enable setup	t_{ws}	0.84		Clock low	t_{ckl}	0.18	
Write enable hold	t_{wh}	0.00		Clock rise slew	t_{ckr}		15.68

* Parameter has a load dependence: K_{load} = 1.46ns/pF

‡ For a pipelined memory, there will be a one clock latency

Clock and Mode Select Timing

FIGURE 1. Synchronous Single-Port SRAM Test Control Signal Timing

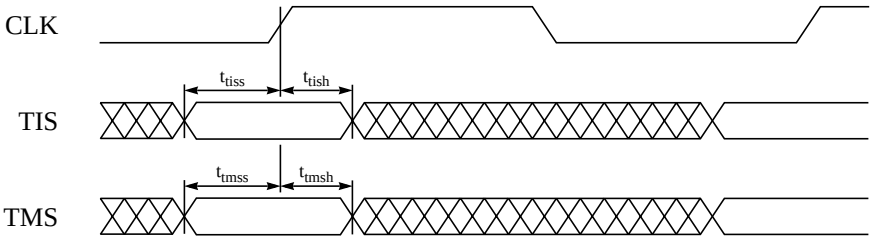


FIGURE 2. Synchronous Single-Port SRAM Test-Mode-Select Output Timing

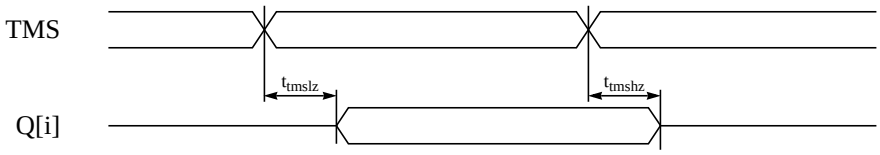
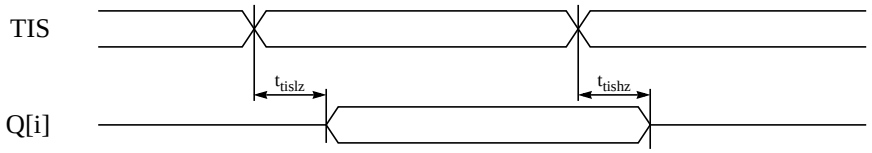


FIGURE 3. Synchronous Single-Port SRAM Test-Input-Select Output Timing



Mission Mode: (TMS = 0, TIS = 0)

FIGURE 4. Synchronous Single-Port SRAM Output-Enable Timing

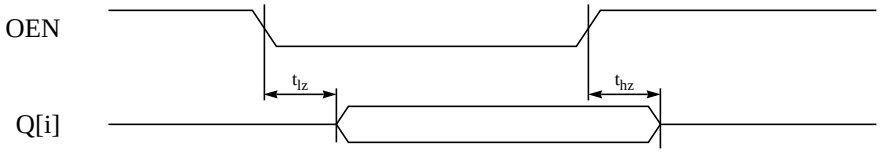


FIGURE 5. Synchronous Single-Port SRAM Test-Data Output-Enable Timing

FIGURE 6. Synchronous Single-Port SRAM Read-Cycle Timing (pipeline = off)

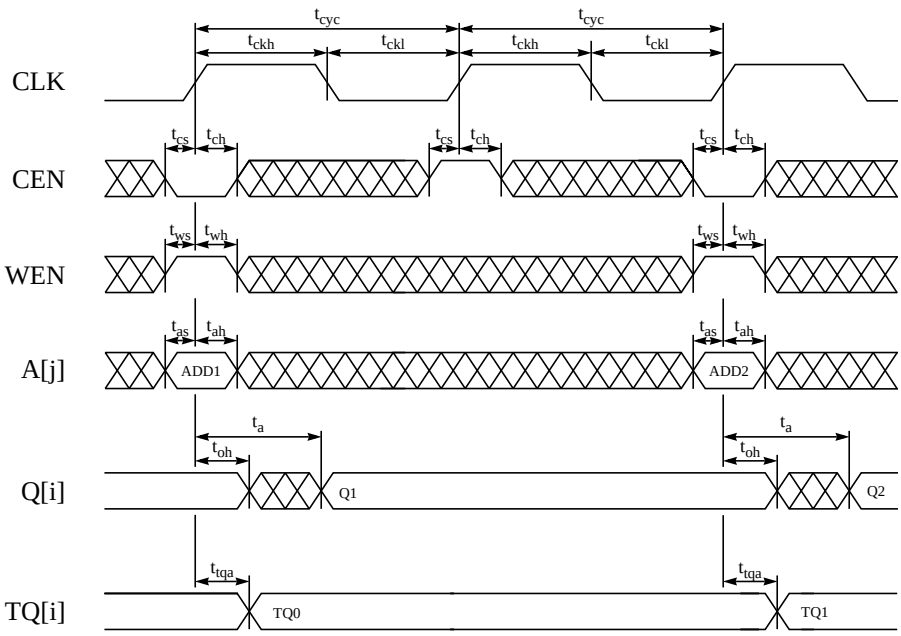


FIGURE 7. Synchronous Single-Port SRAM Write-Cycle Timing (pipeline = off)

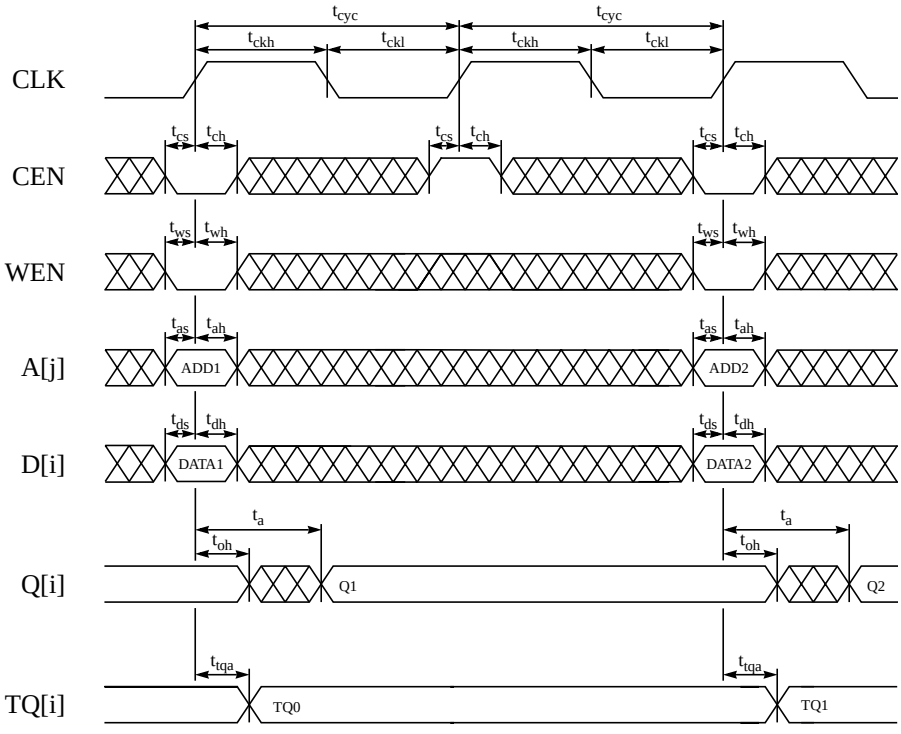


FIGURE 8. Synchronous Single-Port SRAM Read-Cycle Timing (pipeline = on) *[Not applicable for this configuration]*

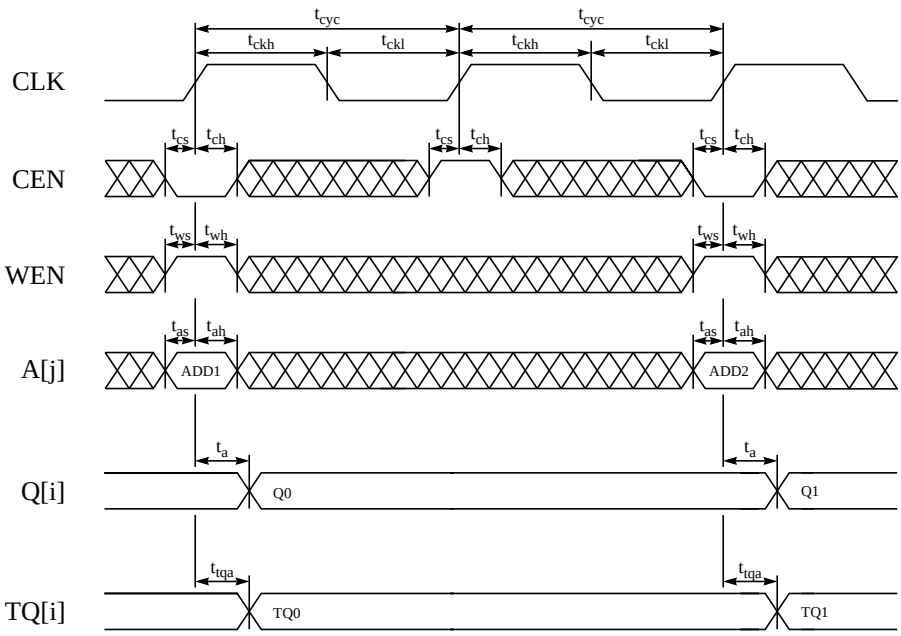
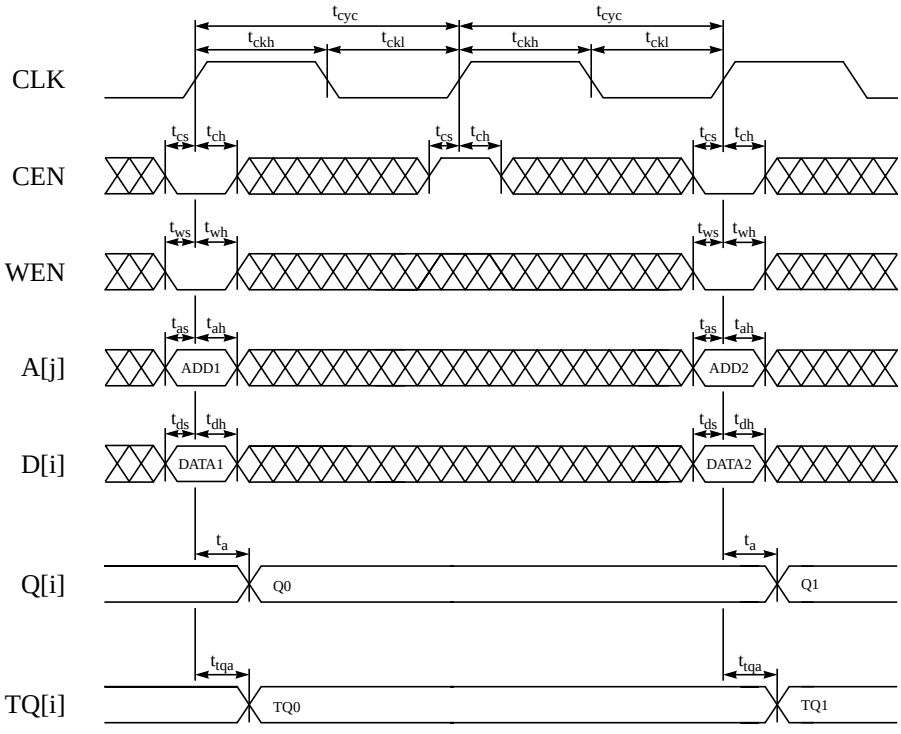


FIGURE 9. Synchronous Single-Port SRAM Write-Cycle Timing (pipeline = on) *[Not applicable for this configuration]*



Parallel Test Mode (TMS = 0, TIS = 1)

FIGURE 10. Synchronous Single-Port SRAM Test Output-Enable Timing

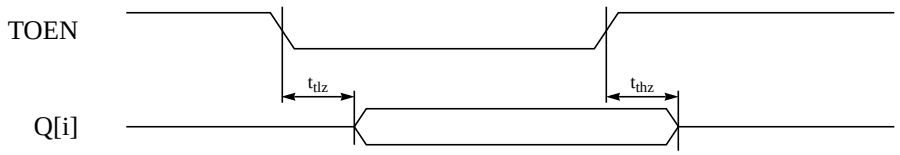


FIGURE 11. Synchronous Single-Port SRAM Test-Data Output-Enable Timing

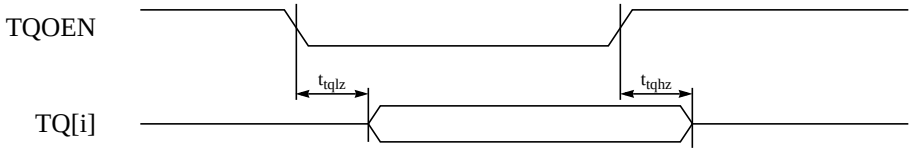


FIGURE 12. Synchronous Single-Port SRAM Test Read-Cycle Timing (pipeline = off)

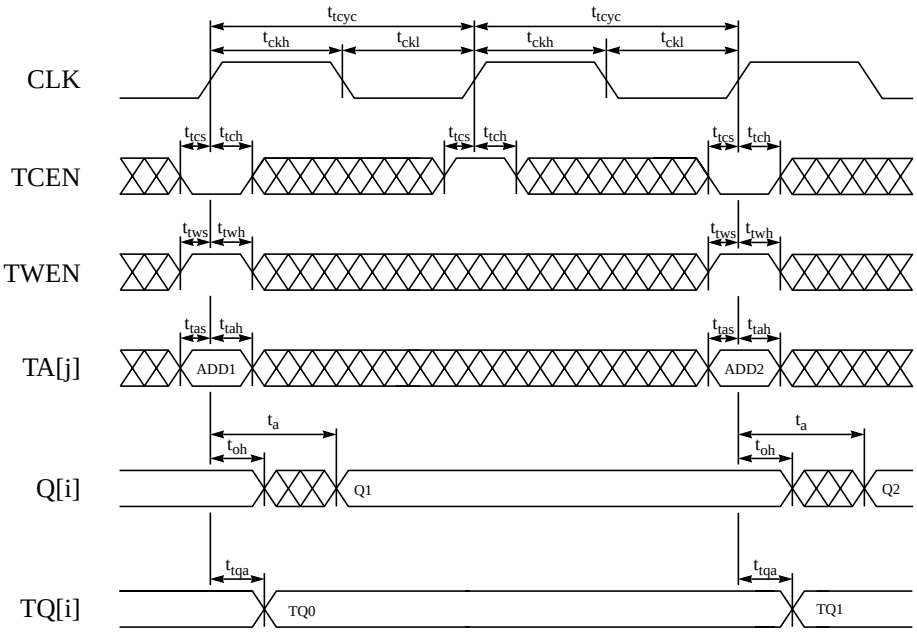


FIGURE 13. Synchronous Single-Port SRAM Test Write-Cycle Timing (pipeline = off)

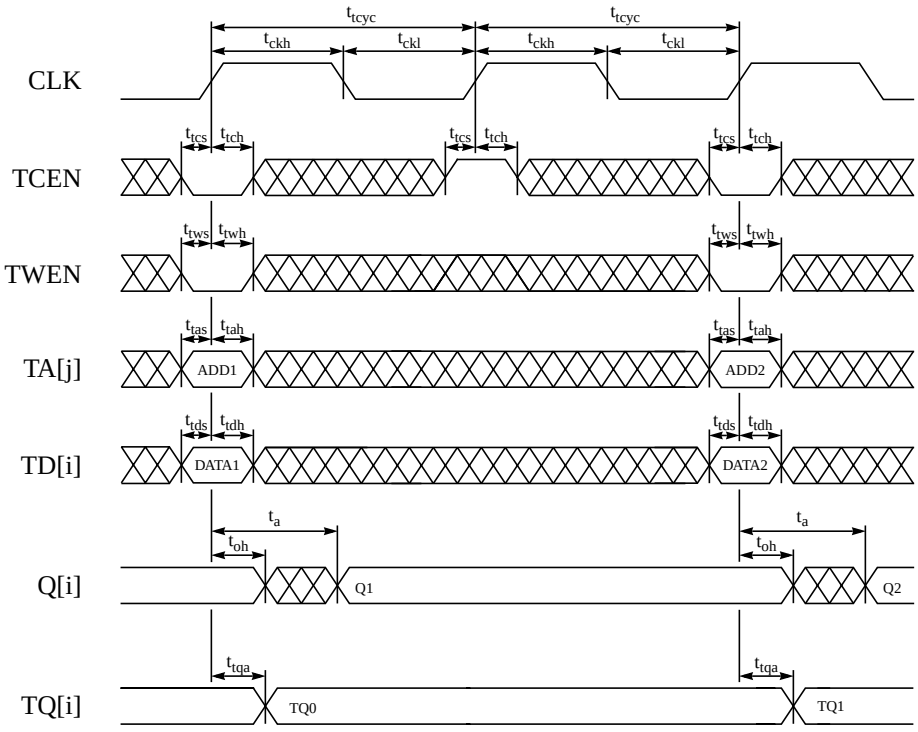


FIGURE 14. Synchronous Single-Port SRAM Test Read-Cycle Timing (pipeline = on) *[Not applicable for this configuration]*

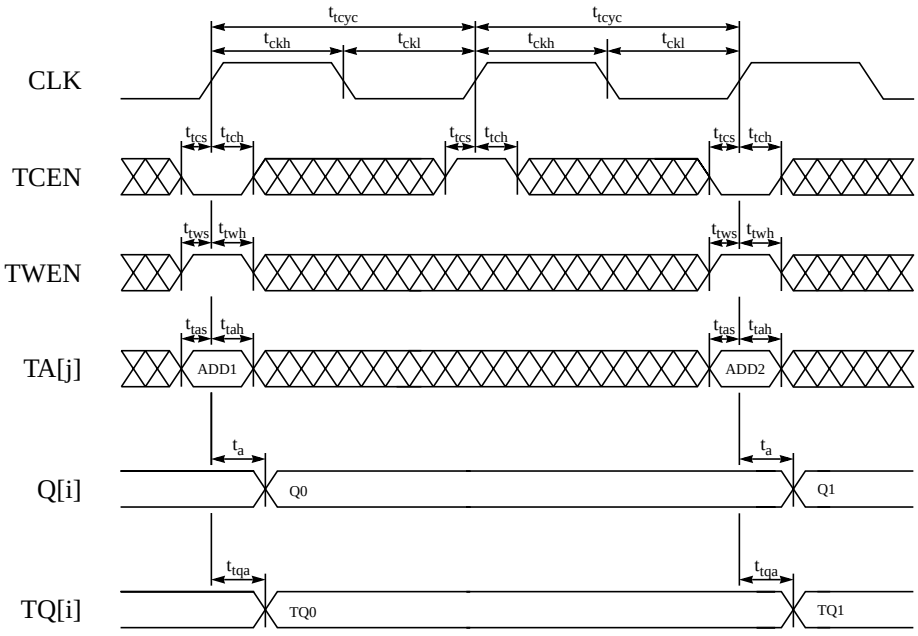
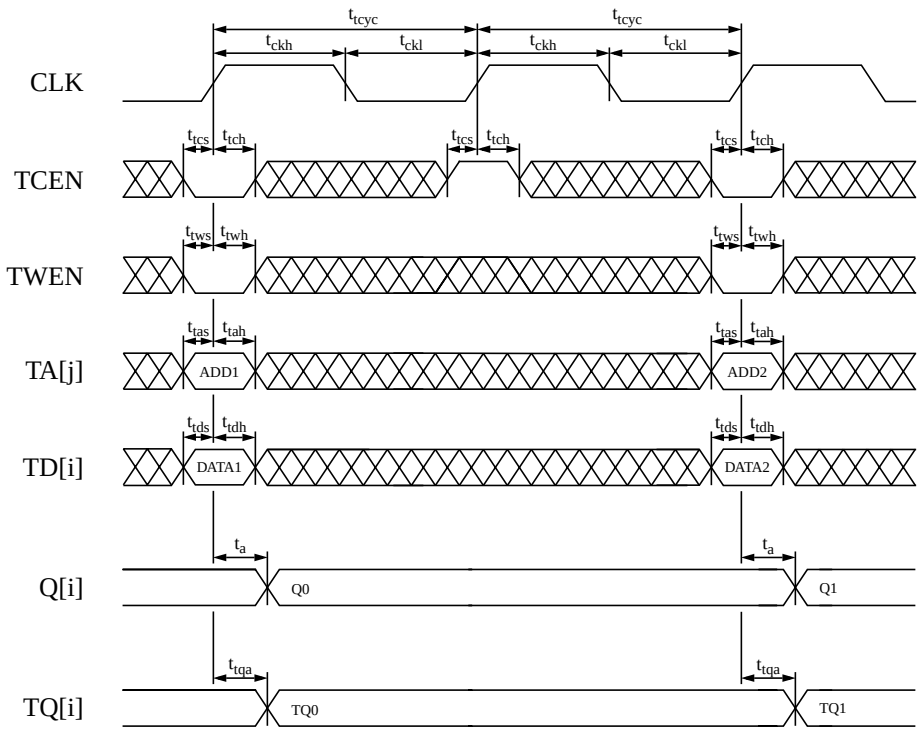


FIGURE 15. Synchronous Single-Port SRAM Test Write-Cycle Timing (pipeline = on) *[Not applicable for this configuration]*



Functional Data Scan Mode (TMS = 1, TIS = 0)

FIGURE 16. Synchronous Single-Port SRAM Output-Enable Timing

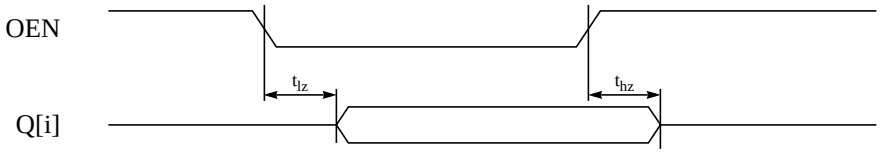


FIGURE 17. Synchronous Single-Port SRAM Test-Data Output-Enable Timing

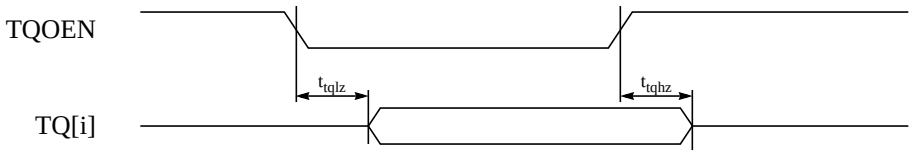
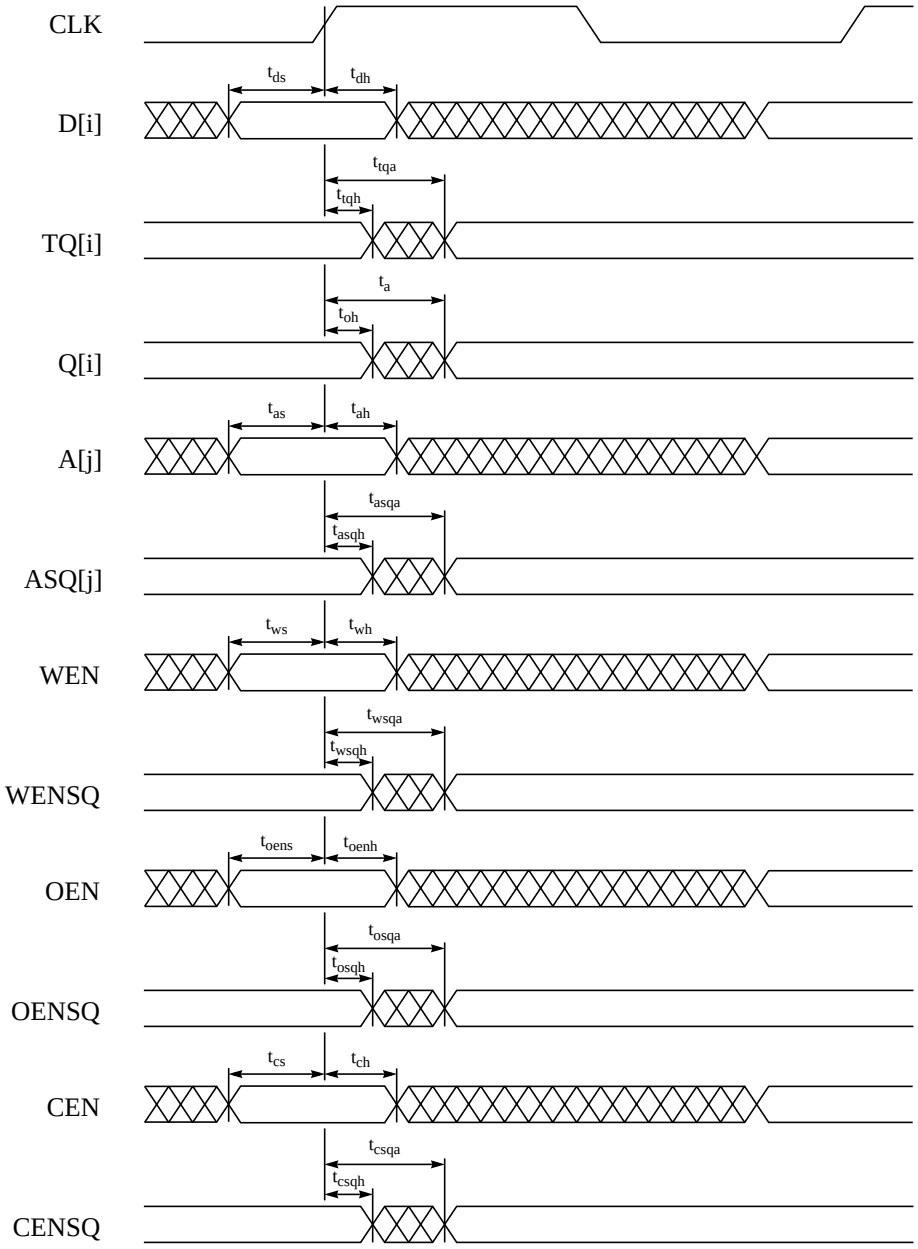


FIGURE 18. Synchronous Single-Port SRAM UTI Latch Timing



Test Data Scan Mode (TMS = 1, TIS = 1)

FIGURE 19. Synchronous Single-Port SRAM Test Output-Enable Timing

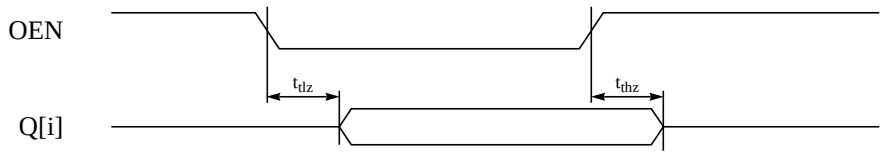


FIGURE 20. Synchronous Single-Port SRAM Test-Data Output-Enable Timing

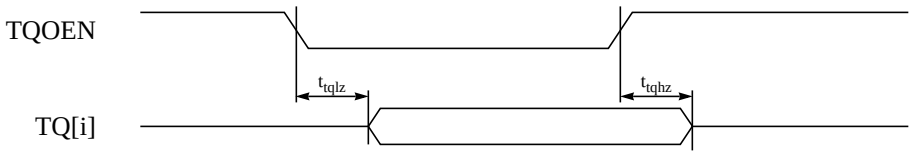
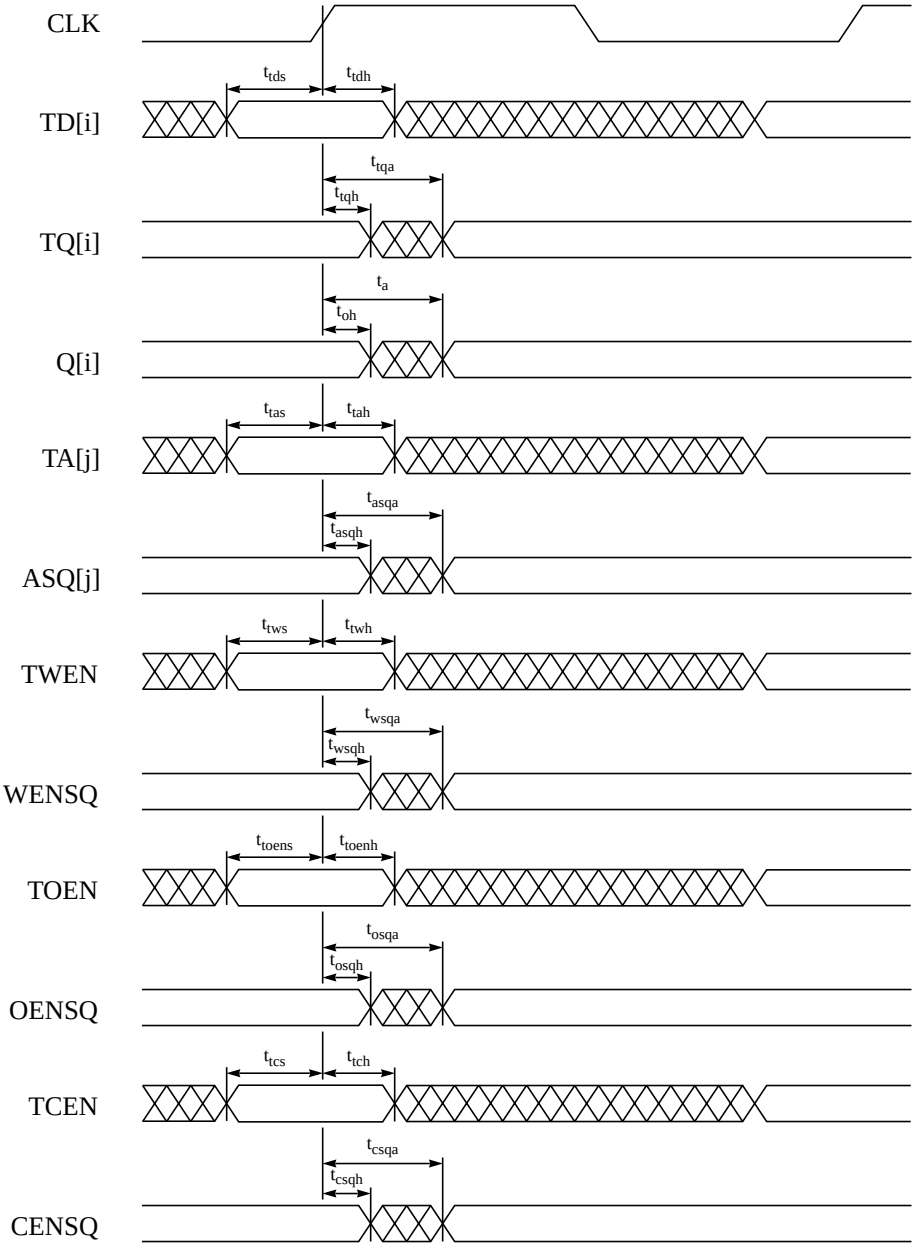


FIGURE 21. Synchronous Single-Port SRAM UTI Latch Timing



SRAM Timing: UTI Test Modes

Test Control Signal Timing

Typical Process, 2.50 Volts, 25˚C

Parameter	Symbol	Min (ns)	Max (ns)	Parameter	Symbol	Min (ns)	Max (ns)
Test input select setup	t_{tiss}	1.17		Test-mode select setup	t_{tmss}	0.62	
Test input select hold	t_{tish}	0.52		Test-mode select hold	t_{tmsh}	0.04	

Test Input Timing

Typical Process, 2.50 Volts, 25˚C

Parameter	Symbol	Min (ns)	Max (ns)	Parameter	Symbol	Min (ns)	Max (ns)
Test address setup	t_{tas}	0.67		Test write enable hold	t_{twh}	0.00	
Test address hold	t_{tah}	0.00		Test data setup	t_{tds}	0.59	
Test chip enable setup	t_{tcs}	0.62		Test data hold	t_{tdh}	0.00	
Test chip enable hold	t_{tch}	0.00		Test output enable to hi-Z	t_{thz}		1.06
Test write enable setup	t_{tws}	0.88		Test output enable active*	t_{tlz}		1.18

* Parameter has a load dependence: K_{load} = 1.46ns/pF

Test Data Output Timing

Typical Process, 2.50 Volts, 25˚C

Parameter	Symbol	Min (ns)	Max (ns)	Parameter	Symbol	Min (ns)	Max (ns)
Test data output access*	t_{tqa}	1.36		Test-mode select active	t_{tmslz}		1.16
Test input select to hi-Z	t_{tishz}		1.29	Test data output drive enable to hi-Z	t_{tqhz}		0.47
Test input select active	t_{tislz}		1.47	Test data output drive enable active*	t_{tqlz}		0.52
Test-mode select to hi-Z	t_{tmshz}		1.04				

* Parameter has a load dependence: K_{load} = 1.32ns/pF

UTI Latch Timing

Typical Process, 2.50 Volts, 25˚C

Parameter	Symbol	Min (ns)	Max (ns)	Parameter	Symbol	Min (ns)	Max (ns)
Scan register address access*	t_{asqa}	0.89		Scan register output enable access*	t_{osqa}	0.86	
Scan register address hold	t_{asqh}	0.74		Scan register output enable hold	t_{osqh}	0.70	
Scan register chip enable access*	t_{csqa}	0.85		UTI latch output enable setup	t_{oens}	0.31	
Scan register chip enable hold	t_{csqh}	0.69		UTI latch output enable hold	t_{oenh}	0.00	
Scan register write enable access*	t_{wsqa}	0.85		UTI latch test-mode output enable setup	t_{toens}	0.37	
Scan register write enable hold	t_{wsqh}	0.69		UTI latch test-mode output enable hold	t_{toenh}	0.04	

* Parameter has a load dependence: K_{load} = 2.32ns/pF

SRAM Logic Table

CEN	WEN	OEN	Data Out	Mode	Function
H	X	L	Last Data	Standby	Address inputs are disabled; data stored in the memory is retained, but the memory cannot be accessed for new reads or writes. Data outputs remain stable.
L	L	L	Data In	Write	Data on the data input bus D[n-1:0] is written to the memory location specified on the address bus A[m-1:0], and driven through to the data output bus Q[n-1:0].
L	H	L	SRAM Data	Read	Data on the data output bus Q[n-1:0] is read from the memory location specified on the address bus A[m-1:0].
X	X	H	Z	High-Z	The data output bus Q[n-1:0] is placed in a high impedance state. Other memory operations are unaffected.

During normal read and write operations, the signals TMS and TIS must be low.

Pin Capacitance

Typical Process, 2.50 Volts, 25˚C

Pin	Value (pF)
A[j:0]	0.090
D[i:0]	0.022
CLK	0.405
CEN	0.048
WEN	0.061
OEN	0.050
Q[i:0]	0.027
TA[j:0]	0.070
TD[i:0]	0.018
TCEN	0.036
TWEN	0.049
TOEN	0.027
TQOEN	0.085
TIS	0.230
TMS	0.389
TQ[i:0]	0.011

Area

Height (μm)	Width (μm)	Area (mm^2)
860.50	723.10	0.62

Height, width and area include ring size = 105μm

Power

Typical Process, 2.50 Volts, 25˚C, 100.00MHz Operation

Condition	Value (mA)
AC Current[1]	24.84
Read AC Current	22.91
Write AC Current	26.77
Peak Current	445.46
Deselected Current[2]	7.75
Standby Current[3]	leakage only

[1] Value assumes 50% read and write operations

[2] Value assumes SRAM is deselected, CLK switches, and half of data and address inputs switch

[3] Value assumes SRAM is deselected and only CLK switches

Power and Ground Noise Limit

Typical Process, 2.50 Volts, 25˚C

Signal	Interval	Voltage (V)
Power	memory cycle	0.50
Ground	memory cycle	0.50

The power/ground noise limit is the maximum supply voltage transition allowable within a memory cycle without causing a memory failure

Clock Noise Limit

Typical Process, 2.50 Volts, 25˚C

Signal	Pulse Width (ns)	Voltage (V)
CLK	10.00	1.13

The clock noise limit is the maximum CLK voltage allowable for the indicated pulse width without causing a spurious memory cycle or other memory failure