National Semiconductor

PRELIMINARY
June 1995

DP83957 10 Mb/s Repeater Information Base

General Description

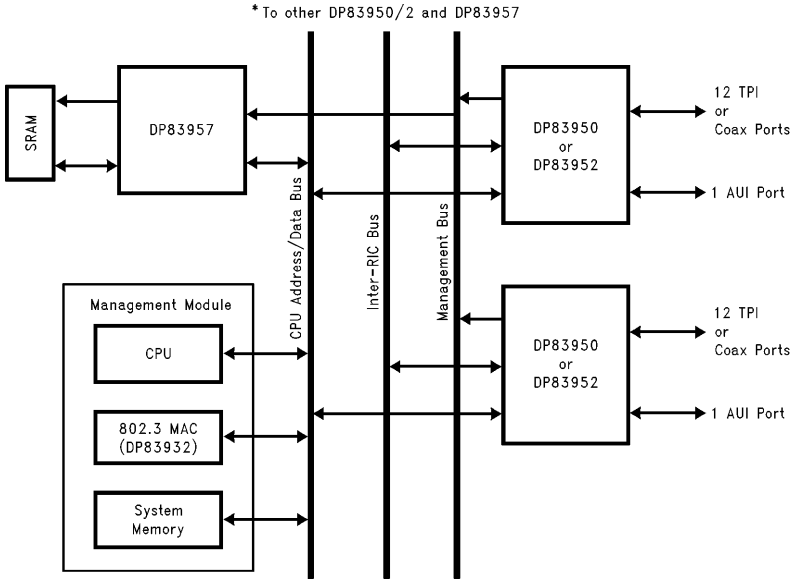
The DP83957 Repeater Information Base ''RIB'' allows effective implementation of managed multi-port 10 Mb/s ethernet repeater hubs. The device supports all the necessary Port Attributes for the IEEE 802.3k standard (Layer Management for 10 Mb/s Baseband Repeaters). This device is designed to be interfaced with Repeater Interface Controllers (DP83950/2) and gathers attributes on a per-port, per-packet basis.

The DP83957 collects management attributes via the DP83950/2 Management Bus and stores this information in an external SRAM. The DP83957 can be programmed to collect information for up to two DP83950/2 on a shared Management Bus. It can also be used in a dedicated one DP83957 per DP83950/2 architecture. The attributes stored in external SRAM can be easily accessed through the DP83957 by an 8-bit multiplexed Address/Data bus.

Features

- Fully IEEE 802.3K-July 1992 compatible
- Supports up to two DP83950/2
- Supports generic 1k x 8 or 2k x 8 SRAMs with variable access times of up to 45 ns
- Guarantees at least one attribute access by the microprocessor in the busiest network scenario
- Pipelined architecture for processing back to back frames
- Supports maskable interrupts for status and error reporting on a shared interrupt pin
- Detection and notification of DP83950 Management Bus errors
- Detection and notification of overflow of attribute counters
- 80-pin PQFP package

1.0 System Diagram

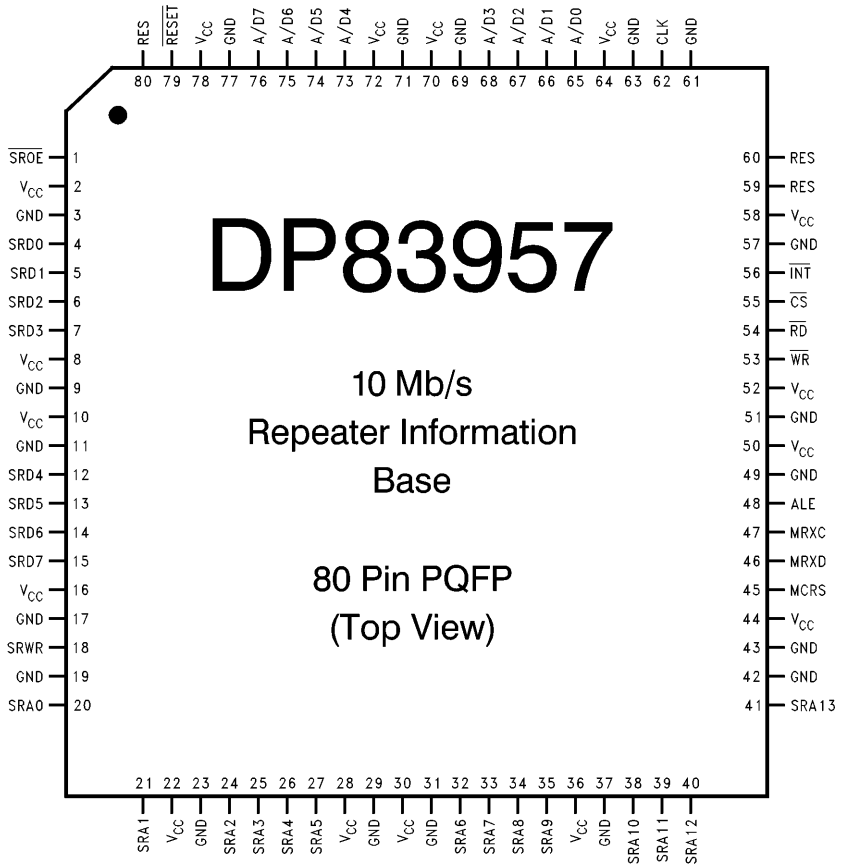


TL/F/12437–1

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Table of Contents

2.0 Pin Connection Diagram



TL/F/12437–3

3.0 Pin Description

3.1 CPU INTERFACE

The CPU interface is a generic 8-bit multiplexed Address/Data bus. The asynchronous interface requires minimum glue logic.

Signal Name	Type	Active	Description
$\overline{CS}$	O/C	Low	**CHIP SELECT:** The Chip Select is generated by the system to select the DP83957 registers. Chip Select must remain valid for the entire cycle.
$\overline{RD}$	O/C	Low	**READ:** Read Data Strobe. The system asserts this pin low to read the DP83957 registers.
$\overline{WR}$	O/C	Low	**WRITE:** Write Data Strobe. The system asserts this pin low to write to the DP83957 registers.
ALE	I/C	High	**ALE:** Address Latch Enable. The system needs to drive this to inform the DP83957 that there is a valid address on the Address/Data bus.
$\overline{INT}$	O/Z/C	Low	**INTERRUPT:** Indicates that an interrupt (if enabled) is pending from one of the sources set in the Interrupt Status Register.
A/D[7:0]	O/I/Z/C	—	**ADDRESS/DATA BUS:** 8-bit multiplexed CPU address/data bus.

3.2 SRAM INTERFACE

The SRAM interface is used to connect the DP83957 to an external SRAM. The DP83957 supports either a 1k x 8 or 2k x 8-bit SRAM. The SRAM interface can support SRAM access times of 25 ns and 45 ns.

Signal Name	Type	Active	Description
SRD[7:0]	O/I/Z		**SRAM DATA BUS:** This data bus should be connected directly to the external SRAM.
SRA[13:0]	O/C	—	**SRAM ADDRESS BUS:** This address bus should be connected directly to a 1k x 8 or 2k x 8 SRAM Address inputs.
SRW	I/C	—	**SRAM READ-WRITE:** A high level signal indicates a Read and a low level signals indicates a Write cycle.
$\overline{SROE}$	I/C	Low	**SRAM OUTPUT ENABLE:** This should be connected directly to the external SRAM output enable.

3.0 Pin Description (Continued)

3.3 MANAGEMENT BUS INTERFACE

The Management Bus Interface provides the input to the DP83957 from the DP83950 or the DP83952. The Management Bus connects directly to the DP83950 or DP83952 or through buffers depending on the repeater design (refer to the DP83950 data sheet).

The Management Bus is a NRZ bus that provides the necessary information to the DP83957 so that it can assemble port attributes on a per-port, per-packet basis.

Signal Name	Type	Active	Description
MRXC	I/C	—	**MANAGEMENT RECEIVE CLOCK:** When asserted this signal provides a clock signal for the MRXD serial data stream. The MRXD signal is changed on the falling edge of this clock.
MRXD	I/C	—	**MANAGEMENT RECEIVE DATA:** When asserted this signal provides a serial data stream in NRZ format. The data stream is made up of the packet data and DP83950/2 status information.
MCRS	I/C	High or Low (Selectable)	**MANAGEMENT CARRIER SENSE:** When asserted this signal provides an activity framing enable for the serial output data stream (MRXD).

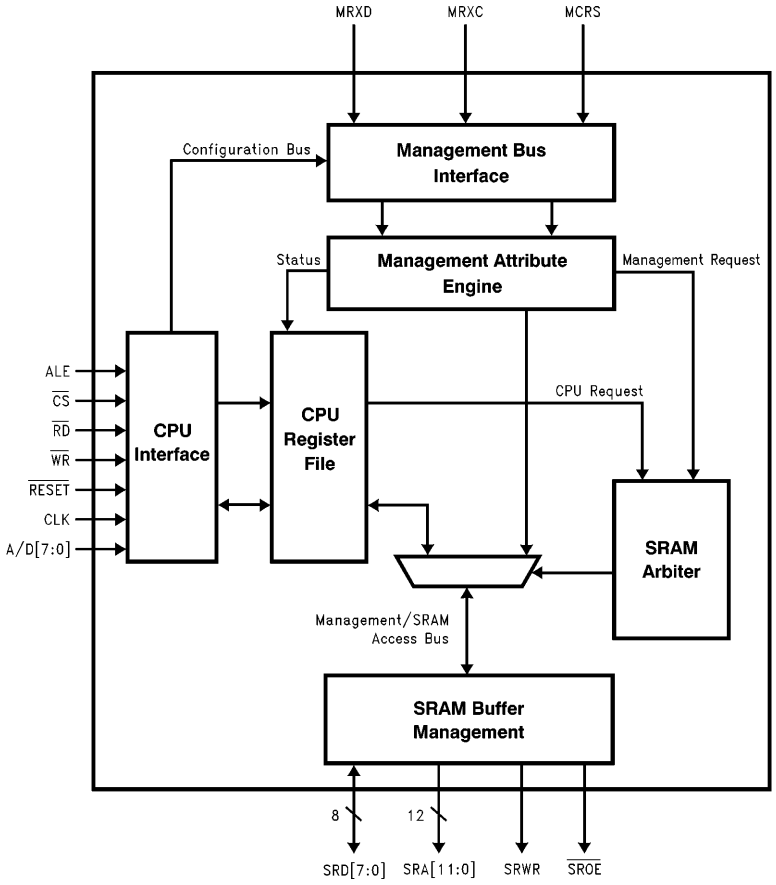
3.4 MISCELLANEOUS PINS

Signal Name	Type	Active	Description
CLK	I/C	—	**CLOCK:** 40 MHz clock for the internal state machines. This clock does not influence the asynchronous CPU Interface. This clock can be obtained directly from the DP83950/2.
$\overline{\text{RESET}}$	I/C	Low	**RESET:** The DP83957 is reset when this signal is asserted low. Asserting this signal will cause all the state machines and registers to enter their reset state.
RES	—	—	**RESERVED:** Leave as No Connect.
V_{CC}	I	—	**V_{CC}:** +5V supply.
GND	I	—	**GND:** Ground return.

3.5 PIN TYPE DESIGNATION

Type	Description
I	Input Buffer
O	Output
Z	High Impedance State
I/O/Z	Bi-directional buffer with high impedance capability
C	CMOS input or output

4.0 Block Diagram



TL/F/12437–2

5.0 Functional Description

This section describes the three major blocks of the DP83957. These are the:

1) SRAM Interface
2) Management Interface
3) CPU Interface

5.1 SRAM INTERFACE

The DP83957 interfaces directly with standard, off-the-shelf, 1k x 8 or 2k x 8 fast SRAM without any additional buffering. The DP83957 can support access times of 25 ns and 45 ns.

If one DP83950/2 is used, then a minimum 1k x 8 SRAM is required.

If two DP83950/2's are used (on a shared management bus), then a minimum 2k x 8 SRAM is required.

The SRAM connected to the DP83957 stores the Management Information Base (MIB) attributes that are extracted from the DP83950's management bus.

The SRAM Interface consists of the following pins:

SRA[13:0]	14-Bit Address Lines
SRD[7:0]	8-Bit Data Bus
SRWR	Write Enable
SROE	Output Enable

The SRAM interface does not include a chip select output to enable the SRAM, as the SRAM is dedicated to the DP83957. Therefore, the SRAM's chip select input must always be enabled.

5.1.1 SRAM Configuration

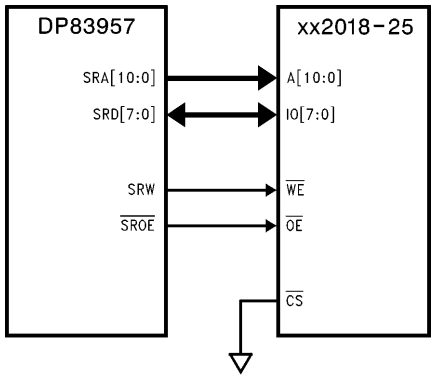
The DP83957 must be configured correctly to allow it to interface with the SRAM. This is achieved through Configuration Registers 1 and 2 (refer to Sections 6.2 and 6.3 for a description of these registers).

The access time of the SRAM can be specified through the SRAM__ACC bit (D4) of Configuration Register 2.

If bit D4 = 0 then a SRAM access time of 25 ns is selected. If bit D4 = 1 then an access time of between 25 ns and 45 ns is selected.

The size of the SRAM must also be specified through the SIZE bit (D3) of Configuration Register 2. If bit D3 = 0, then a 1k x 8 is selected. If bit D3 = 1, then a 2k x 8 is selected.

The following diagram shows the external SRAM connection to the DP83957.



TL/F/12437–4

External SRAM Connection to DP83957

5.1.2 SRAM Read Operation

A read of the SRAM can occur due to a CPU request for one of the PORT attributes, or due to normal updating of attributes by the DP83957 after receiving the management statistics from the DP83950.

In the latter case, the access to the SRAM is achieved automatically by the DP83957. In the case of a CPU request, the SRAM address must be specified in Access Registers 1 and 2 (refer to Sections 6.8 and 6.9).

The REP__SEL bit (D4) of Access Register 2, specifies the DP83950 ID, and the PORT__ID bits (D[3:0]) specify the PORT ID. Together they select the SRAM page. The offset within the page, i.e. the attributes, is specified through Access Register 1. The ACC__I[5:0] bits (D[5:0]) specify the attribute (offset) to be read (Refer to Section 5.1.5, SRAM Address Format).

The DP83957 can read data from the SRAM in variable byte lengths. The number of bytes to be read is specified through bits D[0:2] of Configuration Register 1. The DP83957 can read up to 6 bytes from the SRAM at any one time. The data that is read from the SRAM is placed in Read Data Registers 1–6.

The CPU initiates an SRAM read by setting the ST-RD bit (D4) of Configuration Register 1. The DP83957 resets this bit after the read has completed. It also indicates completion of the SRAM read operation by sending an interrupt (if enabled) to the CPU and setting RD__COM bit (D4) of the Interrupt Status Register.

5.0 Functional Description (Continued)

5.1.3 SRAM Write Operation

A write to the SRAM can occur due to a CPU request to one or all of the MIB attributes, or due to normal updating of attributes by the DP83957 after receiving the management status bytes from a DP83950.

In the latter case, the access to the SRAM is done automatically by the DP83957. In the case of a CPU request, the SRAM address must be specified in the same manner as the read operation (refer to Section 5.1.2).

The DP83957 can write data to the SRAM one byte at a time, or it can fill the entire SRAM with the same value. The value to be written into the SRAM is specified in the Write Data Byte register.

The CPU initiates a one-byte SRAM write by setting the ST__WR bit (D5) in Configuration Register 1.

In order to fill the entire SRAM, both the FILL (D3) and the ST__WR (D5) bits must be set in Configuration Register 1.

This fill-mode is used to initialize the SRAM to a common value. For example, reset all the attributes to zero.

The DP83957 indicates the completion of the SRAM write operation by sending an interrupt (if enabled) to the CPU and setting the WR__COM bit (D5) in the Interrupt Status Register.

5.1.4 SRAM Memory Map

The memory map for the DP83957 consists of two sections. Each section represents one DP83950 device, as shown in the SRAM Memory Map.

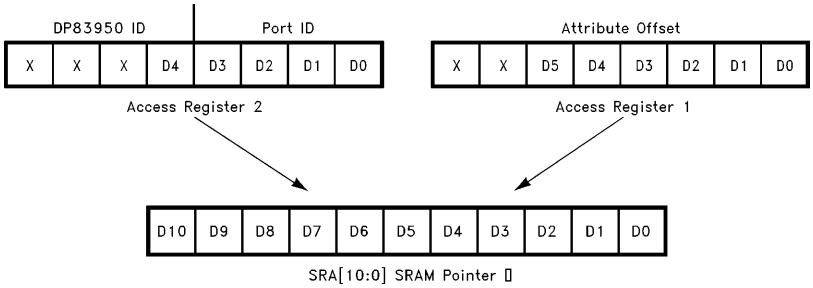
For each DP83950, the map is further divided into 13 pages; where each page represents a physical port for the DP83950. The DP83950 ID and Port number selection is programmed into Access 2 Register.

Each port page is further sub-divided into 64 locations. These locations represent the offset of the Port's Attributes. This offset is programmed into Access 1 Register.

5.1.5 SRAM Address Format

The SRAM SRA[10:0] address is made up by combining the contents of Access Registers 1 and 2. This is shown in the SRAM Address Pointer figure below.

SRAM Address Pointer



TL/F/12437–5

5.0 Functional Description (Continued)

SRAM MEMORY MAP

DP83950 Number	Port Number	11-Bit Address
DP83950 ID 0	Port 0	0x000
	Port 1	0x040
	Port 2	0x080
	Port 3	0x0C0
	Port 4	0x100
	Port 5	0x140
	Port 6	0x180
	Port 7	0x1C0
	Port 8	0x200
	Port 9	0x240
	Port 10	0x280
	Port 11	0x2C0
	Port 12	0x300
	Reserved	0x340-3FF
DP83950 ID 1	Port 0	0x400
	Port 1	0x440
	Port 2	0x480
	Port 3	0x4C0
	Port 4	0x500
	Port 5	0x540
	Port 6	0x580
	Port 7	0x5C0
	Port 8	0x600
	Port 9	0x640
	Port 10	0x680
	Port 11	0x6C0
	Port 12	0x700

	Number	6-Bit Address
Port N	aReadableFrames	0x00
	aReadable Octets	0x04
	aFrameCheckSequenceErrors	0x08
	aAlignmentErrors	0x0C
	aFramesTooLong	0x10
	aShortEvents	0x14
	aRunts	0x18
	aCollisions	0x1C
	aLateEvents	0x20
	aVeryLongEvents	0x24
	aDataRateMismatches	0x28
	aLastSourceAddress	0x2C
	aSourceAddressChanges	0x32
	Port Attributes Status 1	0x36
	Port Attributes Status 2	0x37
	Reserved	0x38-3F

TL/F/12437–6

5.2 MANAGEMENT INTERFACE

The DP83957 interfaces with either one or two DP83950/2 devices to obtain the 7 bytes of network management statistics appended at the end of each packet on the management bus (refer to DP83950 data sheet).

The management interface consists of the Management Carrier Sense (MCRS), Management Receive Clock (MRXC), and the Management Data (MRXD) signals.

The management interface signals connect directly to the corresponding pins of the DP83950/2.

5.2.1 Management Configuration

The attached DP83950/2 devices can be programmed to have an active high or low Management Carrier Sense (MCRS) signal.

The MCRS__LEV bit (D0) of Configuration Register 3 is used to select the active level of the MRCS signal from the DP83950.

If bit D0 = 0, then an active low MCRS signal is selected. If bit D0 = 1, then an active high MCRS is selected.

The DP83952 can operate in a Secure or Non-Secure (DP83950) mode. When set in Secure mode, it is possible for the DP83952 to modify the 7 bytes of management.

To cater for this, the DP83957 must be programmed to accept the modified 7 bytes of management status.

The SECURE bit (D7) of Configuration Register 2 is used to specify the operating mode of the DP83952.

If bit D7 = 0, then non-secure mode is selected. If bit D7 = 1, then secure mode is selected.

5.0 Functional Description (Continued)

5.2.2 Management Bus Interface

The management interface of the DP83957 is responsible for receiving, storing, validating management data, generating all attribute data and updating the attributes stored in the SRAM via the SRAM interface.

The DP83957 receives the per-port statistics information through the management interface (from a DP83950/2) and extracts the attribute information by latching in the last 56 bits (7 bytes) of data. The 7 bytes of data are used to update the appropriate attributes for the specified port.

After the de-assertion of MCRS, the DP83957 generates all attribute information and performs a read-modify-write operation to update the attribute counters stored in the SRAM for the specified DP83950 ID and port ID.

5.2.3 Management Bus Processing

The CPU initiates management data bus processing by setting the START bit (D7) in Configuration Register 1.

During the processing of management bus information, one of three error conditions may occur. This error will generate an interrupt to the microprocessor, if the interrupt is enabled.

Three sources of error interrupts that can occur are:

Source Address Mismatch (SAM) Interrupt

If the last packet received on a particular port has a Source Address that differs from the aLastSourceAddress attribute for that port, then the SAM bit (D7) will be set in the Interrupt Status Register.

No Start Frame Delimiter (SFD__ERR) Interrupt

If no Start Frame Delimiter (SFD) is detected within the MCRS envelope (i.e. before the end of the packet) on the Management Bus, then the SFD__ERR bit (D6) will be set in the Interrupt Status Register.

The management status must contain a minimum of 56 bits.

Invalid Port ID (IPN) Interrupt

If the received management status bytes contain a valid DP83950 ID, but an invalid port ID (i.e. a Port ID normally greater than 13), then the IPN bit (D3) will be set in the Interrupt Status register.

5.2.4 Port Attributes

The DP83957 supports all the Port Attributes that are required to comply with the IEEE 802.3k-1992 Layer Management standard for 10 Mb/s Baseband Repeaters, with the exception of aPortID, aPortAdminState and aAutoPartition attributes.

The aPortID, aPortAdminState and the aAutoPartition attributes are controlled directly by the DP83950.

aPortID

Each unique Port ID can be obtained from the DP83950 ID and the individual Port number (0–13) for each DP83950 or it can be obtained indirectly from the DP83957. The Port ID must be kept in software.

aPortAdminState

This is used to disable or enable a port such that when it is in disable mode it cannot transmit or receive data. This function can be controlled through the DP83950 DISPT bit (D7) in the Port Real Time Status Register. It is not controlled by the DP83957.

aAutoPartitionState

This indicates the state of the auto partition state machine for a particular port (i.e. whether the port is currently partitioned or not). This state is obtained directly from the DP83950 PART bit (D3) in the Port Real Time Status Register. A software routine needs to poll the Port Status Register to keep the counter updated. This state is not controlled by the DP83957.

aReadableFrame

This represents the total number of frames received with a valid frame length. The DP83957 increments the counter by one for each frame whose octet count is greater than or equal to the minFrameSize (64 Bytes) and less than or equal to the maxFrameSize (1518 bytes) and for which FCSError and CollisionEvent are NOT asserted. This is a 32-bit counter.

aReadableOctets

This counter increments by the number of octets received by the specific port for each frame that has been determined to be a Readable frame. This is a 32-bit counter.

aFrameCheckSequenceErrors

This counts the number of frames detected on each port with an invalid frame check sequence. The counter increments by one for each frame with FCSError signal asserted and the Framing Error and CollisionEvent signals de-asserted, and for those frames with a valid FrameSize. This is a 32-bit counter.

aAlignmentError

This counts the number of frames detected on each port with a FCS error and a framing error. The counter increments by one for each frame where the FCSError and FramingError signals are asserted and CollisionEvent de-asserted. In addition to this, the OctetCount must be greater than or equal to the MinFrameSize and less than or equal to the maxFrameSize. This is a 32-bit counter.

aFramesTooLong

This counts the number of frames that exceed the maxFrameSize. The counter increments by one for each frame where OctetCount is greater than the maxSizeFrame and which does not have an Alignment or FCSError. This is a 32-bit counter.

aShortEvents

This counts the number of frames that has CarrierEvent with ActivityDuration less than the ShortEventMaxTime. The ShortEventMaxTime is greater than 74 bits but less than 82 bits. This is a 32-bit counter.

aRunts

This counter increments by one for each CarrierEvent with ActivityDuration greater than the ShortEventMaxTime (74–82 bits) but less than the validPacketMinTime (64 bytes) and with the CollisionEvent signal de-asserted. This is a 32-bit counter.

aCollisions

This counter increments by one for any CarrierEvent signal asserted on any port in which the CollisionEvent signal on this port is asserted.

Note: Since the DP83957 can only keep track of PortN, or the information regarding the repeated packet, this attribute should be kept in the Port-Event Counter of the DP83950/2. This is a 32-bit counter.

aLateEvents

This counter increments by one for each CarrierEvent in which the collision is detected after the LateEventThreshold (480–565 bit times) has been reached in each frame. This is a 32-bit counter.

aVeryLongEvents

This counter increments by one for each CarrierEvent whose ActivityDuration is greater than the MAU jabber lockup protection timer. This is a 32-bit counter.

aDataRateMismatches

This counter increments by one if the frequency or data rate of the received packet is detectably mismatched from the local transmit frequency. For this counter to increment the following conditions must apply; CollisionEvent is not asserted and the ActivityDuration is greater than the ValidPacketMinTime. This is a 32-bit counter.

aSourceAddressChange

This counter increments by one each time the Source Address field, of a ReadableFrame, differs from the previous received Source Address field on the same port. This is a 32-bit counter.

aLastSourceAddress

This attribute stores the SourceAddress value of the last ReadableFrame received by this port. This is a 48-bit buffer.

5.2.5 Port Attribute Status

Port Attribute Status Registers 1 and 2 provide a snap-shot of changes to a ports attribute(s) since the last CPU Read access.

These two registers minimize the number of CPU access needed to obtain the Port's attributes stored in the SRAM. They allow the microprocessor to read only those attributes that have been updated since the last CPU access, instead of reading every attribute for a particular port.

The CPU needs to clear the Port Attribute Status bits after a read to these locations to guarantee that it has taken a snap shot of the Port Attribute changes correctly.

Any subsequent updates to any of the attributes by the DP83957 management block will always set the appropriate bits of the Port Attribute Status octets (refer to Sections 6.16 and 6.17).

5.2.6 Port Attribute Overflow

The attribute overflow condition is an important feature as it can be used to monitor the frequency of occurrence of a specific attribute. This feature is intended to allow software to set thresholds for an appropriate attribute and monitor the frequency of the overflow condition.

An attribute overflow occurs when the attribute counter rolls over from 0xFF to 0x00. This condition is indicated by the OVFL bit (D2) in the Interrupt Status Register. The attribute for which the counter has overflowed is specified in the Overflow Status Register 2 (refer to Section 6.14 for the bit definitions).

The DP83950 ID and Port ID associated with the overflow condition is specified in Overflow Status Register 1 (refer to Section 6.13).

5.0 Functional Description (Continued)

5.3 CPU INTERFACE

This interface allows the CPU to read and write to all of the DP83957's registers and to indirectly access the Port attributes stored in the SRAM (via the DP83957). All read and write accesses are byte wide. The DP83857 operates as a slave device and requires a minimum amount of glue logic to interface with the CPU.

All timing requirements as specified in Section 8.0 (AC Timing Conditions) must be satisfied for proper operation.

The CPU interface consists of a multiplexed Address/Data bus (A/D[7:0]), Chip Select ($\overline{CS}$), Read enable ($\overline{RD}$), Write enable ($\overline{WR}$), Address Latch Enable (ALE), and Interrupt ($\overline{INT}$) signals.

5.3.1 Register Read Operation

A read to one of the DP83957 registers is initiated by the CPU logic asserting $\overline{CS}$. The address (of the desired register) is driven onto the A/D[7:0] bus by the CPU and must be stable before the falling edge of ALE. After the T5 time has elapsed, the $\overline{RD}$ signal can be asserted which switches the direction of the A/D[7:0] bus (to output).

The data driven out onto the A/D[7:0] bus by the DP83957 will not be valid until the T7 time has elapsed. At this point, the A/D bus will display the contents of the desired register (refer to Section 8.1, CPU Read Timing Diagrams).

5.3.2 Register Write Operation

A write to one of the DP83957 registers is initiated by the CPU logic asserting $\overline{CS}$. The address (of the desired register) is driven onto the A/D[7:0] bus by the CPU and must be stable before the falling edge of ALE. The data that is written to the DP83957 must be stable before the de-assertion (rising edge) of $\overline{WR}$ (refer to Section 8.2, CPU Write Timing Diagrams).

5.3.3 Interrupts

The INT is an active low signal driven by the DP83957 to indicate that an interrupt has been generated.

The INT signal is shared between the maskable status interrupts and the error reporting interrupts.

The source of the interrupt can be determined by reading the Interrupt Status Register (refer to Section 6.7 for the bit definition).

The CPU clears the generated interrupt by writing a ''1'' to that bit in the Interrupt Status Register. Writing a ''0'' to a bit has no effect.

The following events can cause the DP83957 to drive the INT pin low:

— Source Address Mismatch (SAM)

— Management Bus Error (SFD_ERR or $<$56 bits)

— SRAM Write complete (WR_COM)

— SRAM Read Complete (RD_COM)

— Invalid Port Number Received (IPN)

— Attribute Overflow (OVFL)

Any of the above events can be masked by setting the corresponding bit in the Interrupt Mask Register (refer to Section 6.5 for the bit definition).

The INT output pin can be disabled (TRI-STATE®) by setting the INT bit D6 in Configuration Register 1.

5.4 REGISTERS

The DP83957 has 18 registers that are used to control the operation of the DP83957 and obtain the attribute information stored in the SRAM. The following section provides a brief description of these registers. Refer to Section 6.0, DP83957 Register Description, for a more detailed explanation.

Configuration Registers 1–3

These registers are used to control and configure the DP83957.

Interrupt Mask Register

This register specifies the events that can cause the INT pin to be driven active by the DP83957.

Interrupt Status Register

This register specifies the source (event) that caused the INT pin to be driven by the DP83957. The bit(s) can be cleared by writing a ''1''.

Read Data Registers 1–6

When the CPU requests a SRAM read of an attribute, the DP83957 transfers the data obtained from the SRAM into these holding registers.

Access Registers 1–2

Access Registers 1 and 2 specify the address for the SRAM read and write operation. The address consists of a page (DP83950/2 ID and Port ID) and offset (Port attribute).

Write Data Byte Register

This register contains the value to be written to a SRAM location during a write operation or during a SRAM fill operation.

DP83950 or DP83952 ID Registers 1–2

These registers contain the DP83950/2 ID of the DP83950/2's that are dedicated to this DP83957.

Overflow Status Registers 1–2

Overflow Status Registers 1 and 2 contain indirectly the DP83950 ID, the actual Port ID, and the attribute whose counter has rolled over from 0xFF to 0x00.

6.0 Register Description

The DP83957 has 18 registers which are addressed in a linear fashion. The Reserved Registers should not be accessed. The register map is given in Section 6.1, followed by a detailed description of each register in Sections 6.2 to 6.17.

6.1 REGISTER MAP

Address (Hex)	Register Name	Access
00	Configuration Register 1	Read/Write
01	Configuration Register 2	Read/Write
02	Configuration Register 3	Read/Write
03	Interrupt Mask	Read/Write
04	Interrupt Status	Read/Write
05–0F	Reserved	—
10	Read Data Byte 1	Read
11	Read Data Byte 2	Read
12	Read Data Byte 3	Read
13	Read Data Byte 4	Read
14	Read Data Byte 5	Read
15	Read Data Byte 6	Read
16–1F	Reserved	—
20	Port Access Register 1	Read/Write
21	DP83950 Access Register 2	Read/Write
22	Write Data Byte	Read/Write
23–2F	Reserved	—
30	DP83950 ID 1	Read/Write
31	DP83950 ID 2	Read/Write
32–3F	Reserved	—
40	Overflow Status Register 1	Read
41	Overflow Status Register 2	Read
42–4F	Reserved	—
50	DP83957 Revision Register	Read
51	Reserved	—

6.0 Register Description (Continued)

6.2 CONFIGURATION REGISTER 1

Configuration Register 1 provides the control to the microprocessor to allow the processor to read and write information into the external SRAM.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7	START	R/W	Setting this bit to a 1 will enable the DP83957 to start processing Port Attributes.
D6	INT	R/W	This bit enables/disables the Interrupt pin. When disabled the output is in place in TRI-STATE. 0: Enable Interrupt 1: Disable Interrupt
D5	ST__WR	R/W	By writing a 1 to this bit will allow the CPU to initiate a SRAM write. The DP83957 will reset this bit to 0 when it has completed a SRAM write.
D4	ST__RD	R/W	By writing a 1 to this bit will allow the CPU to initiate a SRAM read. The DP83957 will reset this bit to 0 when it has completed a SRAM read.
D3	FILL	R/W	Setting this bit to a 1 will fill the entire SRAM with the data pattern contained in the Write Data Byte Register (0x22).
D2–D0	RAC[2:0]	R/W	The CPU must write the number of bytes it needs to read from the SRAM into these 3 bits. The maximum number of bytes that can be read at any one time is 6. The number of bytes read from SRAM is buffered in the Read Data Byte Registers.

6.3 CONFIGURATION REGISTER 2

Configuration Register 2 sets up the DP83957 for different versions of the Repeater Interface Controller (DP83950 or the Secure DP83952) and different external SRAM parameters (i.e. access speeds and SRAM size).

This register must be set up during initialization.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7	SECURE	R/W	This bit selects between a Secure or a Non-Secure Repeater Interface Controller which is connected to the DP83957. 0: Selects the Non-Secure Mode 1: Selects the Secure Mode **Note:** This is only relevant for the DP83952. For the DP83950 this bit must be set to 0.
D6	CLR__ATR	R/W	An attribute will be reset to zero, after the attribute is read from SRAM, if this bit is set to 1.
D5	RES	R/W	This bit must always be set to 0.
D4	SRAM__ACC	R/W	This bit determines the access speed of the external SRAM. 0: Selects an access speed of up to 25 ns 1: Selects an access speed of up to 45 ns
D3	SIZE	R/W	This bit selects the size of the external SRAM. The size will depend on whether one or two DP83950's are connected to the DP83957. 0: Selects a 1024 byte SRAM 1: Selects a 2048 byte SRAM
D2–D0	RES	—	Reserved

6.4 CONFIGURATION REGISTER 3

Configuration Register 3 is used to set-up the Management Interface between the DP83950(s) and the DP83957. The Repeater Interface Controller (DP83950) allows the user to program the Management Carrier Sense (MCRS) signal to be either active high or active low depending on the particular repeater design.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7–D1	RES	—	Reserved.
D0	MCRS__LEV	—	This bit selects the active signal level of the Management Carrier Sense signal. 0: Active Low 1: Active High

6.0 Register Description (Continued)

6.5 INTERRUPT MASK REGISTER (0x03)

This register masks the interrupts that can be generated by the Interrupt Status Register. Writing a 1 to a bit disables the corresponding interrupt. During a hardware Reset all interrupts are enabled.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7	SAM	R/W	0: Enable Source Address Match Interrupt 1: Mask Source Address Match Interrupt
D6	SFD__ERR	R/W	0: Enable Management Bus Error Interrupt 1: Mask Management Bus Error Interrupt
D5	WR__COM	R/W	0: Enable SRAM Write complete Interrupt 1: Mask SRAM Write complete Interrupt
D4	RD__COM	R/W	0: Enable SRAM Read complete Interrupt 1: Mask SRAM Read complete Interrupt
D3	IPN	R/W	0: Enable Invalid Port Number Interrupt 1: Mask Invalid Port Number Interrupt
D2	OVRF	R/W	0: Enable Attribute Overflow Interrupt 1: Mask Attribute Overflow Interrupt
D2–D0	RES	—	Reserved

6.6 INTERRUPT STATUS REGISTER (0x04)

This register indicates the source of an interrupt when the INT pin goes active. Enabling the corresponding bit in the Interrupt Mask Register allows bits in this register to produce an interrupt. When an interrupt occurs, one or more bits in this register are set to a 1.

A specific interrupt is cleared by writing a 1 to the bit that corresponds to the interrupt. A particular interrupt is retained by writing a 0 to it.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7	SAM	R/W	Indicates that the last packet's Source Address did not match with the ports aLastSourceAddress attribute.
D6	SFD__ERR	R/W	Indicates that no SFD was detected within the MCRS envelope. The management status alone must contain 56 bits.
D5	WR__COM	R/W	Indicates that the DP83957 has completed a SRAM Write operation.
D4	RD__COM	R/W	Indicates that the DP83957 has completed ''N'' byte reads from SRAM. The result of the transfer is contained in the Read Data Byte Registers. **Note:** ''N'' corresponds to the value programmed into the RAC[3:0] bits in Configuration Register 1.
D3	IPN	R/W	The Management Status received on the management bus contains a valid DP83950 ID but an invalid port number. This will normally occur if the Port number is greater than 13.
D2	OVRF	R/W	This bit indicates that an attribute overflow occurred for an attribute specified in the Overflow Status Register 2. The DP83950 ID and Port Number is specified in the Overflow Status Register 1.
D1–D0	RES	—	Reserved

6.0 Register Description (Continued)

6.7 READ DATA BYTE REGISTER 1–6 (0x10–0x15)

The Read Data Byte Registers are used to buffer the data requested by the CPU from the external SRAM. The CPU can read data from the SRAM in chunks of 1 to 6 bytes, depending on what values are stored in bits RAC[2:0] of Configuration Register 1.

Reset State: Undefined

Bit	Bit Name	Access	Bit Description
D7–D0	RD__DATA[7:0]	Read	These registers hold ''N'' bytes of data that are read from external SRAM. The first byte read back will be placed in Read Data Register 1 (0x10). Therefore, if a 32-bit counter is read, N will be 4 and the least significant byte will be placed in Read Data Register 1.

6.8 ACCESS REGISTER 1 (0x20)

Access Register 1 selects a Port Attribute (offset) for a selected DP83950 ID and port number. The selected DP83950 and port number is specified in Access Register 2. The ACC__1[5:0] bits provide the 6-bit attribute offset, within a page.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7–D6	RES	—	Reserved
D5–D0	ACC__1[5:0]	Read/Write	These 6 bits specify the Port Attribute for a selected DP83950 and Port number. refer to the Port Attribute Memory Map.

6.9 ACCESS REGISTER 2 (0x21)

Access Register 2 provides the page select for the Port Attribute Memory Map. The memory map for each DP83950 is broken up into 13 pages, where each page represents a port on the DP83950.

To access a Port Attribute, Access Register 2 must be programmed to select which of the two DP83950's associated with the DP83957 and the specific port (1–13) needs to be examined. Once Access Register 2 is programmed, the CPU can now go and examine or modify a Port Attribute mentioned in Section 5.2.4.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D7–D5	RES	—	Reserved
D4	RIC__SEL	Read/Write	This bit selects one of the two DP83950's associated with the DP83957. If RIC__SEL is: 0: DP83950 ID 1 is selected 1: DP83950 ID 2 is selected
D3–D0	PORT[3:0]	Read/Write	These bits specify one of the 13 ports on a DP83950 that needs to be processed. The ports are numbered from 1 to 13, where port 1 is the full AUI port on the DP83950 (refer to the DP83950 data sheet for more information).

6.10 WRITE DATA BYTE REGISTER (0x22)

The Write Data Byte register holds the value that will be written to external SRAM. Depending on the write operation the value can be used to change certain or all bytes of an attribute or fill the entire SRAM with one value.

This register acts as a holding register for the CPU while the DP83957 is busy processing attributes. This allows the CPU to write the value into the register and forget about it, without waiting for the DP83957 to give control to the CPU.

Bit	Bit Name	Access	Bit Description
D[7:0]	WR__D[7:0]	Read/Write	This holds the data byte value that will be transferred to external SRAM on a write command.

6.0 Register Description (Continued)

6.11 DP83950 ID 1 REGISTER (0x30)

The DP83950 ID Registers 1 and 2 are used to associate one or two DP83950's in a multi-DP83950 repeater system, with a DP83957.

The ID address which is placed in these registers must correspond to the value that is placed in the DP83950's Address Register. These registers are located at Page 0 Address 0x17 in DP83950. Refer to Section 8.0 RIC Registers of the DP83950 data sheet for more information.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D[7:6]	RES	—	Reserved
D[5:0]	RICID__1[5:0]	Read/Write	This is the ID for the first DP83950 which is associated with this DP83957.

6.12 DP83950 ID 2 REGISTER (0x31)

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D[7:6]	RES	—	Reserved
D[5:0]	RICID__2[5:0]	Read/Write	This is the ID for the second DP83950 which is associated with this DP83957.

6.13 OVERFLOW STATUS 1 REGISTER (0x40)

Overflow Status Registers 1 and 2 are used to indicate a Port Attribute overflow. Overflow Status Register 1 must be used in conjunction with Overflow Register 2 to determine the overflow attribute.

If an overflow interrupt occurs, the CPU must, in the first instance, read Overflow Status Register 1 to determine on which DP83950 (i.e. 1 or 2) and Port number the overflow occurred. Following this, Overflow Register 2 needs to be read to determine the actual Port attribute which caused the interrupt.

Reset State: 0x00

Bit	Bit Name	Access	Bit Description
D[7:5]	RES	Read	Reserved
D4	RIC__ID	Read	This bit indicates which one of the two DP83950's connected to the DP83957 has an attribute overflow. This bit is encoded as follows: 0: represents DP83950 ID 1 1: represents DP83950 ID 2
D[3:0]	PORT__NUM	Read	These 4 bits indicate which one of the 13 ports of the particular DP83950 identified in bit D4, has an attribute overflow. The attribute which has overflowed is recorded in the Overflow Status Register 2 (refer to Section 6.14).

6.0 Register Description (Continued)

6.14 OVERFLOW STATUS 2 REGISTER (0x41)

Overflow Status Register 2 indicates which one of the port attributes has rolled over from 0xFF to 0x00.

Reset State: 0x3F

Bit	Bit Name	Access	Bit Description
D[7:0]	OVF[7:0]	Read	The byte value represents an encoded value (refer to table below) of the attribute that has rolled over from 0xFF to 0x00.

Overflow Status Encoding

The following table outlines the encoded OVF[7:0] bits for a Port Attribute overflow.

OVF[7:0] Value	Attribute Description
0x01	aReadableFrame Attribute
0x02	aReadableOctets Attribute
0x03	aFrameCheckSequenceErrors Attribute
0x04	aAlignmentErrors Attribute
0x05	aFramesTooLong Attribute
0x06	aShortEvents Attribute
0x07	aRunts Attribute
0x08	aCollisions Attribute
0x09	aLateEvents Attribute
0x0A	aVeryLongEvents Attribute
0x0B	aDataRateMismatches Attribute
0x0C	aSourceAddressChange Attribute

6.15 DP83957 REVISION REGISTER (0x50)

This register may be used to distinguish between different revisions of the DP83957. If this register is read, it will return a different value for each DP83957 revision (contact National Semiconductor for the latest revision information). A write to this register has no effect upon the contents.

Bit	Bit Name	Access	Bit Description
D[7:2]	REV[7:2]	Read	Always read back as 0
D1	REV1	Read	Highest bit of the revision number
D0	REV 0	Read	Lowest bit of the revision number

6.0 Register Description (Continued)

6.16 PORT ATTRIBUTE STATUS REGISTER 1

The Port Attribute Status Registers 1 and 2 are located in the Port Attribute memory map of each port. Port Attribute Registers 1 and 2 are used to indicate if any attributes have changed since the last CPU access to a particular port. These registers therefore provide a status indication of any attribute changes.

The CPU needs to ensure that the port Attributes are cleared after a CPU read to these two registers. This will guarantee that the CPU has taken a snap-shot of the Port Attributes correctly. The Management block of the DP83957 automatically updates the attributes on a port-per-packet basis.

Reset State: Undefined (SRAM)

Bit	Bit Name	Access	Bit Description
D7	LEVNT	Read/Write	This status bit indicates whether a port experienced a Late Event.
D6	COL	Read/Write	This status bit indicates whether a port experienced a Collision.
D5	RUNT	Read/Write	This status bit indicates whether a port experienced a Runt.
D4	SEVNT	Read/Write	This status bit indicates whether a port experienced a Short Event.
D3	FTL	Read/Write	This status bit indicates whether a port experienced a Frame Too Long condition.
D2	AERR	Read/Write	This status bit indicates whether a port experienced an Alignment Error.
D1	FCSERR	Read/Write	This status bit indicates whether a port experienced a Frame Check Sequence Error on a packet.
D0	RFO	Read/Write	This status bit indicates whether a port experienced a Readable Frame or a frame with Readable Octets.

6.17 PORT ATTRIBUTE STATUS REGISTER 2

Port Attribute Status Register 2 is an extension to the Port Attribute Status Register 1 for any port.

Reset State: Undefined (SRAM)

Bit	Bit Name	Access	Bit Description
D7–D3	RES	—	Reserved
D2	SAC	Read/Write	This status bit indicates whether a port experienced a change of Source Address from the address stored in the aLastSourceAddress attribute.
D1	DRM	Read/Write	This status bit indicates whether the port experienced a Data Rate Mismatch.
D0	VLE	Read/Write	This status bit indicates whether the port experienced a Very Long Event.

7.0 DC Specifications

ABSOLUTE MAXIMUM RATINGS

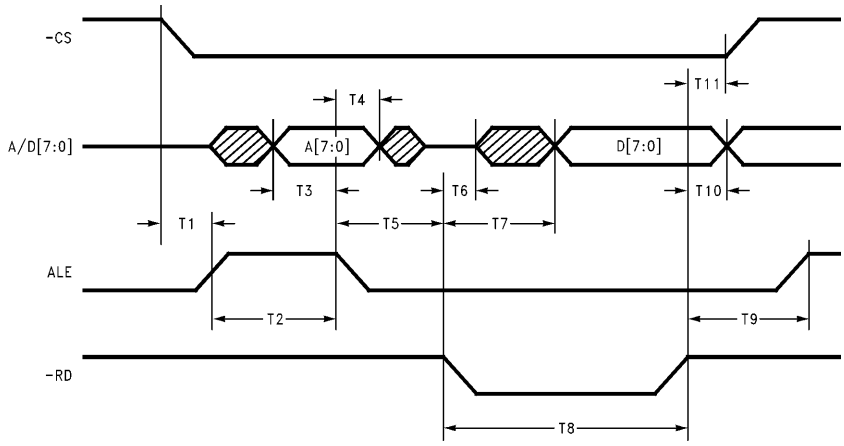
Supply Voltage (V_{CC})	−0.3V to +7V	Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Input Voltage (V_{IN})	−0.5V to V_{CC} + 0.5V	Power Dissipation (P_D)	
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V	ESD Rating (R_{zap} = 1.5k, C_{zap} = 120 pF)	1.5 kV

T_A = 0°C to + 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Description	Conditions	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}/V_{IL}$ V_{DD} = 4.5V I_{OH} = −1 mA to −24 mA	3.7		V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}/V_{IL}$ V_{DD} = 4.5V I_{OH} = 20 μA I_{OH} = 1 mA to −12 mA		 0.1 0.4	 V V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low level Input Voltage			0.8	V
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$ V_{DD} = 5.5V		−10	μA
I_{IH}	High Level Input Current	$V_{IN} = V_{SS}$ V_{DD} = 5.5V		10	μA
I_{OZL}	Low Level TRI-STATE Output Current	$V_O = V_{SS}$ V_{DD} = 5.5V		−10	μA
I_{OZH}	High Level TRI-STATE Output Current	$V_{IN} = V_{SS}$ V_{DD} = 5.5V		10	μA
I_{CC}	Average Operating Current			50	mA

8.0 AC Specifications

8.1 CPU READ TIMING

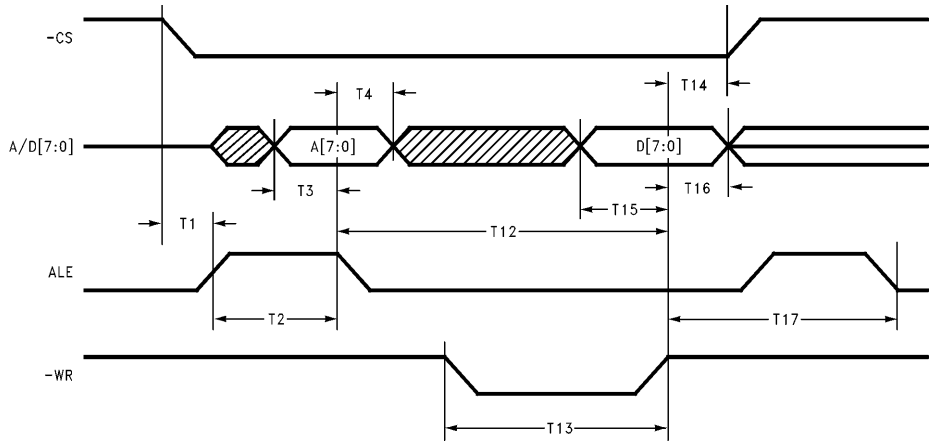


TL/F/12437–7

Number	Parameter	Min	Max	Units
T1	CS Assertion to ALE High	20		ns
T2	ALE High Width	20		ns
T3	Address Setup to ALE	10		ns
T4	Address Hold from ALE	10		ns
T5	ALE Deassertion to RD Assertion	60		ns
T6	Read Assertion to Address/Data Bus Enabled	0		ns
T7	Read Data Strobe to Data Valid		bcyc + 22	ns
T8	Read Low Width	bcyc + 22		ns
T9	Read Deassertion to ALE Assertion	40		ns
T10	Read Data Strobe to Data TRI-STATE	0		ns
T11	Read Deassertion to Chip Select Deassertion	0		ns

8.0 AC Specifications (Continued)

8.2 CPU WRITE TIMING

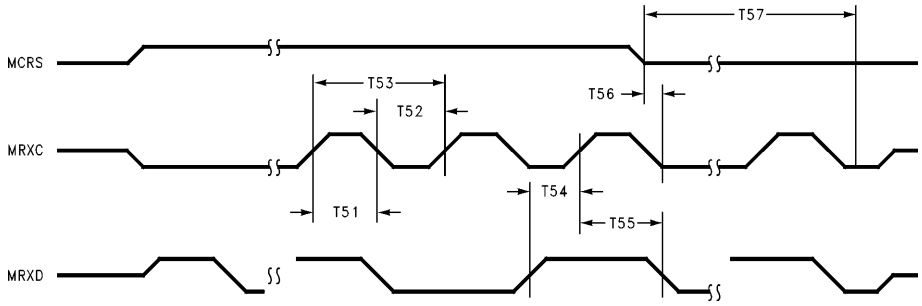


TL/F/12437–8

Number	Parameter	Min	Max	Units
T1	Chip Selection to ALE High	20		ns
T2	ALE High Width	20		ns
T3	Address Setup Time to ALE	10		ns
T4	Address Hold Time from ALE	10		ns
T12	ALE Deassertion to Write Deassertion	60		ns
T13	Write Strobe Low Width	bcyc + 20		ns
T14	Write Deassertion to Chip Selection Deassertion	0		ns
T15	Data Setup to Write Data Strobe	10		ns
T16	Data Hold from Write Data Strobe	10		ns
T17	Write Deassertion to ALE Deassertion	40		ns

8.0 AC Specifications (Continued)

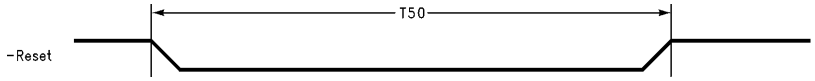
8.3 MANAGEMENT BUS INTERFACE TIMING



TL/F/12437–9

Number	Parameter	Min	Max	Units
T51	MRXC High Time	45	55	ns
T52	MRXC Low Time	45	55	ns
T53	MRXC Cycle Time	90	110	ns
T54	MRXD Setup	40		ns
T55	MRXD Hold Time	45		ns
T56	MRXC Low to MCRS Inactive	−5	6	ns
T57	Min Number of MRXC's after MCRS Inactive	5	5	clks

8.4 RESET TIMING



TL/F/12437–10

Number	Parameter	Min	Max	Units
T50	Reset Pulse Width	800	—	ns

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408