National Semiconductor

PRELIMINARY

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DP83924A Quad 10 Mb/s Ethernet Transceiver

General Description

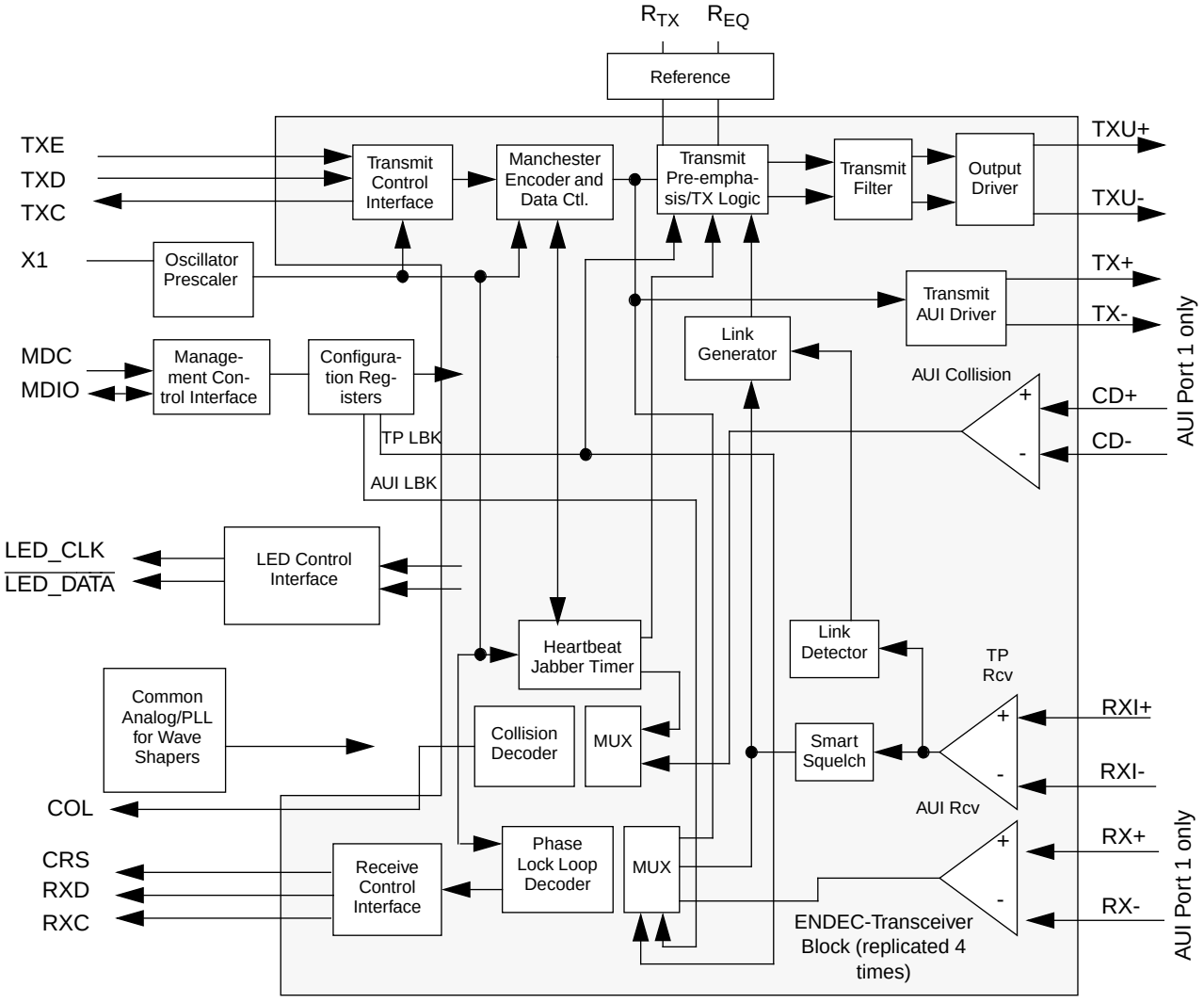
The Quad 10 Mb/s Ethernet Transceiver is a 4-Port Encoder/Decoder (ENDEC) that includes all the circuitry required to interface four Ethernet Media Access Controllers (MACs) to 10BASE-T. This device is ideally suited for switch hub applications where 8, 16, 24, or 32 ports are commonly used.

The DP83924A has three dedicated 10BASE-T ports. There is an additional port that is selectable for either 10BASE-T or for an Attachment Unit Interface (AUI). In 10BASE-T mode, any port can be configured to be Half or Full Duplex. (Continued)

Features

- 100 pin package
- 10BASE-T and AUI interfaces
- 4 ports TP interface with TRI-STATE control
- Single Full AUI and TP Interface on port 1 supports 50 meter drops
- Automatic or manual selection of twisted pair or Attachment Unit Interfaces on port 1
- Direct Interface to NRZ Compatible controllers
- MII-Like Management Interface (Continued)

System Diagram



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General Description (Continued)

The various modes on the transceivers can be configured and controlled via the MII management interface. This management interface makes inter-operability with other manufacturers MAC units relatively easy. If no management interface is desired, some of the critical operating modes of the transceiver can be set via strapping options (latching configuration information during reset). The ENDEC section of the transceiver also supplies a simple Non-Return-to-Zero (NRZ) interface to transmit and receive data to/from standard 10 Mb/s MACs.

The transceivers include on-chip filtered transmit outputs, which reduce emissions and eliminate the need for external filter modules.

Features (Continued)

- Serial management interface for configuration and monitoring of ENDEC/Transceiver operation
- Twisted Pair Transceiver Module
  - On-chip filters for transmit outputs
  - Adjustable Equalization and Amplitude
  - Low Power Driver
  - Heartbeat and Jabber Timers
  - Link Disable and Smart Receive Squelch
  - Polarity detection and correction
  - Jabber Enable/Disable
- ENDEC Module (one per port)
  - Low Power Class AB Attachment Unit Interface (AUI) Driver for one port
  - Enhanced Supply Rejection
  - Enhanced Jitter Performance
  - Diagnostic ENDEC Loopback
  - Squelch on Collision and Receive Pair
- Serial LED interface for LINK, POLARITY, ACTIVITY, and ERROR
- JTAG Boundary Scan per IEEE 1149.1

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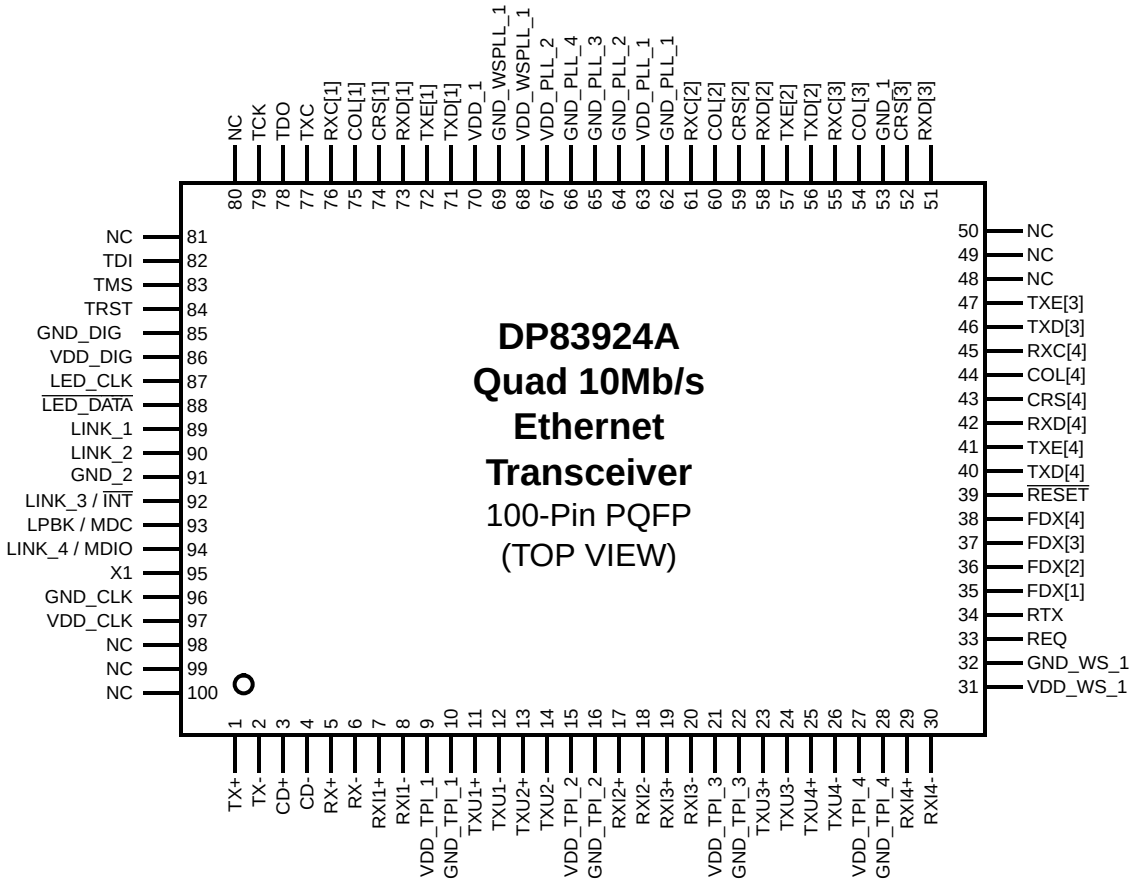
1.0 Pin Information

1.1 Pin Connection Diagram



Order Number DP83924AVCE

NS Package Number VCE100A

1.0 Pin Information (Continued)

1.2 Pin Description

Table 1. NRZ CONTROLLER INTERFACE and MANAGEMENT INTERFACE: These pins provide the interface signalling between the Media Access Controller and the transceiver. (30 Pins)

Symbol	Pin #	Type	Description
TXC	77	O	**Transmit Clock:** This pin outputs a 10 MHz output clock signal synchronized to the transmit data (one pin for all ports).
TXD[4] TXD[3] TXD[2] TXD[1]	40 46 56 71	I	**Transmit Data:** The serial TXD contains the transmit serial data output stream.
$\overline{\text{TXE[4]}}$ $\overline{\text{TXE[3]}}$ $\overline{\text{TXE[2]}}$ $\overline{\text{TXE[1]}}$	41 47 57 72	I	**Transmit Enable:** This active high input indicates the presence of valid data on the TXD pins.
$\overline{\text{CRS[4]}}$ $\overline{\text{CRS[3]}}$ $\overline{\text{CRS{2]}}}$ $\overline{\text{CRS[1]}}$	43 52 59 74	O, pull-up O, pull-up O, pull-up O, pull-up	**Carrier Sense:** Active high output indicates that valid data has been detected on the receive inputs. CRS[3:1] are dual purpose pins. When $\overline{\text{RESET}}$ is active, the value on these pins are sampled to determine the transceiver address for the mgmt interface. These pins have internal pull-ups, a 2.7 kΩ pull down resistor is required to program a logic '0'.
$\overline{\text{COL[4]}}$ $\overline{\text{COL[3]}}$ $\overline{\text{COL[2]}}$ $\overline{\text{COL[1]}}$	44 54 60 75	O, pull-up O, pull-up O, pull-up O, pull-up	**Collision:** This active high output is asserted when a collision condition has been detected. It is also asserted for 1µs at the end of a packet to indicate the SQE test function. COL[4:1] are dual purpose pins. When $\overline{\text{RESET}}$ is active, these pins are sampled and selects the operating mode for the device. To select the non-default mode(s), a 2.7 kΩ pull down resistor(s) is required. The strappable functions are: COL[4]; selects the number of receive clocks after carrier sense deassertion (5 RXCs or continuous RXCs). Default is 5 RXCs. COL[3]; enables or disables the receive filter. Default is to disable the receive filter. COL[2]; selects the full duplex operating mode (normal or enhanced). Default is normal full duplex mode. COL[1]; selects the LED operating mode (normal or enhanced). Default is normal LED mode.
RXC[4] RXC[3] RXC[2] RXC[1]	45 55 61 76	O	**Receive Clock:** This 10 MHz signal is generated by the transceiver, and is the recovered clock from the decoded network data stream. The number of RXCs after the deassertion of CRS is programmable via the Global Configuration Register, GATERXC bit, D0. The options are for 5 RXCs or continuous RXCs.
$\overline{\text{RXD[4]}}$ $\overline{\text{RXD[3]}}$ $\overline{\text{RXD[2]}}$ $\overline{\text{RXD[1]}}$	42 51 58 73	O	**Receive Data:** Provides the decoded receive serial data. Data is valid on the rising edge of RXC.
$\overline{\text{MDC}}$ LPBK	93	I	**Management Data Clock:** When "normal" full duplex mode is selected (strap option, COL[2]=1), this clock signal (0-2.5 MHz) is the clock for transferring data across the management interface. **LoopBack**: When "enhanced" full duplex mode is selected (strap option, COL[2]=0), then this pin is an active high input to configure all ports into diagnostic loopback mode.
$\overline{\text{MDIO}}$ LINK_4	94	I/O	**Management Data I/O:** When "normal" full duplex mode is selected (strap option, COL[2]=1), this Bidirectional signal transfers data on the management interface between the controller and the transceiver. **Link Lost Status Port 4**: When "enhanced" full duplex mode is selected, (strap option, COL[2]=0), this pin outputs the link lost status for port 4. If link is lost, this output is high.
INT LINK_3	92	OD	**Interrupt:** When "normal" full duplex mode is selected (strap option, COL[2]=1), this output pin is driven low when an interrupt condition is detected within the Quad Transceiver. An interrupt can occur when, link status changes or, LED status changes. This is an open-drain output. And requires an external pull-up resistor. **Link Lost Status Port 3**: When "enhanced" full duplex mode is selected, (strap option, COL[2]=0), this pin outputs the link lost status for port 3. If link is lost, this output is high.
LINK_2 LINK_1	90 89	O	**Link Lost Status Ports 1,2**: These pins indicate the link lost status for ports 1 and 2, when "enhanced" full duplex mode is selected.

1.0 Pin Information (Continued)

Table 2. NETWORK INTERFACES: Attachment Unit, Twisted Pair Interface (24 Pins)

Symbol	Pins	Type	Description
RXI4+ RXI4-	29 30	I	**Twisted Pair Receive Input:** This differential input pair receives the incoming data from the twisted pair medium via an isolation transformer.
RXI3+ RXI3-	19 20		
RXI2+ RXI2-	17 18		
RXI1+ RXI1-	7 8		
TXU4+ TXU4-	25 26	O	**UTP Transmit Outputs:** This pair of drivers provide pre-emphasized and filtered differential output for UTP (100Ω cable). These drivers maintain the same common mode voltage during data transmission and idle mode.
TXU3+ TXU3-	23 24		
TXU2+ TXU2-	13 14		
TXU1+ TXU1-	11 12		
REQ	33	I	**Equalization Resistor:** An external resistor connects to ground to adjust the equalization on the twisted pair transmit outputs.
R_{TX}	34	I	**Transmit Amplitude Resistor:** An external resistor connects to ground to adjust the amplitude of the differential transmit outputs to the unshielded twisted pair cable.
Attachment Unit Interface			
RX+ RX-	5 6	I	**Port 1 Full AUI Receive Input:** In AUI mode this differential input pair receives the incoming data from the AUI medium via an isolation transformer.
TX+ TX-	1 2	O	**Port 1 Full AUI Transmit Output:** In AUI mode this differential pair sends encoded data from the AUI transceiver. These outputs are source followers and require 270 Ohm pull down resistors.
CD+ CD-	34	I	**Port 1 Full AUI Collision Detect**: In AUI mode, this differential input pair receives the collision detect signals from the AUI medium via an isolation transformer.

Table 3. LED & GENERAL CONFIGURATION Pins (8 Pins)

Symbol	Pins	Type	Description
$\overline{\text{LED\_DATA}}$	88	O	**LED serial data output:** This output should be connected to the input of the 1st serial shift register.
LED_CLK	87	O	**LED Clock:** This is the clock for the serial shift registers.
X1	95	I	**External Oscillator Input:** This signal is used to provide clocking signals for the internal ENDEC. A 20 MHz oscillator module should be used to drive this pin.
$\overline{\text{RESET}}$	39	I	**Reset:** Active low input resets the transceiver, and starts the initialization of the device. This pin has a noise filter on it's input, which requires that the reset pulse must be greater than 30 TXC's.
FDX[4:1]	38 -35	I	**Full Duplex:** This pin is sampled during reset. They control the full duplex (or half duplex) configuration of each port.

1.0 Pin Information (Continued)

Table 4. SCAN TEST Pins (5 Pins)

Symbol	Pins	Type	Description
TCK	79	I	**Test Clock:** This signal is used during boundary scan to clock data in and out of the device.
TDI	82	I	**Test Input:** The signal contains serial data that is shifted into the device by the TAP controller. An internal pullup is provided if not used.
TDO	78	O,Z	**Test Output:** The signal can be set to TRI-STATE and contains serial data that is shifted out of the device by the TAP controller.
TMS	83	I	**Test Mode Select:** This selects the operation mode of the TAP controller. An internal pullup is provided if not used.
$\overline{\text{TRST}}$	84	I	**Test Reset:** When this signal is asserted low, it forces the TAP (Test Access Port) controller into a logic reset state. An internal pullup is provided. This pin should be pulled low during normal operation.

Table 5. POWER AND GROUND Pins (33 Pins)

Symbol	Pins	Type	Description
NC NC NC NC NC NC NC NC	48 49 50 80 81 98 99 100	NA	No Connect
VDD_TPI_4 VDD_TPI_3 VDD_TPI_2 VDD_TPI_1	27 21 15 9	P	Power for TPI Ports 1-4
GND_TPI_4 GND_TPI_3 GND_TPI_2 GND_TPI_1	28 22 16 10	G	Ground for TPI Ports 1-4
VDD_PLL_2 VDD_PLL_1	67 63	P	Power for PLL Circuitry
GND_PLL_4 GND_PLL_3 GND_PLL_2 GND_PLL_1	66 65 64 62	G	Ground for PLL Circuitry
$\overline{\text{VDD\_WSPLL\_1}}$	68	P	Power for Wave Shaper and PLL Circuitry
GND_WSPLL_1	69	G	Ground for Wave Shaper and PLL Circuitry
VDD_WS_1	31	P	Power for Wave Shaper Circuitry
GND_WS_1	32	G	Ground for Wave Shaper Circuitry
VDD_DIG	86	P	Power for Core Logic
GND_DIG	85	G	Ground for Core Logic
GND_CLK	96	G	Ground for Clock Circuitry
VDD_CLK	97	P	Power for Clock Circuitry
GND_2 GND_1	91 53	G	Ground for NRZ Circuitry
VDD_1	70	P	Power for NRZ Circuitry

Table 6. Pin Type Description

Pin Type	Description
I	Input Buffer
O	Output Buffer (driven at all times)
I/O	Bi-directional Buffer
O, Z	Output Buffer with High Impedance Capability
OD	Open Drain-Like Output. Either driven Low or to a High Impedance State

2.0 Interface Descriptions

Interface Overview

The Quad Transceiver's interfaces can be categorized into the following groups of signals:

1. Management Interface - Allows host to read status and set operating modes.
2. Media Access Control Interface - Straight forward NRZ interface to Ethernet MACs.
3. LED Interface - Serial LED interface to off chip shift registers.
4. Network Interfaces - Integrated 10BASE-T and AUI.
5. Clock - Allows connection of an external clock module.

2.1 Management Interface

This interface is a simple serial interface that is modeled after the MII standard serial interface, though it does not adhere to the MII standard completely (the protocol is followed, but the register space is not). The interface signals consist of a clock and data line for transfer of data to and from the registers.

In a multiple Quad Transceiver system, it is necessary to distinguish between the devices in order to access the correct registers for configuration and status information. This is accomplished by assigning each Quad Transceiver a unique transceiver address. The lower 3 bits of the transceiver address, T[2:0], is latched in during reset based on the logic state of CRS[3:1]. The upper 2 bits of the transceiver address, T[4:3], must be zero. Therefore, 32 ports can be supported with a single MII bus.

The register address field indicates which register within the DP83924A that is to be accessed (read or write).

During a write operation, all 32 bits are driven onto MDIO by the host, indicating which transceiver and register the data is to be written.

During a read operation, the first 14 bits are driven onto MDIO by the host, then the bus is released, allowing the DP83924A to drive the requested data onto MDIO.

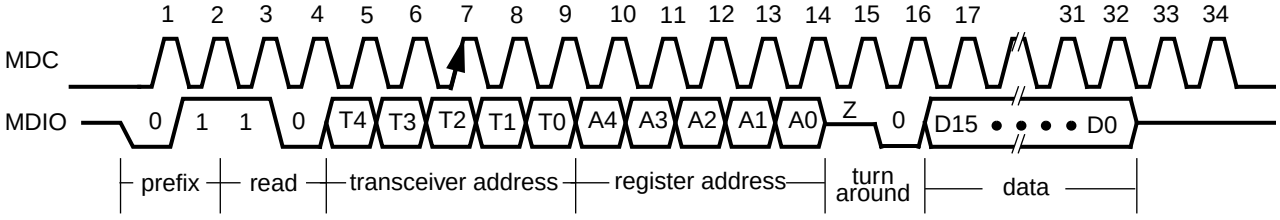
The serial lines do not require any preamble on these pins, however if it is provided it is ignored so long as the 0110 or 0101 pattern is not present. If a continuous MDC is not supplied, then at the end of each command (read or write), 2 additional MDCs are required in order to allow the internal state machine to transition back to it's idle state. Refer to Figure 1.

2.2 MAC Interface

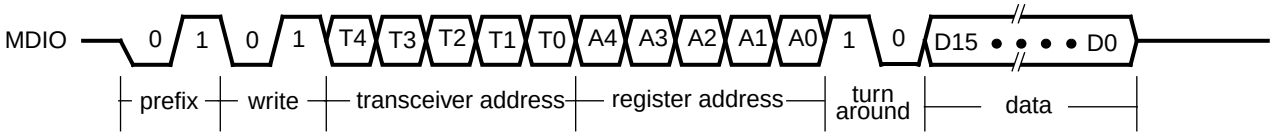
This interface connects the ENDEC/Transceiver to an Ethernet MAC controller. This interface consists of a serial data transmit interface and a serial receive interface. The interface clocks data out (on receive) or in (on transmit) on the rising edge of the clock. Refer to Figure 2. All signals are active high with rising edge sampling.The recovered clock (RXC) is selectable for 5 RXCs after the deassertion of carrier sense (CRS) or for continuous RXCs after the deassertion of CRS. This is programmable through the serial MII or through the COL[4] strapping option.

2.3 LED Interface

The LED interface consists of two modes. The first option, normal LED mode, requires an external 8-bit shift register. During every LED update cycle, 8-bits are shifted out to the external shift registers. This allows two status LEDs per port. One LED indicates activity (Tx or Rx) and the second indicates port status (per Table 6). The LEDs attached to the shift register will be on, if the associated port has tx or rx activity. The status LEDs will blink at different rates depending on the associated ports status.



Register Read



Register Write

Note 1: The management interface addressing includes a 5 bit field for the Transceiver Address, T[4:0], and a 5 bit field for the register address, A[4:0]. The MII assumes the transceiver address applies to a single port, but in this implementation a single address refers to a single IC. The transceiver address is set by 3 external pins, CRS[3:1]. T[4:3] must be zero to address the transceiver. Thus up to 32 10BASE-T ports can be addressed from a single interface (8 addr x 4 ports/addr).

Note 2: Two MDCs (clocks 33, 34) are required after each read or write in order to allow the internal state machine to transition back to it's IDLE state.

Figure 1. Serial Management Interface Timing Diagram (read/write)

2.0 Interface Descriptions (Continued)

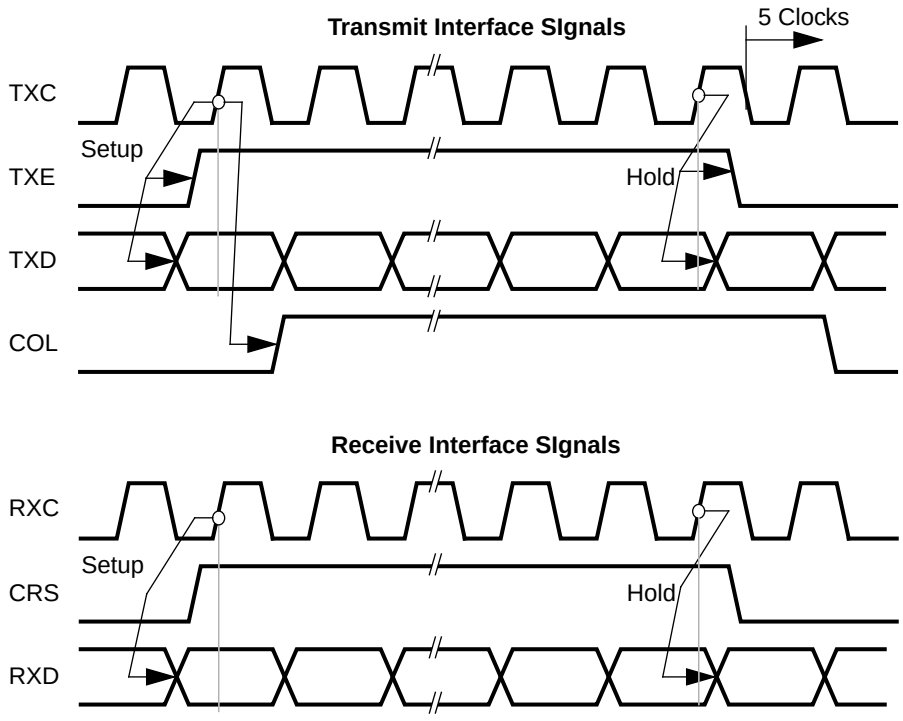


Figure 2. NRZ Interface Timing Diagram

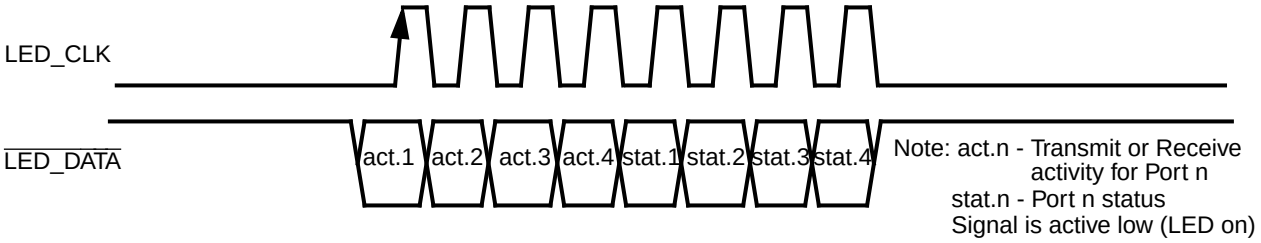


Figure 3. Normal LED Mode Timing Diagram

If a port experiences both Bad Polarity and Link Lost, then the LEDs will go to the fast blink state (i.e. Link Lost). Port activity and status are shifted out serially, with port 1 shifted out first. The LED update rate is every 50 ms. The LED clock rate is 1 MHz. All port activity is extended to 50 ms to make it visible. Data is valid on the rising edge of LED_CLK and is active low (LED on). Refer to Figure 3.

Table 7. Normal LED Mode

LED Condition	Status Indication
Off	Good Status
On - Solid	Error'd Status
Fast Blink (400 ms)	Link Lost
Slow Blink (1600 ms)	Bad Polarity

The second option, enhanced LED mode, serially shifts a 16-bit stream out of the Quad Transceiver. This option outputs per port data for Rx, Tx, Full Duplex (FDX), and LinkCoded status. These four bits per port are intended to be used to support two LEDs. One is a bi-color LED (decode of the FDX and LinkCoded bits) to indicate LINK status. The second LED indicates activity (Tx or Rx). The Tx and Rx bits are not intended to be used as separate LEDs for transmit and receive activity. Refer to the User Information document regarding this mode. As with the first LED option, port 1 status is shifted out first. Refer to Figure 4.

Table 8. Enhanced LED Mode - Bit Decode

FDX	LinkCoded	LED Status	Comments
0	0	OFF	Link Fail, Full Duplex
0	1	ON	Good Link, Full Duplex
1	0	ON	Good Link, Half Duplex
1	1	OFF	Link Fail, Half Duplex

2.0 Interface Descriptions (Continued)

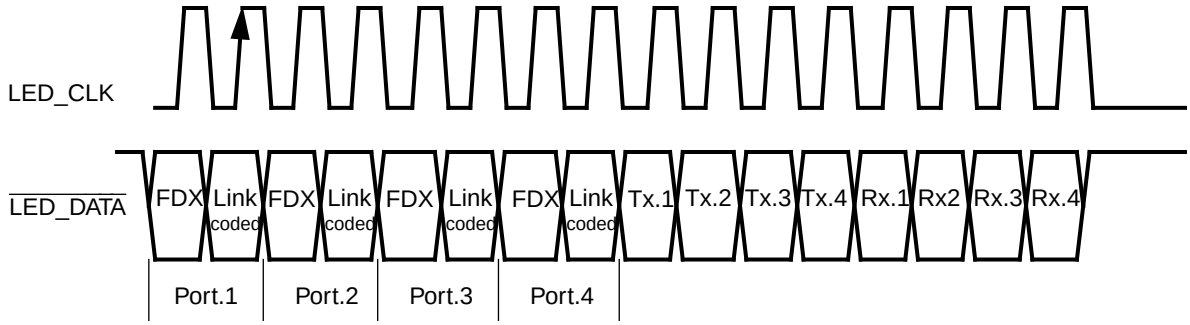


Figure 4. Enhanced Mode LED Timing Diagram

To select the desired LED mode, the COL [1] pin has a strapping feature. If COL[1] is a logic '0' during reset, then "enhanced" LED mode is enabled. If COL[1] is a logic '1' during reset, then "normal" LED mode is enabled.

2.4 Network Interface

2.4.1 Twisted Pair Interface

The Quad 10 Mb/s Transceiver provides two buffered and filtered 10BASE-T transmit outputs (for each port) that are connected to the output isolation transformer via two impedance matching resistor/capacitor networks. See Figure 5. The twisted pair receiver implements an intelligent receive squelch on the RXI+ differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. This smart squelch circuitry (which is described in detail under the Functional Description) employs a combination of amplitude and timing measurements to determine the validity of data on the twisted pair inputs. Only after these conditions have been satisfied will Carrier Sense (CRS) be generated to indicate that valid data is present.

2.4.2 Attachment Unit Interface

A single port (port 1) on the transceiver has a separate (non- multiplexed) AUI interface. This interface is a full 802.3 standard AUI interface capable of driving the full 50m cable. The schematic for connecting this interface to the AUI connector is shown in Figure 6.

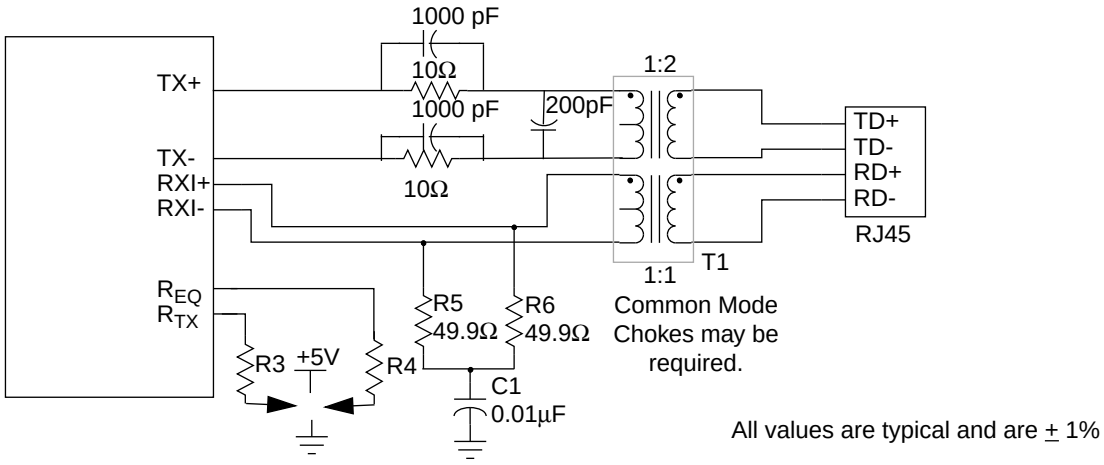


Figure 5. Twisted Pair Interface Schematic Diagram

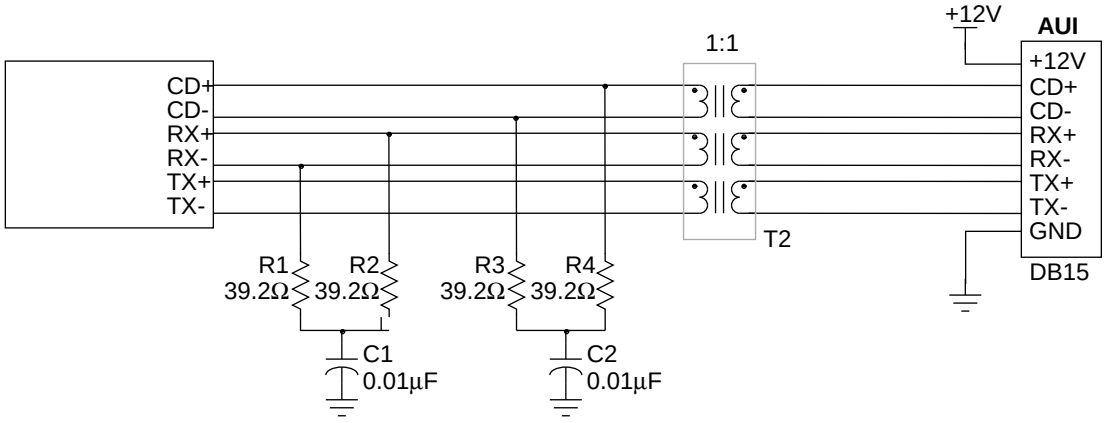


Figure 6. Full AUI Interface Schematic

If the standard 78Ω transceiver cable is used, the receive differential input must be externally terminated with two 39Ω resistors connected in series. In thin Ethernet applications, these resistors are optional. To prevent noise from falsely triggering the decoder, a squelch circuit at the input rejects signals with levels less than -175 mV. Signals more negative than -300 mV are decoded.

2.4.3 Oscillator Clock

When using an oscillator, additional output drive may be necessary if the oscillator must also drive other components. The X1 pin is a simple TTL compatible input. See Figure 7.

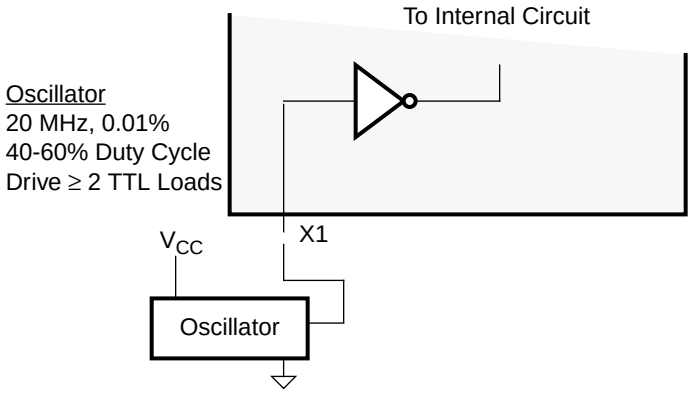


Figure 7. External Oscillator Connection Diagram

3.0 Detailed Functional Description

This product utilizes the standard 10BASE-T and AUI interface core building blocks which are replicated on this device, one per port. The basic function of these blocks are described in the following sections. Also described are the common digital blocks. Refer to the “System Diagram” on page 1.

3.1 Twisted Pair Functional Description

3.1.1 Smart Squelch

The Smart Squelch is responsible for determining when valid data is present on the differential receive inputs (RXI±). The Twisted Pair Transceiver (TPT) implements an intelligent receive squelch on the RXI± differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal.

The squelch circuitry employs a combination of amplitude and timing measurements to determine the validity of data on the twisted pair inputs. The operation of the smart squelch is shown in Figure 8.

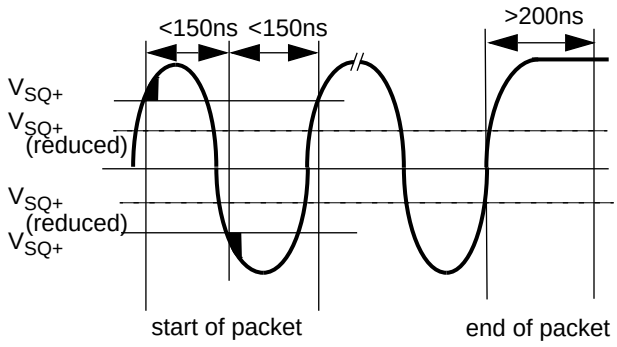


Figure 8. Twisted Pair Squelch Operation Diagram

The signal at the start of packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected. The checking procedure results in the loss of typically three bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart squelch circuitry is reset.

Valid data is considered to be present until squelch level has not been generated for a time longer than 150ns, indicating End of Packet. Once good data has been detected the squelch levels are reduced to minimize the effect of noise causing premature End of Packet detection.

3.1.2 Collision Detect

A collision is detected on the twisted pair cable when the receive and transmit channels are active simultaneously. If the ENDEC is receiving when a collision is detected (AUI only) it is reported to the MAC block immediately (through the COL signal). If, however, the ENDEC is transmitting when a collision is detected the collision is not reported until seven bits have been received while in the collision state. This prevents a collision being reported incorrectly due to noise on the network. The COL signal remains for the duration of the collision.

Approximately 1µsec after the transmission of each packet a signal called the Signal Quality Error (SQE) consisting of typically 10 cycles of a 10 MHz signal is generated by the transceiver. This 10 MHz signal, also called the Heartbeat, assures the continued functioning of the collision circuitry. The SQE signal is passed on to the MAC via the COL signal and is represented as a pulse.

3.1.3 Link Detector/Generator

The link generator is a timer circuit that generates a link pulse as defined by the 10BASE-T specification that will be sent by the transmitter section. The pulse which is 100ns wide is transmitted on the transmit output, every 16ms, in the absence of transmit data. The pulse is used to check the integrity of the connection to the remote MAU.

The link detection circuit checks for valid pulses from the remote MAU and if valid link pulses are not received the link detector will disable the twisted pair transmitter, receiver and collision detection functions.

3.1.4 Jabber

The Jabber function disables the transmitter if it attempts to transmit a much longer than legal sized packet. The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than 20-30ms. The transmitter is then disabled for the entire time that the ENDEC module's internal transmit is asserted. The transmitter signal has to be deasserted for approximately 400-600 ms (the unjab time) before the Jabber re-enables the transmit outputs.

There is also a jabber disable bit in each of the port control/status registers which when activated, disables the jabber function.

3.1.5 Transmit Driver

The transmit driver function utilizes the internal filters to provide a properly matched and wave shaped output which directly drives the isolation transformer/choke.

3.1.6 Transmit Filter

There is no need for external filters on the twisted pair transmit interface because the filters are integrated. Only an isolation transformer and impedance matching resistors are needed for the transmit twisted pair interface (see Figure 5). The transmit filter ensures that all the harmonics in the transmit signal are attenuated by at least 27dB. The transmit signal requires a 1:2 (1 on the chip side and 2 on the cable side) isolation transformer.

3.2 ENDEC Module

The ENDEC consists of two major blocks:

— The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester, and transmits it differentially to the transceiver, through the differential transmit driver.

— The Manchester decoder receives Manchester data from the transceiver, converts it to NRZ data and recovers clock pulses and sends them to the controller.

3.2.1 Manchester Encoder and Differential Driver

The encoder begins operation when the Transmit Enable input (TXE) goes high and converts the clock and NRZ data to Manchester data for the transceiver. For the dura-

tion of TXE remaining high, the Transmit Data (TXD) is encoded for the transmit-driver pair (TX±). TXD must be valid on the rising edge of Transmit Clock (TXC). Transmission ends when TXE goes low. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

3.2.2 Manchester Decoder

The decoder consists of a differential receiver and a PLL to separate the Manchester encoded data stream into internal clock signals and data. Once the input exceeds the squelch requirements, Carrier Sense (CRS) is asserted off the first edge presented to the decoder. Once the decoder has locked onto the incoming data stream, it provides data (RXD) and clock (RXC) to the MAC.

The decoder detects the end of a frame when no more mid-bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for at least five more bit times after CRS goes low, to guarantee the receive timings of the controller.

The GATERXC bit, D0, in the Global Control and Status Register, controls the receive clock (RXC) gated function. This allows the selection between 5 RXCs after the deassertion of carrier sense (CRS) or continuous RXCs after the deassertion of CRS. The GATERXC function which is programmable through the serial management interface is also available via a strap option. The default mode is to enable 5 RXCs after the deassertion of CRS. If a 2.7 k resistor is connected to the COL[4] pin (and the device reset), then the continuous RXCs mode is enabled. If the GATERXC mode is configured through the strap option, a register write via the serial management interface to the GATERXC control bit in the Global Control Register will be ignored (this bit only). A read of this register will always show the default value for this bit (5 RXCs) even though continuous RXCs may have been programmed through the strap option. All other bits are read/write as normal.

3.2.3 Collision Translator

When in AUI Mode and the external Ethernet transceiver detects a collision, it generates a 10 MHz signal to the differential collision inputs (CD ±) of the Quad Transceiver. When these inputs are detected active, the transceiver asserts COL which signals the MAC controller to back off its current transmission and reschedule another one.

The differential collision inputs are terminated the same way as the differential receive inputs. The squelch circuitry is the same, rejecting pulses with levels less than -175 mV.

3.3 Additional Features

3.3.1 Transceiver Loopback

When diagnostic loopback is programmed (in twisted pair mode), the transceiver redirects its transmitted data back into its receive path. The transmit driver and receive input circuitry are disabled in diagnostic loopback mode, hence, the transceiver is isolated from the network cable. This allows for diagnostic testing of the data path all the way up to the transceiver without transmitting or being interrupted by the media. This test can be performed regardless of the link status (i.e. a twisted pair cable does not have to be connected to perform transceiver loopback).

3.3.2 AUI/TP AutoSwitching - Port 1

The AUI/TP autoswitching lets the transceiver auto-switch between the AUI and TP outputs. At power up, the autoswitch function is enabled (AUTOSW bit = 1). When the auto-switch function is enabled, it allows the transceiver to automatically switch between TP and AUI outputs. If there is an absence of link pulses, the transceiver will switch to AUI mode. Similarly, when the transceiver starts detecting link pulses it will switch to TP mode. The switching from one mode to the next is only done after the current packet has been transmitted or received. If the twisted pair output is jabbering and it gets into the link fail state, then the switch to AUI mode is made only after the jabbering has stopped (this includes the time it takes to unjab). Also, if TP mode is selected, transmit packet data will only be driven by the twisted pair outputs and the AUI transmit outputs will remain idle. Similar behavior applies when AUI mode is selected. In TPI mode, the twisted pair drivers will continue to send link pulses, however, no packet data will be transmitted. It must also be noted that when switching from TP to AUI mode, it might take a few msec to completely power-up the AUI before it becomes fully operational. Switching in the opposite direction (AUI to TP) does not have this power-up time, since the TP section is already powered (the twisted pair transmit section still sends link pulses in AUI mode).

3.3.3 Full Duplex Mode

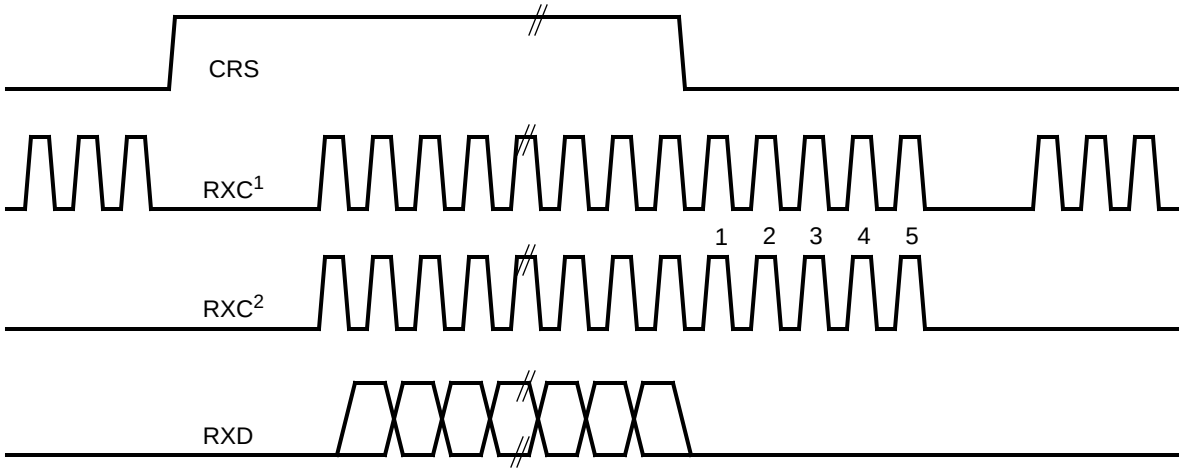
The full duplex mode is supported by the transceiver being able to simultaneously transmit and receive without asserting collision. The ENDEC has been implemented such that it can encode and decode simultaneously and also be robust enough to reject crosstalk noise with both transmit and receive channels enabled.

The full duplex feature has two modes of operation. The first option (normal FDX mode), allows full duplex configuration of the ports only after a reset (through the FDX[4:1] pins). The FDX[4:1] pins are sampled during reset to determine which ports to configure into full duplex mode. Changing the logic state on the FDX[4:1] pins will not take affect until a reset is performed. A logic ‘0’ enables full duplex and a logic ’1’ enables simplex mode. In addition, the full duplex capability of a port can also be changed dynamically by writing the FDX bit (D12) of the Port Control Register via the Mgmt Interface.

The second option (enhanced FDX mode), allows changing the full duplex configuration of each port dynamically through the FDX[4:1] pins. As soon as the logic state on the FDX[4:1] pins are changed, the corresponding ports full duplex mode will be enabled or disabled.

In order to select the desired full duplex mode, the COL[2] pin has a strapping feature. The default is normal full duplex mode. If enhanced full duplex mode is desired, then a 2.7k pull-down resistor is required on the COL[2] pin. During reset, the COL[2] pin is sampled to determine the correct full duplex mode configuration.

Regardless of the full duplex mode, the logic state of the FDX[4:1] pins are sampled during reset to determine a port’s initial configuration for full duplex capability.



Note 1: Continuous receive clock mode. In this mode, when CRS is deasserted, at least 5 RXCs are generated. RXC will go to idle until the RXC can be switched to an internal free running 10 MHz signal. Conversely, when CRS is asserted, RXC will go to idle. It remains idle until the decoder is able to lock onto the incoming data stream and generate the recovered clock.

Note 2: 5 Receive clock mode. In this mode, when CRS deasserts, at least 5 RXCs are generated before RXC goes to idle. RXC will remain in idle until the next received packet.

Figure 9. Receive Clock Timing - 5 RXC Mode vs Continuous RXC Mode

3.3.4 JTAG Boundary Scan

The DP83924A supports JTAG Boundary Scan per IEEE 1149.1 via test clock (TCK), test data input (TDI), test data output (TDI), test mode select (TMS), and test reset (TRST).

3.3.5 Strapping Options

Table 9 shows the various strapping options and the associated pins used to configure the device at power-up. These pins are sampled during reset. These pins have internal pull-ups, if the default modes are desired, no external resistors are required. A 2.7 kΩ pull down resistor(s) are required to select non-default modes. If some type of control logic is used to select the non-default modes, instead of pull down resistors, then the level on the strapping pins must be maintained for approximately 10 clocks after the $\overline{\text{RESET}}$ signal deasserts.

3.3.6 R_{EQ} and R_{TX}

These pins can change the twisted pair differential output voltage amplitude. By adding pull-up resistors, the differential output voltage will increase. And adding pull down resistors, the differential output voltage will decrease. R_{TX} controls the amplitude of the output waveform and R_{EQ} controls the waveform equalization (pre-emphasis, location of the knee in a 5M waveform). If resistors are used to change the differential output voltage, then it is recommended that the same value resistor be used for both pins and both pins are either pulled-up or pulled-down. All IEEE transmitter electrical characteristics should be verified after adding resistors to R_{EQ} and R_{TX}. Based on device characterization, it is recommended that 47 kΩ pull down resistors be used for both R_{EQ} and R_{TX} in order to meet the IEEE 802.3 differential output voltage specification.

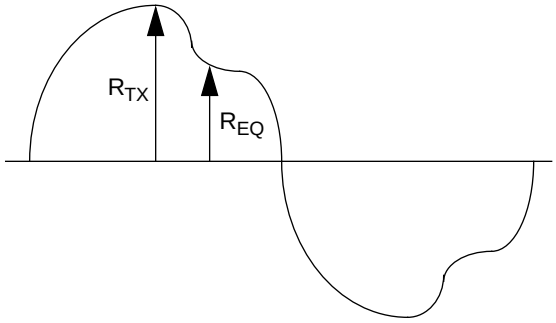


Figure 10. 5M Waveform Differential Output Voltage

Table 9. Strapping Option Description

Pin Name	Function	Default '1'	'0'	Comments
COL[4]	Gate RXC	5 RXCs	Continuous	Selects the # of RXCs after CRS deassertion
COL[3]	Rx Filter Select	Disabled	Enabled	Enables/disables the Rx filter. Suggest enable
COL[2]	Full Duplex Mode Select	Normal	Enhanced	Selects normal or enhanced full duplex mode
COL[1]	LED Mode Select	Normal	Enhanced	Selects normal or enhanced LED mode
CRS[3:1]	Transceiver Address Select	Address	Address	Sets the tcvr's address for MII access
FDX[4:1]	Per Port Full Duplex Select	None	Full Duplex	Selects full or half duplex configuration per port (no internal pull-ups)

4.0 Register Descriptions

4.1 Register Map and Descriptions

The following is an overall register map for the transceiver/ENDEC. There are two groups of registers. The first group provides individual port control which configures and reports status for functions applicable on a port basis. The second group provides global control which enables configuration of operations that are common to all the ports.

Table 10. DP83924A Register Map Accessible via the Management Interface

Register Address	Name	Description	Access
00H	Port 1 Control/Status	Configuration setting and Operational Status for Port 1.	R/W
01H	Port 2 Control/Status	Configuration setting and Operational Status for Port 2.	R/W
02H	Port 3 Control/Status	Configuration setting and Operational Status for Port 3.	R/W
03H	Port 4 Control/Status	Configuration setting and Operational Status for Port 4.	R/W
04H - 07H	Reserved	reserved	R
08H	Global Control and status	Provides global reset and interrupt configuration capabilities.	R/W
09H - 1EH	Reserved	reserved	R
1FH	Test Control	Controls test functions for manufacturing test of the device. User MUST NOT access this register.	R/W

Table 11. Port N Control/Status Register, addr = 00h - 03h (port 1 to port 4)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RST	LPBK	resv	FDX	JABE	resv	resv	LNKDIS	ERR	resv	resv	resv	resv	POLST	LNK ST	JAB ST

This register controls the various operating modes available for the transceiver and ENDEC functions. There is one register per ENDEC/Transceiver on this device.

Name	Bit	Reset (Default) Value	Description	Type
RST	D15	0	**Software Reset/Enable:** If this bit is set, then this port's transceivers and ENDEC modules are reset back to their idle state. If this bit is reset, then normal operation is expected.	R/W
LPBK	D14	0	**Loopback Transceiver:** If this bit is set, then this port's 10base-T transceiver will loop data from near the network interface pins back to the MAC, to test the operation of the transceiver. If this bit is reset, loopback is disabled.	R/W
resv	D13	0	**Reserved:** Must be written with '0'.	R/W
FDX	D12	strap	**Full Duplex Operation**: If this bit is set, then the ports full duplex capability is enabled. If this bit is reset, then half-duplex is enabled.	R/W
JABE	D11	1	**Jabber Enable:** If this bit is set, then the ports jabber function is enabled. If this bit is reset, then the jabber feature is disabled.	R/W
resv	D10-9	0	**Reserved**: Must be written with '0'.	R
LNKDIS	D8	0	**Link Disable:** If this bit is set, this port's link detection circuitry will be disabled. If this bit is reset, then normal link operation is enabled.	R/W
ERR	D7	0	**LED Error**: If this bit is set, this port's status LED will go solid. If this bit is reset, normal LED operation is resumed.	R/W
resv	D6-3	0	**Reserved**: Must be written with '0'.	R
POL ST	D2	1	**Polarity Status**: This bit is set when bad polarity has been detected. Status bit, read-only.	R
LNK ST	D1	1	**Link Status**: This bit is set when the port is in the link-fail state. Status bit, read-only.	R
JAB ST	D0	0	**Jabber Status**: This bit is set when the port is in the jabber condition. Status bit, read-only.	R

Table 12. Global Control/Mask Register, addr = 08h

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
resv	resv	LNKJABINT	AUTOSW	TPIAUI	HBEN	ENPOLSW	resv	resv	resv	resv	resv	resv	KLED	LJINTMASK	GATERXC

This register controls the various operating modes available for the transceiver and ENDEC functions. This register will affect the operation of ALL ports of the DP83924A.

Name	Bit	Reset (Default) Value	Description	Type
resv	D15-14	0	**Reserved**: Must be written with '0'.	R
LNKJABINT	D13	0	**Link Jabber Interrupt Status**: This bit is set when an interrupt occurs due to a link status change or a jabber condition on any port. This bit is cleared on a register read (the interrupt is also cleared).	R
AUTOSW	D12	1	**Auto Switching**: If this bit is set, automatic selection of TPI or AUI on port 1 is enabled. If this bit is reset, port 1 configuration is determined by the TPIAUI bit.	R/W
TPIAUI	D11	1	**TPI Select**: If this bit is set, then port 1 is placed into TP mode. If this bit is reset, then port 1 is configured for AUI mode. This bit is ignored if the AUTOSW bit is set.	R/W
HBEN	D10	1	**Hearbeat Enable**: If this bit is set, then heartbeat is enabled. If this bit is reset, it is disabled for all ports.	R/W
ENPOLSW	D9	1	**Enable Polarity Switching**: If this bit is set, then auto polarity detection and correction is enabled for all ports. If this bit is reset, it is disabled.	R/W
resv	D[8:3]	0	**Reserved**: Must be written with '0'.	R
KLED	D2	0	**Enhanced LED Mode**: If this bit is set, "enhanced" LED mode is selected. If this bit is reset, "normal" LED mode is selected.	R/W
LJINTMASK	D1	0	**Link Jabber Interrupt Mask**: If this bit is set, an interrupt will NOT be generated on a link-fail or jabber condition experienced on any port. If this bit is reset, interrupt generation is enabled.	R/W
GATERXC	D0	1	**RXC Gated**: If this bit is set, five RXC clocks are forced after CRS is deasserted. If this bit is reset, then RXC clocks are continuous after CRS deasserts.	R/W

5.0 Application Information

5.1 Magnetics Specifications

This section describes the required magnetics to be used with the Quad Transceiver. The external filter/transformer used in conventional twisted pair ports is now replaced by a transformer. By integrating the transmit filter, the transformer is the only magnetics required. In this configuration, a transformer with 1:2 turn ratio on the transmit path and a 1:1 turn ratio on the receive path is required. The system designer must determine if a choke is required. Careful layout may eliminate the need.

The following is a list of suppliers that may provide magnetic components with the electrical specifications listed in Table 13. This is not an exclusive list, and National Semiconductor makes no warranty as to the suitability of any of the magnetics. It is the responsibility of the user to verify the performance of any magnetics prior to production use.

BEL FUSE
HALO Electronics
PCA
PULSE Engineering
VALOR Electronics

Table 13. Transformer Electrical Specifications

Parameter	Pins	Value
Open Circuit Inductance (OCL)	3-4, 5-6	50 µH (min)
	1-2, 7-8, 9-10, 11-12, 13-14, 15-16.	200 µH (min)
Inter-winding Capacitance (C_{ww})	1-2 to 15-16, 3-4 to 13-14 5-6 to 11-12 7-8 to 9-10	12 pF (max)
Leakage Inductance (LL)	1-2, short 15-16 3-4, short 13-14 5-6, short 11-12 7-8, short 9-10	0.3 µH (max)
DC Resistance (DCR)	3-4, 5-6	0.35Ω (max)
	1-2, 7-8, 9-10, 15-16.	0.5Ω (max)
	11-12, 13-14	1.0Ω (max)
High Potential	1-2 to 15-16 3-4 to 13-14 5-6 to 11-12 7-8 to 9-10	2000 Vrms for 1 min.

5.2 Layout Considerations

Power Plane

— Minimize signal traces which traverse across multiple islands to reduce reflections and impedance mismatches. Therefore, the ground should extend from the DP83924A to under the magnetics (transformer).

— Use a single power plane.

Ground Plane

— Use a single ground plane, similar to the Power Plane.

DP83924A Placement and Routing

— The DP83924A should be placed as close as possible to the external transformer module/RJ45 connector.

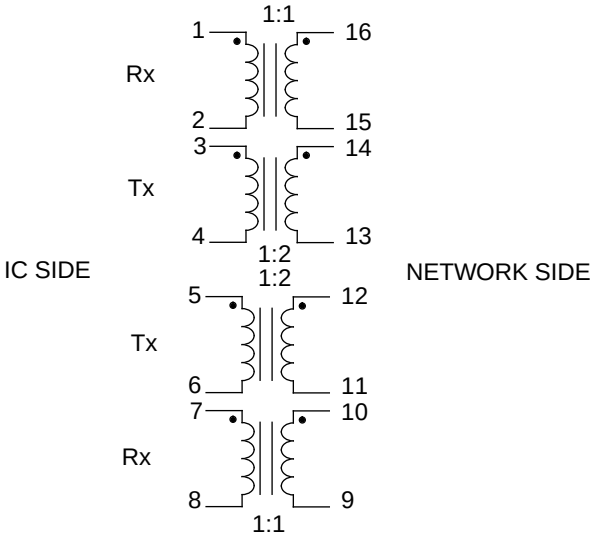


Figure 11. Typical Dual Transformer Pinout

— Each trace of a differential pair (i.e. TX+, TX-) between the DP83924A and the transformer module should be as follows:

Rx ± pair trace lengths should be matched. The width should be 8 mils min, with a trace-to-trace spacing of 8 mils min.

Tx ± pair trace lengths should be matched. The width should be 15 mils min, with a trace-to-trace spacing of 15 mils min (if the total trace length between the DP83924A and the RJ45 connector is less than 1.5", then 8 mil spacing and width can be used).

The Tx and Rx spacing should be 15 mils min.

— The source termination (R,C) must be placed as close to the device as possible.

— 100Ω traces between the transformer module and the RJ45 connector.

Analog Power and Ground Circuit

Recommended Low Pass Filter for the Internal PLL and WSPLL Circuitry to eliminate any power supply injected noise. This applies to both the PLL and WS supply pins. This should improve jitter performance. Refer to Figure 10 and Figure 11.

Bypass for all other supplies should use a 0.01 µF capacitor.

Additional bypass for the VDD_TPI supplies should use a 1.0 µF capacitor.

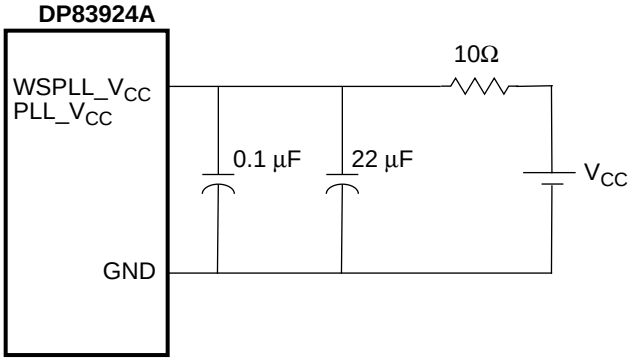


Figure 12. WSPLL and PLL V_{CC} Circuit Diagram

6.0 AC and DC Electrical Specifications

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.5V to + 7.0V
DC Input Voltage (V_{IN})	-0.5V to V_{CC} + 0.5V
DC Output Voltage (V_{OUT})	-0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	-65°C to + 150°C
Power Dissipation (PD)	1.6W
Lead Temperature (TL) (Soldering, 10 sec.)	260°C
ESD Rating (R_{ZAP} = 1.5k, C_{ZAP} = 120 pF)	1.5 kV

Recommended Operating Conditions

Supply voltage (V_{CC})	5 Volts ± 5%
Ambient Temperature	0°C to 70°C

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.*

DC Specifications T_A = 0˚C to 70˚C, V_{CC} = 5V ± 5%.

Symbol	Parameter	Conditions	Min	Max	Units
DIGITAL PINS (LED_CLK,$\overline{\text{LED\_DATA}}$,MDIO,MDC,CRS,RXC,RXD,COL,TXE,TXD,TXC,X1,$\overline{\text{RESET}}$,LINK,$\overline{\text{INT}}$,TCK,TDI,TDO,TMS,TRST)					
V_{OH1}	Minimum High Level Output Voltage	I_{OH} = -2 mA (Except MDIO and INTz)	3.0		V
V_{OH2}	Minimum High Level Output Voltage	I_{OH} = -8 mA (MDIO Only)	3.0		V
V_{OL1}	Maximum Low Level Output Voltage	I_{OL} = 2 mA (except MDIO and INTz)		0.4	V
V_{OL2}	Maximum Low Level Output Voltage	I_{OL} = 8 mA (MDIO and INTZ Only)		0.4	V
V_{IH}	Minimum High Level Input Voltage		2.0		V
V_{IL}	Maximum Low Level Input Voltage			0.8	V
I_{IN}	Pull-up Resistor Current (Note 1, 3)	V_{IN} = GND, V_{CC}=5V	-250	-100	µA
I_{IL}	Input Leakage (Note 2)	V_{IN} = V_{CC} or GND	-10	10	µA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND	-10	10	µA
I_{CC}	Average Operating Supply Current	TXU ± Transmitting into 50Ω (Note 4)		320	mA
AUI INTERFACE PINS (TX±, RX±, and CD±)					
V_{OD}	Diff. Output Voltage (TX±)	78Ω Termination	± 550	± 1200	mV
V_{DS}	Diff. Squelch Threshold (RX± and CD±)		-160	-300	mV
TWISTED PAIR INTERFACE PINS					
V_{ODT}	TXU ± Differential Output Voltage	100Ω Load @RJ45 Connector	4.4	5.6	Vp-p
V_{SRON1}	Receive Threshold Turn-On Voltage 10BASE-T Mode		± 300	± 585	mV
V_{SROFF}	Receive Threshold Turn-Off Voltage		± 175	± 300	mV

Note 1: CRS[4:1], COL[4:1], TDI, TMS, TRST

Note 2: MDIO, MDC, TXE[4:1]. TXD[4:1], X1, $\overline{\text{RESET}}$, TCK

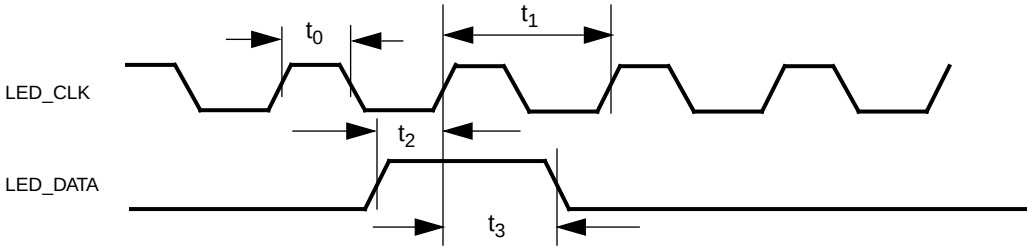
Note 3: Internal pull-up resistor typically 20 kΩ - 50 kΩ

Note 4: This includes the current consumed off chip by the load. Typically, the power dissipated off-chip is about 76 mW/port so the on-chip power being dissipated will be: [Total power dissipation (5.0v x 320ma)] - [the off-chip power dissipation (4 ports x 76 mW/port)] = 1.3W

6.0 AC and DC Electrical Specifications (Continued)

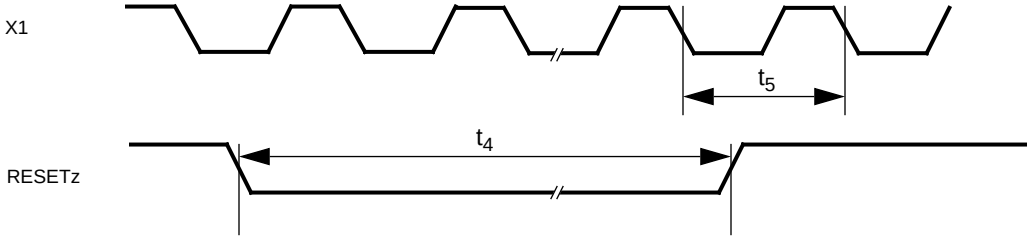
AC Switching Specifications $T_A = 0^\circ C$ to $70^\circ C$, $V_{CC} = 5V \pm 5\%$

LED Interface Timing



Symbol	Parameter	Min	Max	Units
t_0	LED Clock Duty Cycle	40	60	%
t_1	LED Clock Cycle Time	900	1100	ns
t_2	LED_Data Valid to LED_Clk	25		ns
t_3	LED_Data Valid from LED_Clk	25		ns

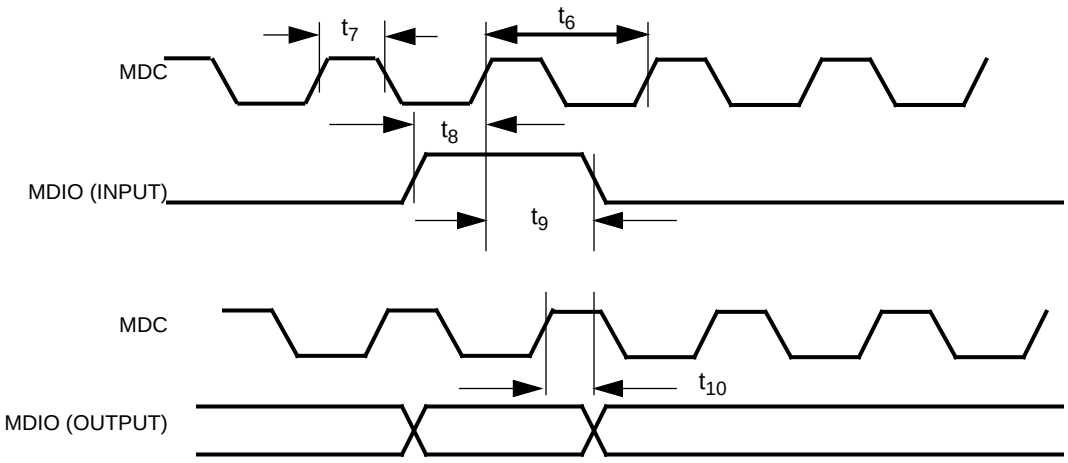
Reset and Strapping Timing



Symbol	Parameter	Min	Max	Units
t_4	Reset Pulse Width (X1 Must be Active During RESETz)	30	-	X1 Clks
t_5	X1 Duty Cycle	40	60	%

6.0 AC and DC Electrical Specifications (Continued)

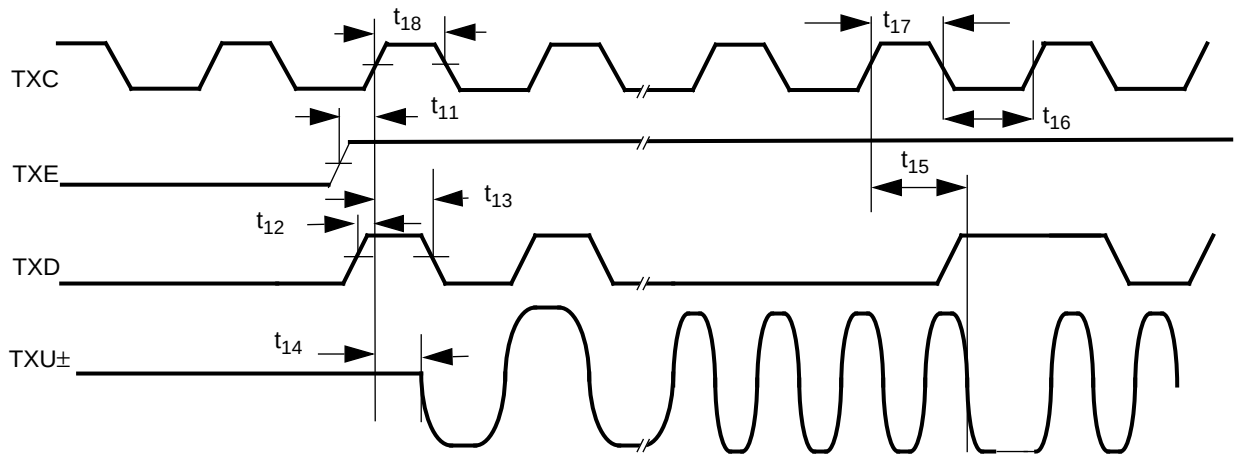
Management Interface Timing



Symbol	Parameter	Min	Max	Units
t_6	MDC Frequency		2.5	MHz
t_7	MDC Duty Cycle	40	60	%
t_8	MDIO (Input) Set Up to MDC Rising Edge	10		ns
t_9	MDIO (Input) Hold MDC from Rising Edge	10		ns
t_{10}	MDC to MDIO (Output) Delay Time		300	ns

6.0 AC and DC Electrical Specifications (Continued)

Twisted Pair Start of Transmit Packet

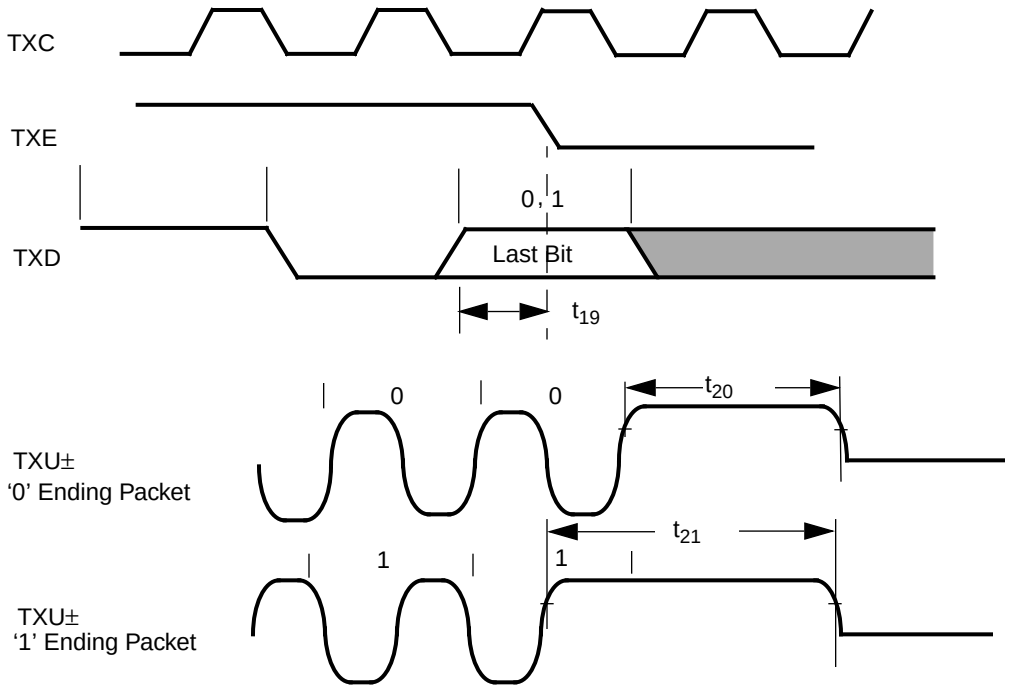


Symbol	Parameter	Min	Max	Units
t_{11}	TXE Setup Time to TXC Rising Edge	20		ns
t_{12}	TXD Setup Time to TXC Rising Edge	20		ns
t_{13}	TXD Hold Time from TXC Rising Edge	5		ns
t_{14}	TXU Start-up Delay from TXC Rising Edge		400	ns
t_{15}	TX Prop Delay (TXC Rising Edge to TXU±)		350	ns
t_{16}	TXC Low Time (Note 1)	40		ns
t_{17}	TXC High Time (Note 1)	40		ns
t_{18}	TXC Duty Cycle (Note 1)	40	60	%

Note 1: This specification is provided for information only and is not tested

6.0 AC and DC Electrical Specifications (Continued)

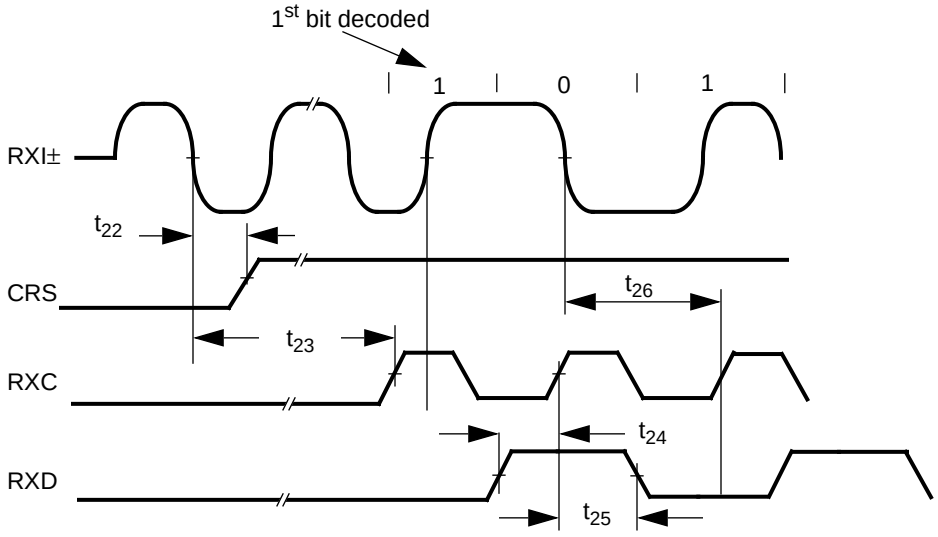
Twisted Pair Transmit End of Packet



Symbol	Parameter	Min	Max	Units
t_{19}	TXE Hold Time from TXC Rising Edge	5		ns
t_{20}	TXU± End of Packet Hold Time with "0" Ending Bit	225		ns
t_{21}	TXU± End of Packet Hold Time with "1" Ending Bit	225		ns

6.0 AC and DC Electrical Specifications (Continued)

Twisted Pair Start of Receive Packet

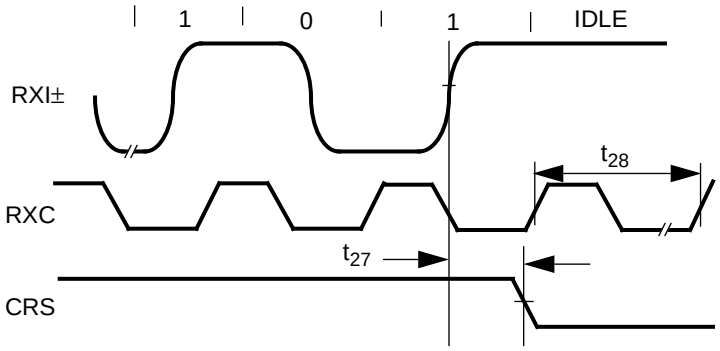


Symbol	Parameter	Min	Max	Units
t_{22}	Carrier Sense Turn On Delay (RXI± to CRS)		550	ns
t_{23}	Decoder Acquisition Time (Note 1)		2200	ns
t_{24}	Receive Data Valid to RXC Rising Edge	25		ns
t_{25}	Receive Data Invalid From RXC Rising Edge	25		ns
t_{26}	Receive Data Bit Delay		375	ns

Note 1: This parameter includes TPI smart squelch turn on time plus ENDEC data acquisition time.

6.0 AC and DC Electrical Specifications (Continued)

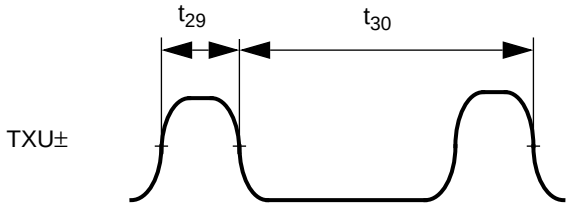
Twisted Pair End of Receive Packet



Symbol	Parameter	Min	Max	Units
t_{27}	Carrier Sense Turn Off Delay		400	ns
t_{28}	Number of RXCs after CRS Low (Note 1)	5		Bit Times

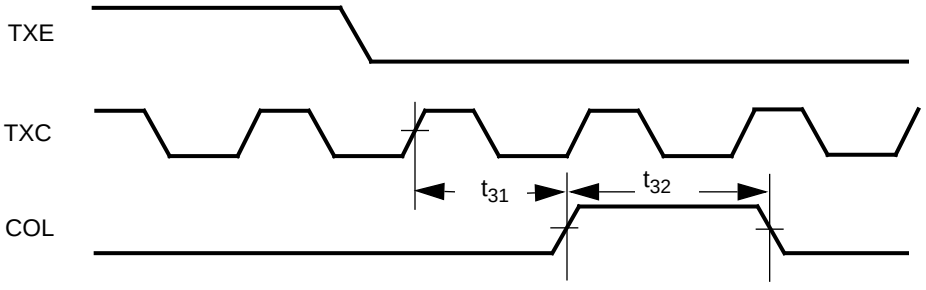
Note 1: This only applies when the GATERXC bit, D0, in the Global Configuration Register is set.

Link Pulse Timing



Symbol	Parameter	Min	Max	Units
t_{29}	Link Integrity Output Pulse Width	80	130	ns
t_{30}	Time between Link Output Pulses	8	24	ms

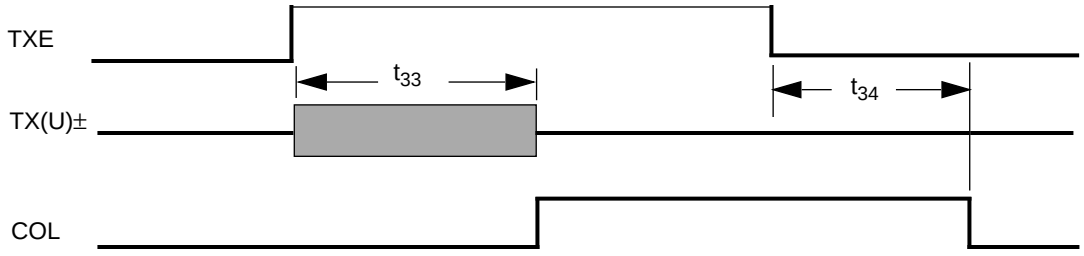
Heartbeat Specifications



Symbol	Parameter	Min	Max	Units
t_{31}	CD Heartbeat Delay	600	1600	ns
t_{32}	CD Heartbeat Duration	500	1500	ns

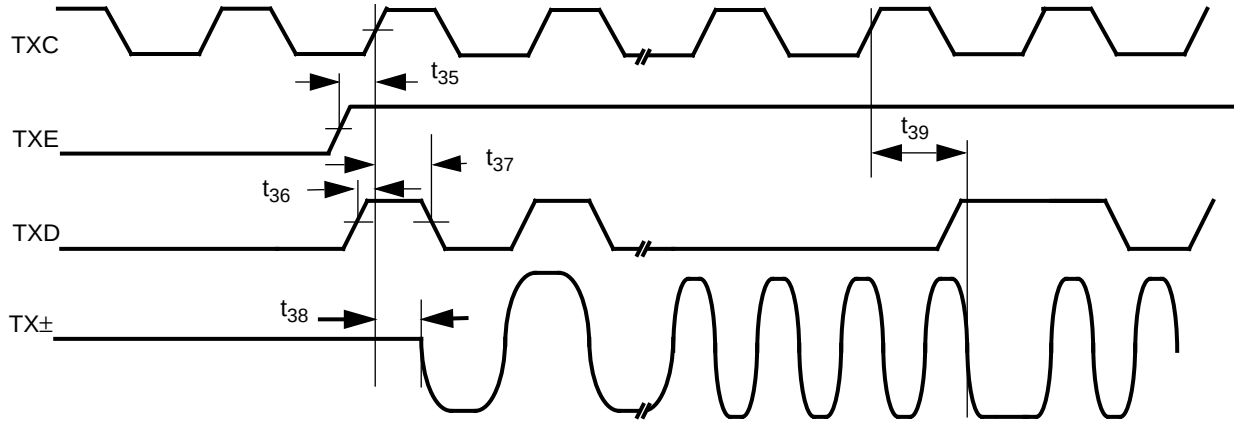
6.0 AC and DC Electrical Specifications (Continued)

Jabber Specifications



Symbol	Parameter	Min	Max	Units
t_{33}	Jabber Activation Time	20	60	ms
t_{34}	Jabber Deactivation Time	250	750	ms

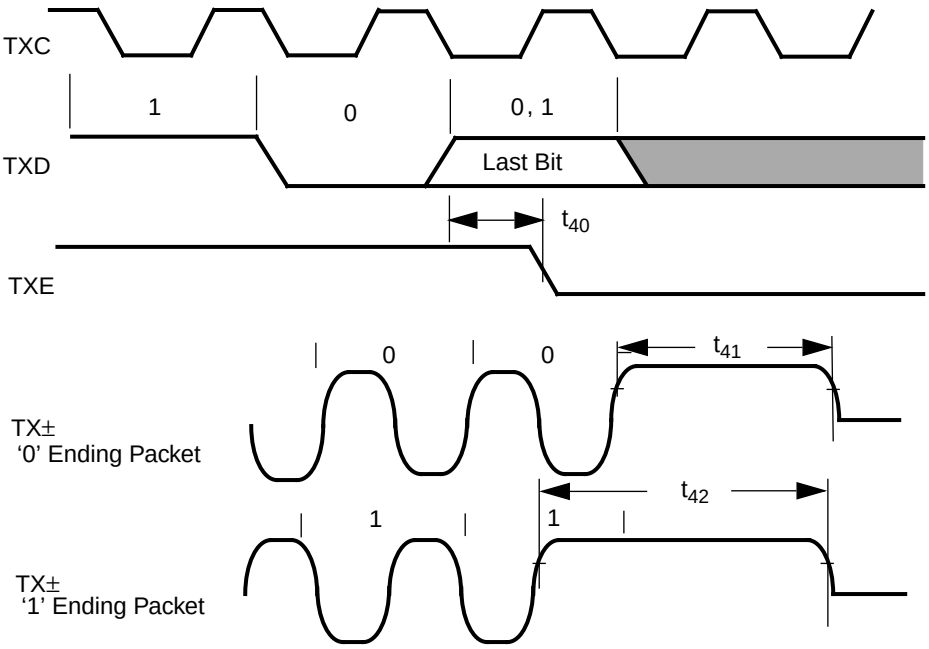
AUI Start of Packet Transmit Timing



Symbol	Parameter	Min	Max	Units
t_{35}	TXE Setup Time to TXC Rising Edge	20		ns
t_{36}	TXD Setup Time to TXC Rising Edge	20		ns
t_{37}	TXD Hold Time from TXC Rising Edge	5		ns
t_{38}	TX± Start-up Delay from TXC Rising Edge		300	ns
t_{39}	TX Prop Delay (TXC Rising Edge to Tx±)		300	ns

6.0 AC and DC Electrical Specifications (Continued)

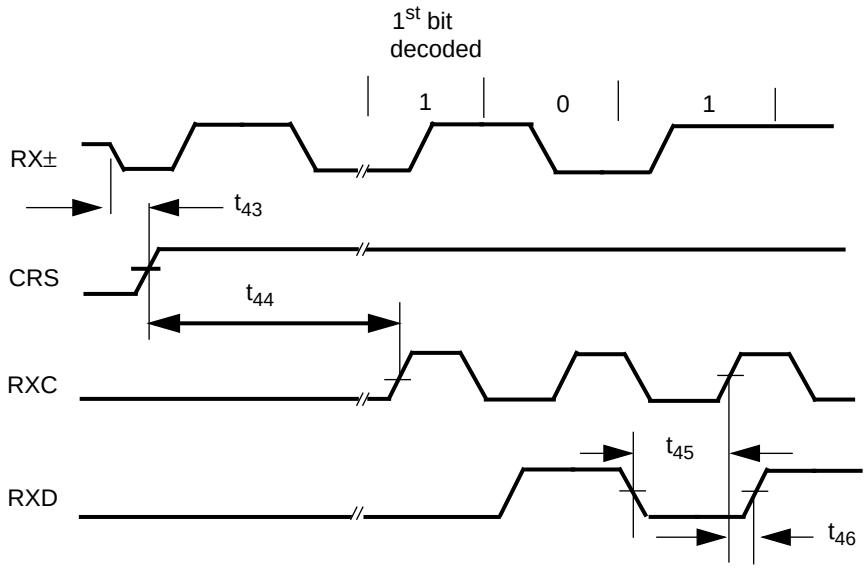
AUI End of Packet Transmit Timing



Symbol	Parameter	Min	Max	Units
t_{40}	TXE Hold Time from TXC Rising Edge	5		ns
t_{41}	TX± End of Packet Hold Time with "0" Ending Bit	200		ns
t_{42}	TX± End of Packet Hold Time with "1" Ending Bit	200		ns

6.0 AC and DC Electrical Specifications (Continued)

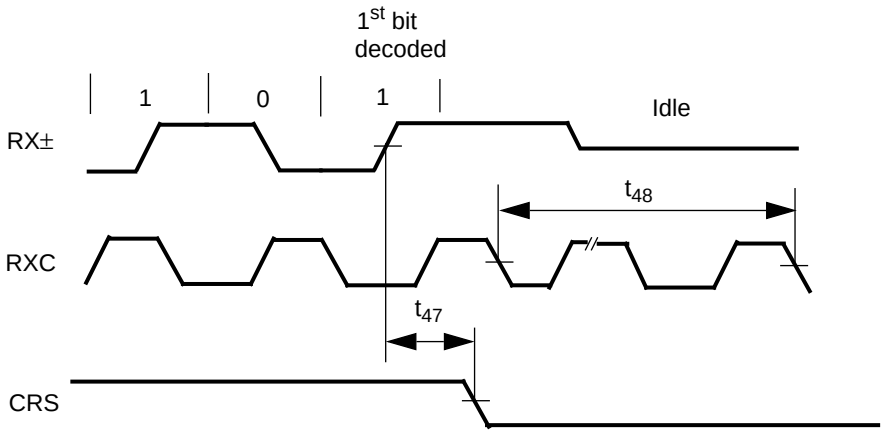
AUI Start of Packet Receive Timing



Symbol	Parameter	Min	Max	Units
t_{43}	Carrier Sense Turn On Delay (RX± to CRS)		200	ns
t_{44}	Decoder Acquisition Time		2200	ns
t_{45}	Receive Data Valid to RXC Rising Edge	25		ns
t_{46}	Receive Data Invalid from RXC Rising Edge	25		ns

6.0 AC and DC Electrical Specifications (Continued)

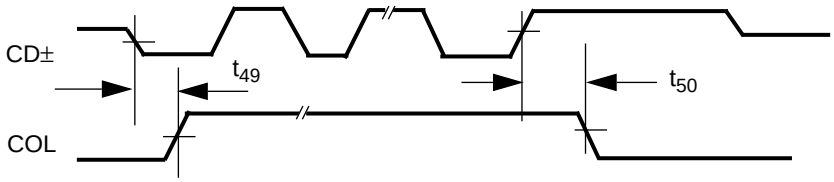
AUI End of Packet Receive Timing



Symbol	Parameter	Min	Max	Units
t_{47}	Carrier Sense Turn Off Delay		400	ns
t_{48}	Number of RXCs after CRS Low (Note 1)	5		Bit Times

Note 1: This only applies when GATERXC, bit D0, in the Global Configuration Register is set.

Collision Specifications



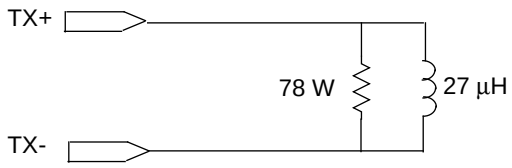
Symbol	Parameter	Min	Max	Units
t_{49}	Collision Turn On Delay (CD± to COL)		600	ns
t_{50}	Collision Turn Off Delay (CD± to COL)		900	ns

6.0 AC and DC Electrical Specifications (Continued)

Network Test Loads

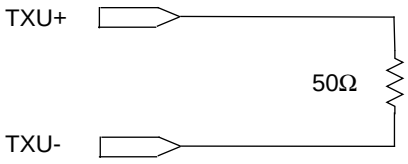
Attachment Unit Interface Load

TX± Output Test Load



TX± is after the secondary side of the transformer.

Twisted Pair Interface Load



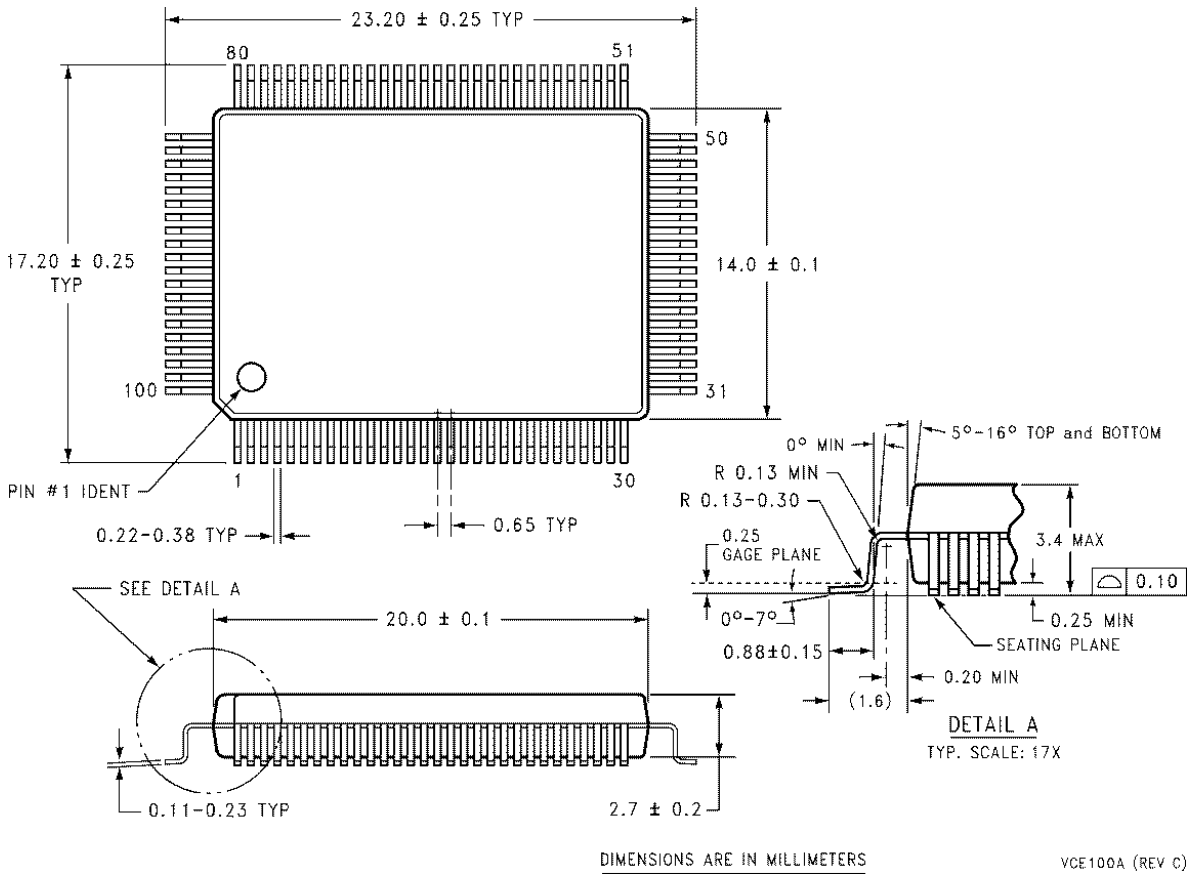
TXU± is after the secondary side of the transformer.

AC Timing Test Condition

All measurement taken with the external transformer in place.

Reference	Limits
Input Levels (Digital Pins, $t_R = t_F = 3ns$)	0V - 3.0V
Input/Output Reference Levels (Digital Pins)	1.5V
Differential Input Reference Levels	2.0 Vp-p
Differential Input/Output Reference Levels	50% of Differential

7.0 Physical Dimensions inches (millimeters) unless otherwise noted



Molded Plastic Quad Flat Package, JEDEC
Order Number DP83924AVCE
NS Package Number VCE100A

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