National Semiconductor

PRELIMINARY
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DP84900 1,7 Encoder/Decoder Circuit

General Description

The DP84900 is designed to perform the encoding and decoding for disk memory systems. It is designed to interface directly with National Semiconductor's integrated read channel circuits such as the DP8492. This Encoder/Decoder (ENDEC) circuit employs a 2/3 (1,7) Run Length Limited (RLL) code type and supports hard sectored format.

The ENDEC also includes write data precompensation circuitry which detects the need for precompensation. This circuitry issues early, late and level (PCOMP3T) output signals necessary for two levels of precompensation. Precompensation information is generated against both the 2T and 3T patterns. The precompensation circuitry can be bypassed by the setting of a bit in the control register.

A control register is included to configure the ENDEC and to select several device operation options such as output code inversion and TRI-STATE® of the NRZ output.

The DP84900 is available in a 20-pin SO and SSO package.

Features

- Operates at Non-Return to Zero (NRZ) data rates up to 25 Mbits/second
- Single +5V power supply operation
- Low Power dissipation—110 mW at 25 Mbits/sec NRZ rate
- TTL compatible inputs and outputs
- Supports write data precompensation with Early, Late and Level (PCOMP3T) output signals
- Power Down Mode included
- DC-erasure is available to support analog flaw map testing
- Bypass mode available which permits un-encoded test patterns to be issued at the CODEOUT pin

Block Diagram

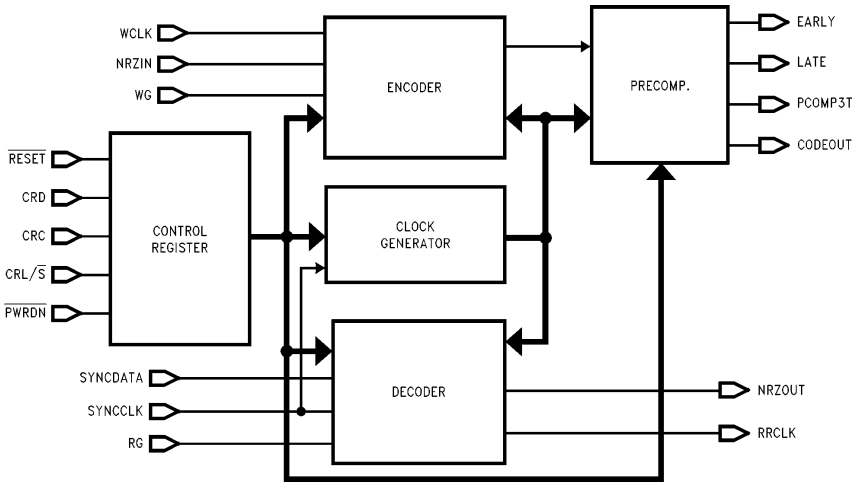

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FIGURE 1. ENDEC Block Diagram

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
IBM® is a registered trademark of International Business Machines Corporation.

Connection Diagram

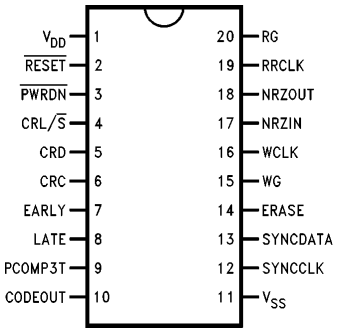

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FIGURE 2

DP84900 Pinout
Order Number DP84900M or DP84900MS
See NS Package Number M20B or MSA20

Pin Description for the DP84900

POWER SUPPLY PINS

Pin 1 V_{DD}: 5V ±10%

Pin 11 V_{SS}: Ground reference

INPUT PIN DESCRIPTIONS

Pin 2 $\overline{\text{RESET}}$: A logical low level applied to this input puts the ENDEC into a known state. This ENDEC does not power up in known or set states. During normal operation, this pin must be held at a high logical level.

Pin 3 $\overline{\text{Power Down}}$ ($\overline{\text{PWRDN}}$): When this input is set to a logical low state, the device is powered down and all clocks are disabled. The content of the control register does not change from previously entered data.

Pin 4 Control Register Latch/$\overline{\text{Shift}}$ (CRL/$\overline{\text{S}}$): A logical low state applied to this input allows the CONTROL REGISTER CLOCK input to clock data into the control register via the CONTROL REGISTER DATA input. A logical high state latches the data into a bank of latches and issues the information to the appropriate circuitry within the ENDEC.

Pin 5 Control Register Data (CRD): Control register data input.

Pin 6 Control Register Clock (CRC): Positive-edge-active control register clock input.

Pin 12 Synchronized Clock (SYNCCLK): This input accepts code rate (1.5F) synchronized clock signal from the read channel's data synchronizer. This signal is used to clock the synchronized data into the decoder on the negative edge of SYNCCLK in the read mode and is the source clock for clocking codeout from the encoder during the write mode.

Pin 13 Synchronized Data (SYNCDATA): This input accepts the synchronized data signal from the read channel's data synchronizer for the decoder's use.

Pin 14 Erase: This active high input is used while in the write mode to force a logical low at the CODEOUT output. This is useful to blank out (write all lows or all highs) a track for analog flaw map testing.

Pin 15 Write Gate (WG): This input accepts a mode control signal from the controller for the encoder. It permits the writing of header and data to the disk when at a logical high level and prohibits writing when at a logical low level. There are no set-up or hold timing requirements for the enabling or disabling of WRITE GATE.

Pin 16 Write Clock (WCLK): This input accepts the NRZ data rate (1F) clock signal from the controller and is used to strobe the NRZ INPUT data into the ENDEC. This signal must be the READ/REFERENCE CLOCK echoed by the controller.

Pin 17 NRZ Input (NRZIN): This input accepts the NRZ data signal from the controller. Data is strobed into the ENDEC on the positive edge of the WRITE CLOCK, encoded and written to the disk in (1,7) format. The NRZ input must be held low while the preamble and address mark fields are being written. The data encoding begins at the occurrence of the first NRZ ''one'' bit.

Pin 20 Read Gate (RG): This input accepts a mode control signal from the controller for the decoder's use, active high for a read operation. There are no set-up or hold timing restrictions for enabling or disabling of READ GATE.

OUTPUT PIN DESCRIPTIONS

Pin 7 Early: This pin is the early precompensation output. It issues a logical high level to indicate that early precompensation is needed. This signal is used by the National Semiconductor integrated read channel chip, such as the DP8492, to precompensate the final coded data before it goes to the read/write head.

Pin 8 Late: This pin is the late precompensation output. It issues a logical high level to indicate that late precompensation is needed. This signal is used by the National Semiconductor integrated read channel chip, such as the DP8492, to precompensate the final coded data before it goes to the read/write head.

Pin 9 PCOMP3T: This pin is the precompensation level output. This output acts as a switch to the supply line. When precompensation for a 3T pattern is needed this output will be at the supply line. When 2T or no precompensation is needed this output will be tristated.

Pin 10 (1,7) RLL Code Output (CODEOUT): This output issues encoded data to be written to the disk. The control register controls various attributes of this output. The sense of the output can be selectively inverted to allow the active edge to be either the positive or negative transition. It can be tristated which allows the multiplexing of this pin with another device or pin. The precompensation circuitry can be bypassed. The encoder can also be bypassed thus permitting un-encoded test patterns to be issued from this pin.

Pin 18 NRZ Output (NRZOUT): This output issues decoded NRZ data to the controller during a read operation. NRZOUT data will be clocked into the controller on the positive edge of the READ/REFERENCE CLOCK. It can be tristated in write mode by setting the appropriate bit within the control register. This allows the NRZIN and NRZOUT pins to be tied together as a single, bidirectional port.

Pin 19 Read/Reference Clock (RRCK): This output issues NRZ data rate (1F) clock to the controller at all times. This signal is used to clock decoded NRZ data into the controller in read mode (READ CLOCK), and is to be echoed back to the ENDEC by the controller in write mode for use as a write clock (REFERENCE CLOCK). READ CLOCK is derived from the clock generator circuit in the ENDEC.

DC and AC Device Specifications

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
TTL Input Maximum Voltage	7V
Maximum Output Voltage	7V
ESD Susceptibility	2000V (Note 1)

Note 1: Human body model is used. (100 pF through 1.5 kΩ)

General Operating Conditions (Note 1)

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply Voltage	4.5	5	5.5	V
T_A	Operation Ambient Temperature	0		70	°C
T_S	Storage Temperature	−65		150	°C
I_{OH}	High Logic Level Output Current			−8	mA
I_{OL}	Low Logic Level Output Current			8	mA
V_{IH}	High Logic Level Input Voltage	2			V
V_{IL}	Low Logic Level Input Voltage			0.8	V
C_{LOAD}	Capacitive Load on any TTL Output			25	pF
f_{NRZ}	NRZ Transfer Rate Operating Frequency	5		25	Mb/s
f_{SCLK}	SYNC CLK Operating Frequency			37.5	MHz
$t_{PW(RESET)}$	RESET Pulse Width (negative)	5			SYNCCLK PERIODS
$t_{PW(PWRDN)}$	PWRDN Pulse Width (negative)	5			SYNCCLK PERIODS
$t_{W(RG,WG)}$	RG or WG Wait Time After Power Down or Reset		5		SYNCCLK PERIODS

Note 1: Guaranteed over recommended free air temperature and supply voltage range (unless otherwise specified).

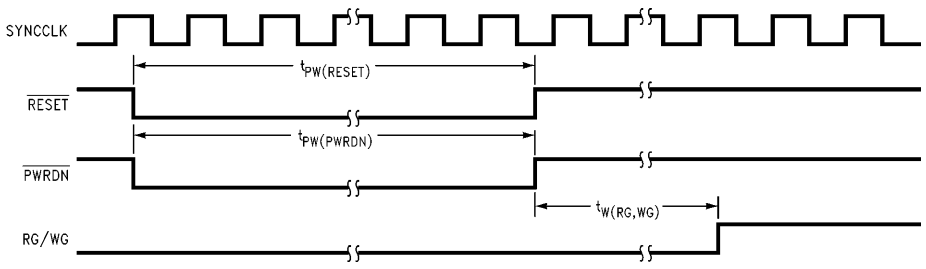

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FIGURE 3. Reset and Powerdown Pin Timing Diagram

Control Register Operating Conditions (Note 1)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PW(CRC)}$	CRC Pulse Width (positive or negative)	40			ns
$t_{SU(CRD)}$	CRD setup time w.r.t. CRC (positive edge)	20			ns
$t_{H(CRD)}$	CRD hold time w.r.t. CRC (positive edge)	10			ns
$t_{SU(CRL/\overline{S})}$	CRL/$\overline{S}$ setup time w.r.t. CRC (positive edge)	20			ns
$t_{H(CRL/\overline{S})}$	CRL/$\overline{S}$ hold time w.r.t. CRC (positive edge)	25			ns

Note 1: Parameters guaranteed to operate over free air temperature and supply voltage range (unless otherwise specified) by design or correlation data. No outgoing tests are performed.

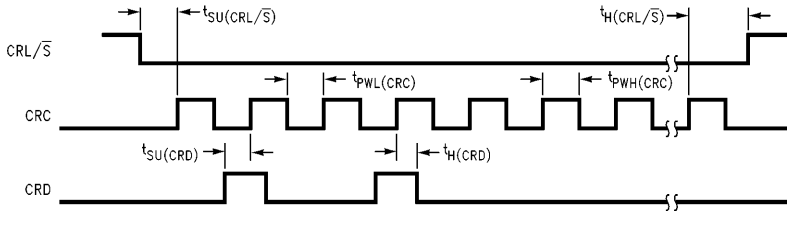


FIGURE 4. Control Register Timing Diagram

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High Logic Level Output Voltage	V_{DD} = Min, $\lvert I_{OH} \rvert$ = 10 mA	PCOMP3T	V_{CC} − 0.4			V
		V_{DD} = Min, $\lvert I_{OH} \rvert$ = 20 μA	Others	V_{CC} − 0.1			
		V_{DD} = Min, $\lvert I_{OH} \rvert$ = Max		3.5			
V_{OL}	Low Logic Level output Voltage	V_{DD} = Min, $\lvert I_{OL} \rvert$ = 20 μA				0.1	V
		V_{DD} = Min, $\lvert I_{OL} \rvert$ = Max				0.4	V
I_{IN}	Input Current	V_{DD} = Max		−20		20	μA
I_{OZ}	TRI-STATE Output Current	V_{DD} = Max		−20		20	μA
I_{DD}	Supply Current	V_{DD} = Max, f_{NRZ} = 25 Mb/s			20		mA
$I_{DD(PD)}$	Supply Current in Power Down Mode	V_{DD} = Max			5		mA

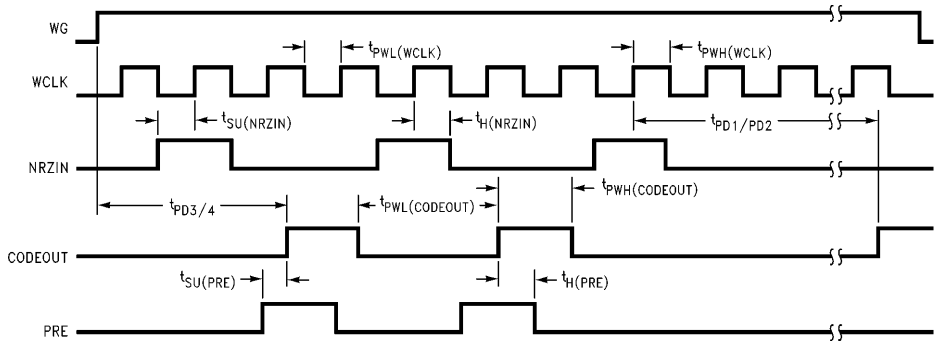
Note 1: Guaranteed over recommended operating free air temperature and supply voltage range (unless otherwise specified).

Write Mode

AC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{SU(NRZIN)}$	NRZIN Setup Time w.r.t. WCLK (positive edge)		8			ns
$t_{H(NRZIN)}$	NRZIN Hold Time w.r.t. WCLK (positive edge)		8			ns
t_{PD1}	Propagation Delay of Encoder, WCLK (positive edge) to CODEOUT (positive edge)	Precompensation enabled	11	12	13	WCLK PERIODS
t_{PD2}	Propagation Delay of Encoder, WCLK (positive edge) to CODEOUT (positive edge)	Precompensation disabled	7	8	9	WCLK PERIODS
t_{PD3}	Propagation Delay of Encoder, WG (positive edge) to First Valid CODEOUT output	Precompensation enabled		13		SYNCCLK PERIODS
t_{PD4}	Propagation Delay of Encoder, WG (positive edge) to First Valid CODEOUT output	Precompensation disabled		7		SYNCCLK PERIODS
$t_{SU(EARLY)}$	EARLY Setup Time w.r.t. CODEOUT (positive edge)		10			ns
$t_{H(EARLY)}$	EARLY Hold Time w.r.t. CODEOUT (positive edge)		10			ns
$t_{SU(LATE)}$	LATE Setup Time w.r.t. CODEOUT (positive edge)		10			ns
$t_{H(LATE)}$	LATE Hold Time w.r.t. CODEOUT (positive edge)		10			ns
$t_{SU(PCOMP3T)}$	PCOMP3T Setup Time w.r.t. CODEOUT (positive edge)		10			ns
$t_{H(PCOMP3T)}$	PCOMP3T Hold Time w.r.t. CODEOUT (positive edge)		10			ns
$t_{PW(CODEOUT)}$	CODEOUT Pulse Width (High or Low)			1		SYNCCLK PERIODS
$t_{PW(WCLK)}$	WCLK Pulse Width (High or Low)		8			ns

Note 1: Guaranteed over recommended operating free air temperature and supply voltage range (unless otherwise specified).



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PRE = EARLY, LATE or PCOMP3T Signals

FIGURE 5. Write Timing Diagram

Read Mode

AC Electrical Characteristics (Note I)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{SU(SYCDAT)}$	SYNCDATA Setup Time w.r.t. SYNCCLK (negative edge)		10			ns
$t_{H(SYCDAT)}$	SYNCDATA Hold Time w.r.t. SYNCCLK (negative edge)		−1			ns
$t_{PW(NRZOUT)}$	NRZOUT Pulse Width (High or Low)			1		RRCLK PERIODS
$t_{SU\ (NRZOUT)}$	NRZOUT Setup Time w.r.t. RRCLK (positive edge)		8			ns
$t_{H(NRZOUT)}$	NRZOUT Hold Time w.r.t. RRCLK (positive edge)		8			ns
t_{PD5}	Propagation Delay of Decoder, SYNCCLK (negative edge) to RRCLK		4			RRCLK PERIODS
$t_{PW(RRCLK)}$	RRCLK Pulse Width (High or Low)		(Note 2)			ns

Note 1: Guaranteed over recommended operating free air temperature and supply voltage range (unless otherwise specified).

Note 2: Minimum pulse width = (smaller half cycle of SYNCCLK) + 2 ns.

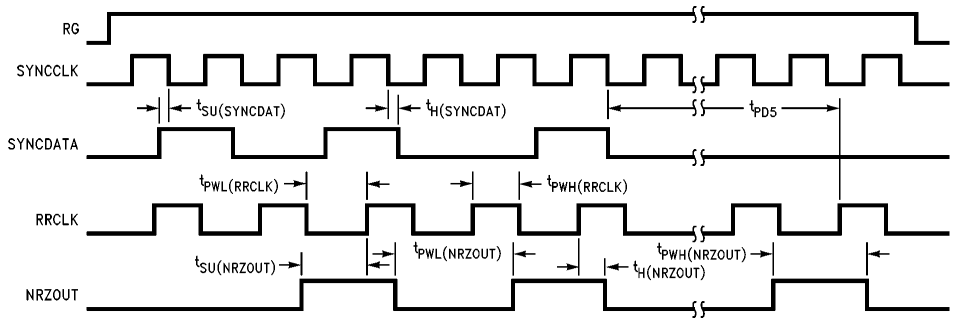

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FIGURE 6. Read Timing Diagram

Functional Description

The Encoder/Decoder (ENDEC) translates NRZ data to and from the (1,7) RLL format; indicates the need to precompensate write data and issues READ/REFERENCE CLOCK (RRCK). The multiplexing of the RRCK is done without glitches.

1,7 RLL CODE

The (1,7) code used is based on US patent #4,413,251 via cross-licensing with International Business Machines Corporation (IBM®). Table 1 summarizes the decoding method used for this device. Nine SYNCDATA bits are used to decode the first three SYNCDATA bits of the nine bit stream into two NRZ bits, a Most Significant Bit (MSB) and a Least Significant Bit (LSB). Bit 8 is the first SYNCDATA bit shifted into the decoder. The leftmost column of the table identifies whether the row represents the NRZ MSB or LSB. This table identifies the combinations which will produce a high logical level. If the code bits do not match the table, a low logical state will be produced.

Functional Description (Continued)

TABLE 1. Decoding Table

NRZOUT Bit	SYNCDATA (CODE BITS)								
	8	7	6	5	4	3	2	1	0
LSB = 1	X	X	X	1	X	X	X	X	X
LSB = 1	X	X	X	X	0	0	X	X	X
MSB = 1	X	X	X	0	X	1	X	X	X
MSB = 1	X	X	X	1	X	1	X	X	X
MSB = 1	X	X	0	0	0	X	X	X	X
MSB = 1	X	X	X	X	1	X	0	0	0
MSB = 1	X	X	X	1	X	X	0	0	0

Table 1.5 summarizes the state diagram used by this device to encode NRZIN data into 1,7 coded data. The table is read from left to right during the encoding process. To encode data the ''CURRENT STATE'' (column 1) must be determined first. The initial ''CURRENT STATE'' is always zero. This ''CURRENT STATE'' selects a group of four rows in the table. The two NRZIN bits determine the exact row, within the group, to be used. Once the row is identified, follow the row to the right of the ''NRZIN'' column to locate the coded output, in the ''1,7 OUT'' column. Continue by identifying the next state in the ''NEXT STATE'' column immediately to the right of the ''1,7 OUT'' column. The number located in this column is used as the ''CURRENT STATE'' for the next two NRZIN bits. This procedure is continued until all the NRZ data is encoded.

TABLE 1.5. Encoding Table

NRZIN			CODEOUT			
Current State	MSB	LSB	1,7 Out			Next State
0	0	0	0	1	0	0
0	0	1	0	1	0	2
0	1	0	0	1	0	4
0	1	1	0	1	0	3
1	0	0	0	0	0	0
1	0	1	0	0	0	2
1	1	0	0	0	0	4
1	1	1	0	0	0	3
2	0	0	1	0	0	0
2	0	1	1	0	0	2
2	1	0	1	0	0	4
2	1	1	1	0	0	3
3	0	0	1	0	1	0
3	0	1	1	0	1	1
3	1	0	1	0	1	4
3	1	1	1	0	0	1
4	0	0	0	0	1	0
4	0	1	0	0	1	1
4	1	0	0	0	1	4
4	1	1	0	1	0	1

Control Register

The control register is comprised of a nine-bit serial shift register and a nine-bit latch. Information is strobed into the shift register via the CONTROL REGISTER DATA (CRD) input on the positive edge of the CONTROL REGISTER CLOCK (CRC) input with the CONTROL REGISTER LATCH/$\overline{\text{SHIFT}}$ (CRL/$\overline{\text{S}}$) pin at a logical low state. The information is parallel transmitted to the latch bank and the ENDEC when the CRL/$\overline{\text{S}}$ input is taken to a logical high state. The control register truth table describes the functions controlled by each bit in the control register. The bit at the right of each bit stream (8) in the table is the first bit entered into the shift register.

Two bits of the control register (bits 1, 2) control the power down option. The other bits of the control register determine various aspects of the ENDEC's outputs. Bit 3 will enable the tristating of NRZOUT while WG is high. This allows NRZIN and NRZOUT pins to be wired together for single port operation. Bit 4 inverts the sense of CODEOUT data. Bit 6 enables the use of precompensation for 3T spaced bits. If this bit is not selected, the amount of precompensation is set to one level (2T spaced bits). Bits 7 and 8 control bypass selection. No bypass can be selected (bit7 = bit8 = 0), the precompensation circuit can be bypassed (bit8 = 1, bit7 = 0). The encoder can be bypassed (bit8 = 0, bit7 = 1). In this mode the data received at the NRZIN pin will pass through the encoder to the CODEOUT pin without being encoded. This is used to transmit test patterns. The last combination of these bits (bit7 = 1, bit8 = 1) tristate the CODEOUT pin. All reserved bits (0, 5) are to be selected at a logical low level.

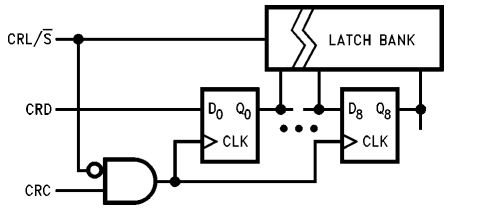

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FIGURE 7. CTRL Register Block Diagram

Precompensation Outputs

The precompensation circuit in the ENDEC generates output data to be used externally to provide write precompensation. The precompensation truth table (Table 3) demonstrates what outputs are expected per data sequence (bit stream). In the table, the bit which is being considered for precompensation is the target bit, T. This target bit is a high logic level. The location of data bits on either side of the target bit dictates the logic states of the precompensation outputs. No shift indicates that all the precompensation outputs are at a logical low level. The mention of a precompensation output in the function column indicates that it is at a logical high level while those not mentioned are at a logical low level.

TABLE 2. Control Register Truth Table

LSB			Bit Stream				MSB		Function Selected
0	1	2	3	4	5	6	7	8	
0	X	X	X	X	X	X	X	X	Reserved Bit
X	0	0	X	X	X	X	X	X	Normal Operation
X	1	1	X	X	X	X	X	X	Power Down
X	X	X	1	X	X	X	X	X	TRI-STATE NRZOUT during a Write operation
X	X	X	X	1	X	X	X	X	Inverts CODEOUT data
X	X	X	X	X	0	X	X	X	Reserved Bit
X	X	X	X	X	X	1	X	X	Enable precompensation for 3T spaced bits
X	X	X	X	X	X	X	0	0	No bypass
X	X	X	X	X	X	X	0	1	Bypass precomp. circuit
X	X	X	X	X	X	X	1	0	Bypass encoder
X	X	X	X	X	X	X	1	1	TRI-STATE CODEOUT pin

TABLE 3. Precompensation Truth Table

MSB			Bit Stream			LSB	Function
0	0	0	T	0	0	0	no shift
1	0	0	T	0	0	1	no shift
x	1	0	T	0	1	x	no shift
1	0	0	T	0	1	x	no shift
x	1	0	T	0	0	1	no shift
1	0	0	T	0	0	0	EARLY, PCOMP3T
x	1	0	T	0	0	0	EARLY
0	0	0	T	0	0	1	LATE, PCOMP3T
0	0	0	T	0	1	x	LATE

The EARLY, LATE, and PCOMP3T outputs need to be connected to inputs of a precompensation circuit to achieve write precompensation. Using the NSC DP8492 device as an example, the EARLY and LATE outputs of the ENDEC will be connected to the EARLY and LATE inputs of the DP8492, respectively. The PCOMP3T output of the ENDEC will be connected to the RPCM input of the DP8492 through a resistor (see *Figure 8*). The amount of precompensation is set by a RC combination at the RPCM input. When the ENDEC indicates that there is a need for precompensation against a 3T pattern (a lesser amount) the PCOMP3T output is switched to the supply rail. This lowers the resistor value of the RC combination by putting the resistor connected between the PCOMP3T output and the RPCM input in parallel with the precompenation resistor connected to the RPCM pin. When the full amount of precompensation is needed (2T pattern) the PCOMP3T output goes to a high impedance state removing the parallel resistor combination.

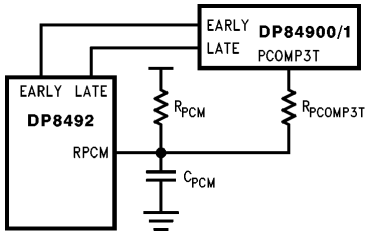

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FIGURE 8. Using PCOMP3T Function

Address Mark Mode

HARD SECTORED READ MODE

The ENDEC supports only a 3T preamble pattern. At the assertion of READ GATE, the decoder searches for 16 uninterrupted code pulses of (3T) preamble. Once the sixteenth bit has been found, lock is detected and phase synchronization will occur. Decoding of 1,7 data will begin after phase synchronization.

HARD SECTORED WRITE MODE

At assertion of WRITE GATE with NRZIN held low, the encoder issues (3T) preamble at the CODEOUT pin. Preamble will continue until the first non-zero NRZ input bit appears. The first NRZ byte must have a leading ''1'', with no restrictions on the remaining 7 bits (i.e., the byte should appear as 1XXXXXXX). The leading ''1'' is required for proper phase synchronization during the decoding operation. No other restrictions are placed upon the incoming NRZ data during the write mode.

Hard Sectored Waveforms

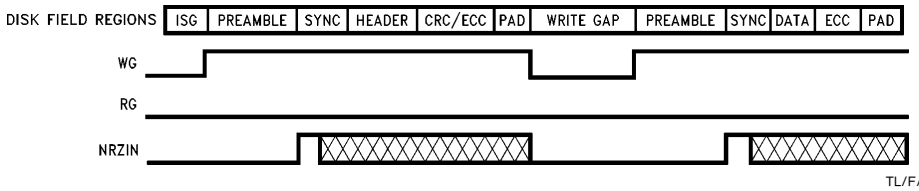

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FIGURE 9. Hard Sectored Write Mode Waveforms

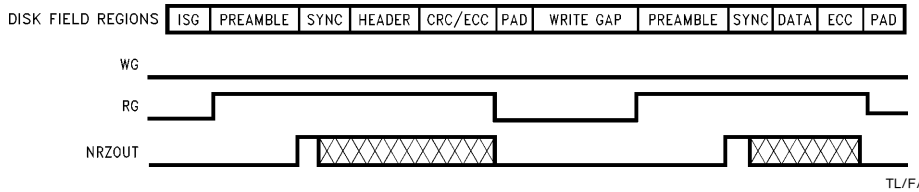

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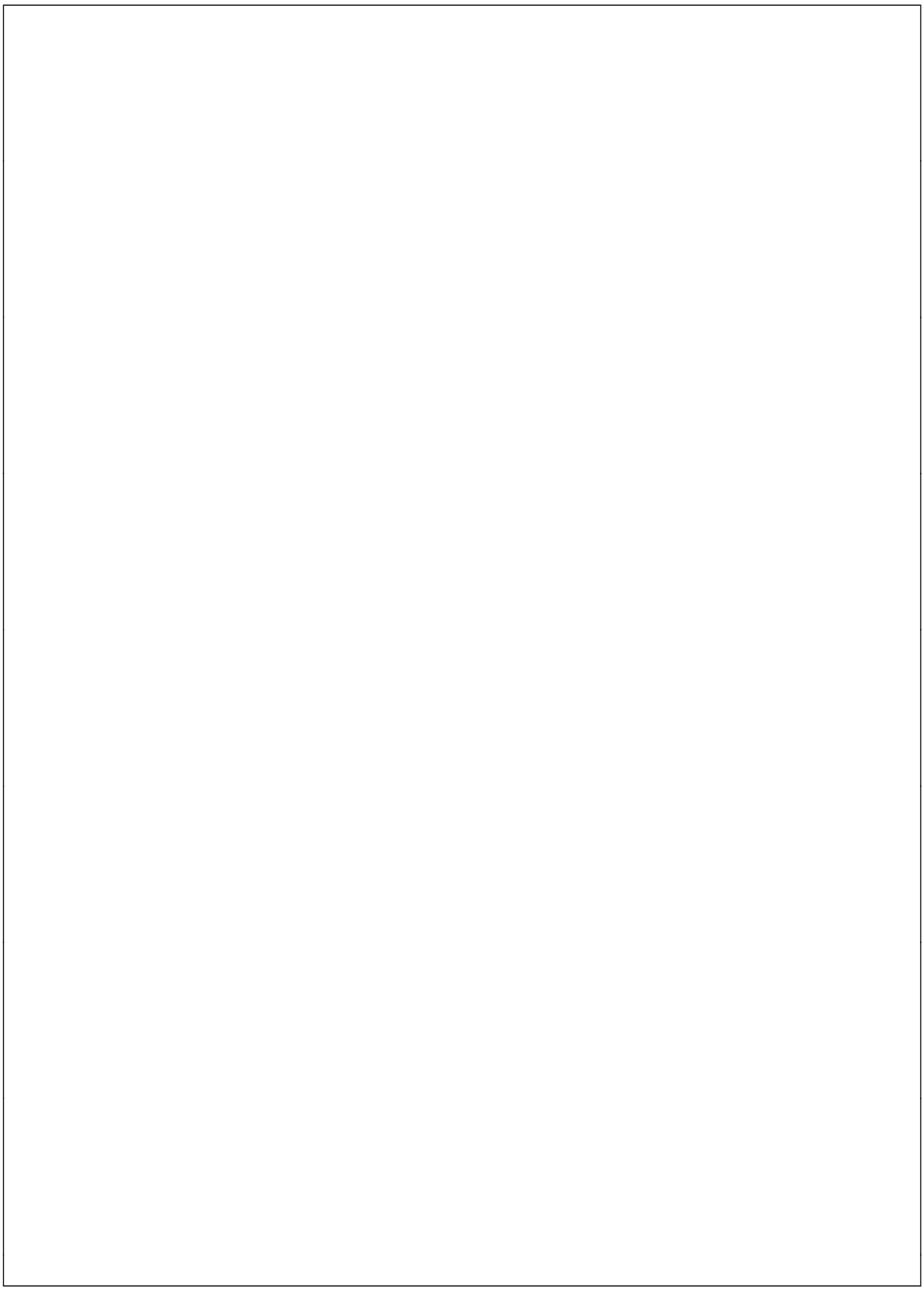
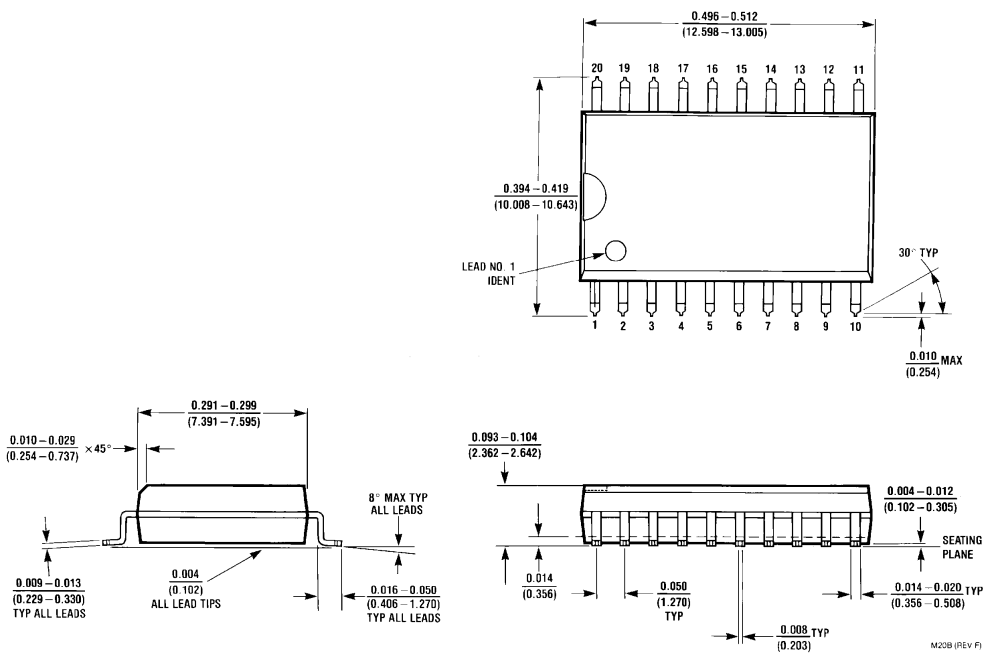
FIGURE 10. Hard Sectored Read Mode Waveforms



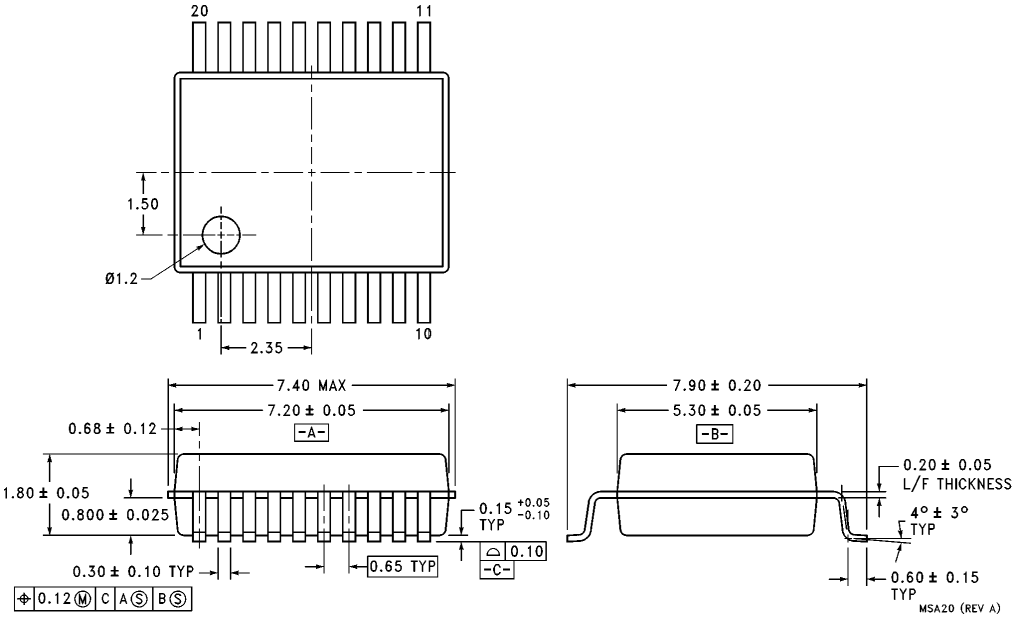
Physical Dimensions inches (millimeters)



20-Pin Small Outline (M)
Package Dimension Diagram
Order Number DP84900M
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114200



20-Pin Shrink Small Outline (MS)
Package Dimension Diagram
Order Number DP84900MS
NS Package Number MSA20

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408