National Semiconductor

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DS1485
High-Speed RS-485/RS-422 Multipoint Transceiver

General Description

The DS1485 is a high-speed low power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The driver's output transition time supports operation up to 40 Mbps while minimizing power consumption.

The transceiver draws 5mA of supply current when unloaded or fully loaded with the driver disabled and operates from a single +5V supply.

The driver is short-circuited current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE® (High Impedance state) under faut conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

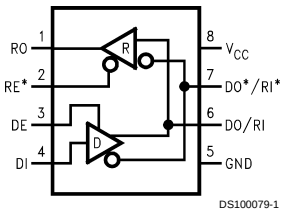
The receiver incorporates a fail safe circuit which guarantees a logic high output state when the inputs are left open. (Note 1)

The DS1485 is available in surface mount and DIP packages and is characterized for Industrial (−40˚C to +85˚C) and Commercial temperature range operation.

Features

- Meets TIA/EIA RS-485 Multipoint Standard
- Supports 40 Mbps operation
- Guaranteed Full Load Output Voltage (V_{OD3})
- Low Quiesent Current 5mA typ
- −7V to +12V Common−Mode Input Voltage Range
- TRI-STATE Outputs on Driver and Receiver
- AC Performance:
  - Driver Transition Time 3ns typ
  - Driver Propagation Delay 7ns typ
  - Driver Skew 0.2ns typ
  - Receiver Propagation Delay 3ns typ
  - Receiver Skew 0.3ns typ
- Half−Duplex Flow Through Pinout
- Operates from a single 5V supply
- Allows up to 32 Transceivers on the Bus
- Current−Limiting and Thermal Shutdown for Driver Overload Protection
- Industrial temperature range: −40˚C to +85˚C
- ±10kV ESD (human body model) Protection on Bus Pins
- Pin and Functional Compatibility with ADM1485, MAX485, LTC1485, SN75LBC176 and SN75ALS176B

Connection and Logic Diagram



DS100079-1

Order Number DS1485TM, DS1485TN, DS1485M, DS1485N
See NS Package Number M08A or N08E

Truth Table

DRIVER SECTION				
RE*	**DE**	**DI**	**DO/RI**	**DO*/RI***
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE*	**DE**	**RI−RI***		**RO**
L	L	≥ +0.2V		H
L	L	≤ −0.2V		L
H	L	X		Z
L	L	OPEN (Note 1)		H

Note 1: Non-terminated, open input only

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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7V
Input Voltage (DE, RE*, & DI) −0.5V to (V_{CC} +0.5V)
Common Mode (V_{CM})
Driver Output/Receiver Input −10V to +15V
Input Voltage (DO/RI, DO*/RI*) −10V to +15V
Receiver Output Voltage (RO) −0.5V to (V_{CC} +0.5V)
Maximum Package Power Dissipation @ +25˚C
M Package TBD mW, derate TBD mW/˚C above +25˚C
N Package TBD mW, derate TBD mW/˚C above +25˚C
Storage Temperature Range −65˚C to +150˚C
Lead Temperature
(Soldering 4 sec) +260˚C
ESD (HBM) ≥ 10kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Bus Voltage	−7		+12	V
Operating Free Air Temperature (T_A)				
DS1485	0	25	+70	˚C
DS1485T	−40	25	+85	˚C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified ((Note 3) and (Note 4))

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage−Unloaded	I_O = 0 mA (No Load)	DO/RI, DO*/RI*	1.5		5.0	V
V_{OD2}	Differential Driver Output Voltage with load	R_L = 50Ω (RS−422), *Figure 1*		2.0	TBD		V
		R_L = 27Ω (RS−485), *Figure 1*		1.5	TBD	5.0	V
ΔV_{OD}	Change in Magnitude of Output Differential Voltage	R_L = 27Ω or 50Ω, *Figure 1* (Note 5)		−0.2		+0.2	V
V_{OD3}	Differential Driver Output Voltage (Full Load w/max V_{CM})	R1 = 54Ω, R2 = 375Ω V_{TEST} = −7V to +12V, *Figure 2*		1.5	TBD	5.0	V
V_{OC}	Driver Common Mode Output Voltage	R_L = 27Ω or 50Ω, *Figure 1*		−1	TBD	3.0	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	R_L = 27Ω or 50Ω, *Figure 1* (Note 5)		−0.2		+0.2	V
V_{IH}	High Level Input Voltage		DE, RE*, DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN1}	Input Current	V_{IN} = 0V or V_{CC}				±1	µA
I_{IN2}	Input Current (Note 6) DE = 0V, V_{CC} = 0V or 5.5V	V_{IN} = +12V	DO/RI, DO*/RI*			1.0	mA
		V_{IN} = −7V				−0.8	mA
V_{TH}	Receiver Differential Threshold Voltage	−7V ≤ V_{CM} ≤ +12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage	I_{OH} = −4 mA, V_{ID} = +0.2V *Figure 11*	RO	4.0			V
V_{OL}	Receiver Output Low Voltage	I_{OL} = +4 mA, V_{ID} = −0.2V *Figure 11*				0.4	V
I_{OZR}	Receiver TRI-STATE Leakage Current	V_O = 0.4V to 2.4V				±1	µA
R_{IN}	Receiver Input Resistance	−7V ≤ V_{CM} ≤ +12V	DO/RI, DO*/RI*	TBD			kΩ
I_{CC}	Power Supply Current (No Load) (Note 7)	DE = V_{CC}, RE = 0V	V_{CC}		TBD	5	mA
I_{CCR}		DE = 0V, RE = 0V			TBD	5	mA
I_{CCD}		DE = V_{CC}, RE = V_{CC}			TBD	5	mA
I_{CCZ}		DE = 0V, RE = V_{CC}			TBD	5	mA
I_{OSD}	Driver Output Short-Circuit Current	V_O = +12V (RS−485), *Figure 4*	DO/RI, DO*/RI*	35		+250	mA
		V_O = −7V (RS−485), *Figure 4*		−35		−250	mA
I_{OSR}	Receiver Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	RO	7		85	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. ((Note 4), (Note 8) and (Note 9))

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PHLD}	Driver Differential Propagation Delay High to Low	RL = 54Ω, C_L = 100 pF *Figure 5* and *Figure 6*	over V_{CC}, temp and process		TBD	10	ns
t_{PLHD}	Driver Differential Propagation Delay Low to High				TBD	10	ns
t_{SKEW1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$		@ any specific V_{CC}/temp	0	TBD	1	ns
t_{SKEW2}	Differential Channel−Channel Skew (between devices)		@ any specific V_{CC}/temp (over process)	0	TBD	2	ns
t_{SKEW3}	Complementary Output Skew (Dynamic Common Mode)	difference in propagation delay between outputs at the 50% point		0	TBD		ns
t_r	Driver Rise Time	R_L = 54Ω, C_L = 100 pF		3	TBD	6	ns
t_f	Driver Fall Time	*Figure 5* and *Figure 6*		3	TBD	6	ns
t_{PHZ}	Dr. Disable Time High to Z	C_L = 15 pF, *Figure 7* and *Figure 8*				20	ns
t_{PLZ}	Dr. Disable Time Low to Z	C_L = 15 pF, *Figure 9* and *Figure 10*				20	ns
t_{PZH}	Dr. Enable Time Z to High	C_L = 100 pF, *Figure 7* and *Figure 8*				20	ns
t_{PZL}	Dr. Enable Time Z to Low	C_L = 100 pF, *Figure 9* and *Figure 10*				20	ns
RECEIVER CHARACTERISTICS							
t_{PHL}	Receiver Propagation Delay High to Low	C_L = 15 pF *Figure 12* and *Figure 13*	over V_{CC}, temp and process		TBD	12	ns
t_{PLH}	Receiver Propagation Delay Low to High				TBD	12	ns
t_{SKEW1}	Pulse Skew $\|t_{PHL} - t_{PLH}\|$		@ any specific V_{CC}/temp	0	TBD	1	ns
t_{SKEW2}	Differential Channel−Channel Skew		@ any specific V_{CC}/temp (over process)	0	TBD	2	ns
t_{PLZ}	Rec. Disable Time from Low	C_L = 15 pF			TBD	25	ns
t_{PHZ}	Rec. Disable Time from High	*Figure 14*, *Figure 15* and *Figure 16*			TBD	25	ns
t_{PZL}	Rec. Enable Time to Low				TBD	25	ns
t_{PZH}	Rec. Enable Time to High				TBD	25	ns
f_{MAX}	Maximum Data Rate	(Note 10)		40	TBD		Mbps

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD1}, V_{OD2}, V_{OD3} and V_{ID}.

Note 4: All typicals are given for: V_{CC} = +5.0V, T_A = + 25˚C.

Note 5: Delta $|V_{OD}|$ and Delta $|V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when input changes state.

Note 6: I_{IN2} includes the receiver input current and driver TRI-STATE leakage current.

Note 7: Supply current specification is valid for loaded transmitters when DE = 0V or enabled (DE = H) with no load.

Note 8: f = 1MHz, t_r and $t_f \leq$ 6ns, Z_O=50Ω.

Note 9: C_L includes probe and jig capacitance.

Note 10: f_{MAX} is the guaranteed data rate for 50 ft of twisted pair cable. f_{MAX} may be conservatively determined from the ratio of driver transition time (t_r) to the data rate unit interval ($1/f_{MAX}$). Using a 25% ratio yields f_{MAX}= 6ns/0.25 ~ 40 Mbps. Higher data rates may be supported by allowing larger ratio, or shorter cables.

Parameter Measurement Information

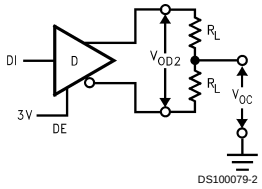


FIGURE 1. Driver V_{OD2} and V_{OC}

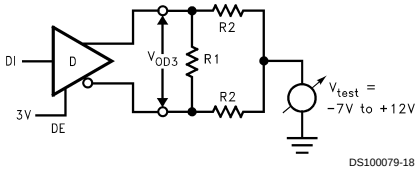


FIGURE 2. Driver V_{OD3}

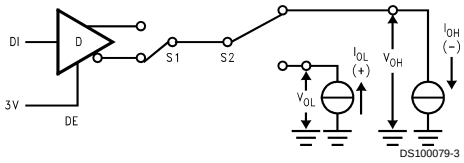
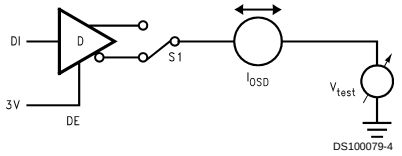


FIGURE 3. Driver V_{OH} and V_{OL}



Vtest = −7V to +12V

FIGURE 4. Driver I_{OSD}

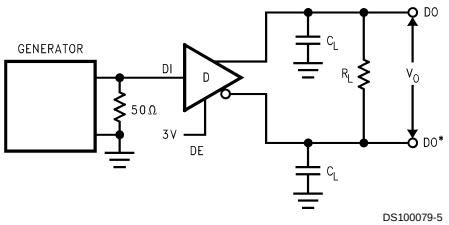


FIGURE 5. Driver Differential Propagation Delay Test Circuit

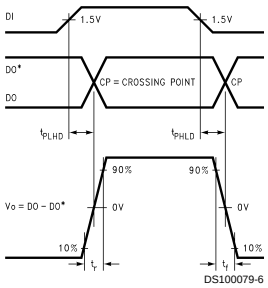


FIGURE 6. Driver Differential Propagation Delays and Differential Rise and Fall Times

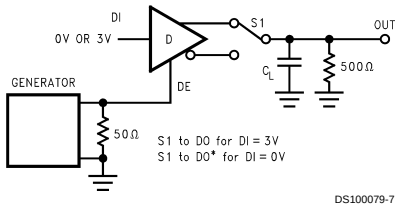


FIGURE 7. TRI-STATE Test Circuit (t_{PZH} , t_{PHZ})

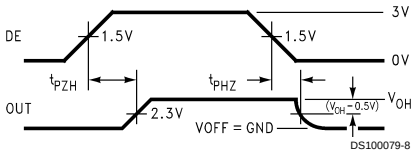


FIGURE 8. TRI-STATE Waveforms (t_{PZH}, t_{PHZ})

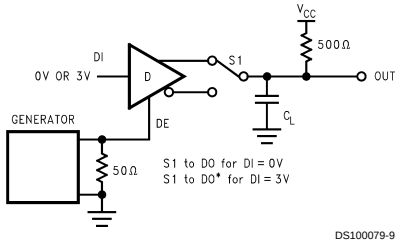


FIGURE 9. TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

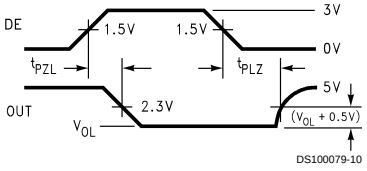


FIGURE 10. TRI-STATE Waveforms (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)

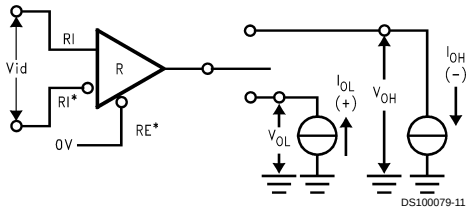


FIGURE 11. Receiver V_{OH} and V_{OL}

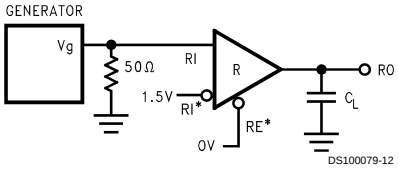


FIGURE 12. Receiver Differential Propagation Delay Test Circuit

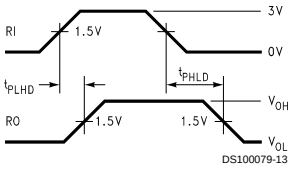


FIGURE 13. Receiver Differential Propagation Delay Waveforms

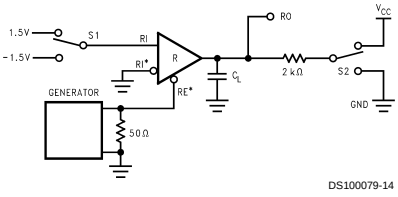


FIGURE 14. Receiver TRI-STATE Test Circuit

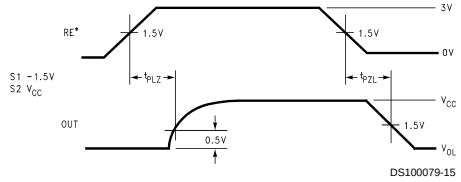


FIGURE 15. Receiver Enable and Disable Waveforms (t_{PLZ}, t_{PZL})

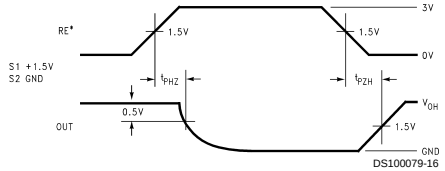


FIGURE 16. Receiver Enable and Disable Waveforms (t_{PHZ}, t_{PZH})

TABLE 1. Device Pin Descriptions

Pin No.	Name	Description
1	RO	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON); if DO/RI ≥ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI ≤ DO*/RI* by 200 mV, RO will be LOW. Additionally, RO will be HIGH for open (non-terminated) inputs.
2	RE*	Receiver Output Enable: When RE* is LOW, the receiver output is enabled. When RE* is HIGH, the receiver output is in TRI-STATE (OFF).
3	DE	Driver Output Enable: When DE is HIGH, the driver outputs (DO/RI and DO*/RI*) are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). Pins DO/RI and DO*/RI* also function as the receiver input pins.
4	DI	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled; if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection.
6	DO/RI	Non-inverting Driver Output/Receiver Input pin. Driver ouput levels conform to RS-485 signaling levels.
7	DO*/RI*	Inverting Driver Output/Receiver Input pin. Driver ouput levels conform to RS-485 signaling levels.
8	V_{CC}	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.5V to +5.5V.

Typical Application Information

Unit Load

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see *Figure 17*). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes. For example, an aircraft that has 32 rows with 4 seats per row would benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS1485 has ½ unit load and ¼ unit load (UL) options available. This device will allow up to 64 nodes or 128 nodes guaranteed over temperature depending upon which option is selected. The ½ UL option is available in industrial temperature and the ¼ UL is available in commercial temperature.

First, for a ½ UL device the top and bottom borders shown in *Figure 17* are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see *Figure 17*). Second, for a ¼ UL device the top and bottom borders shown in *Figure 17* are scaled also. Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see *Figure 17*).

The advantage of the ½ UL and ¼ UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS1485 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

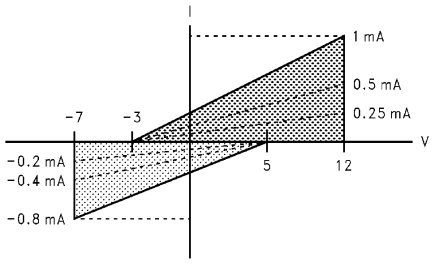
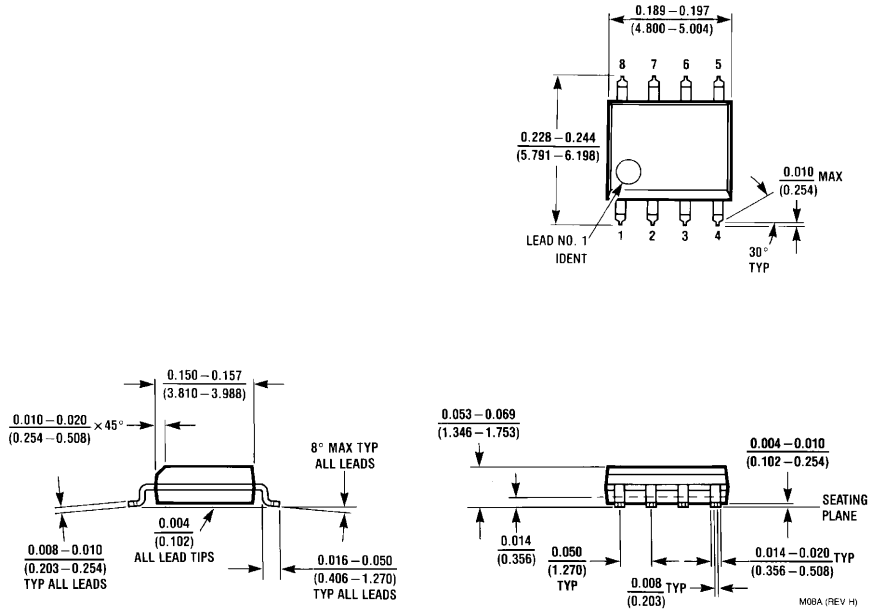
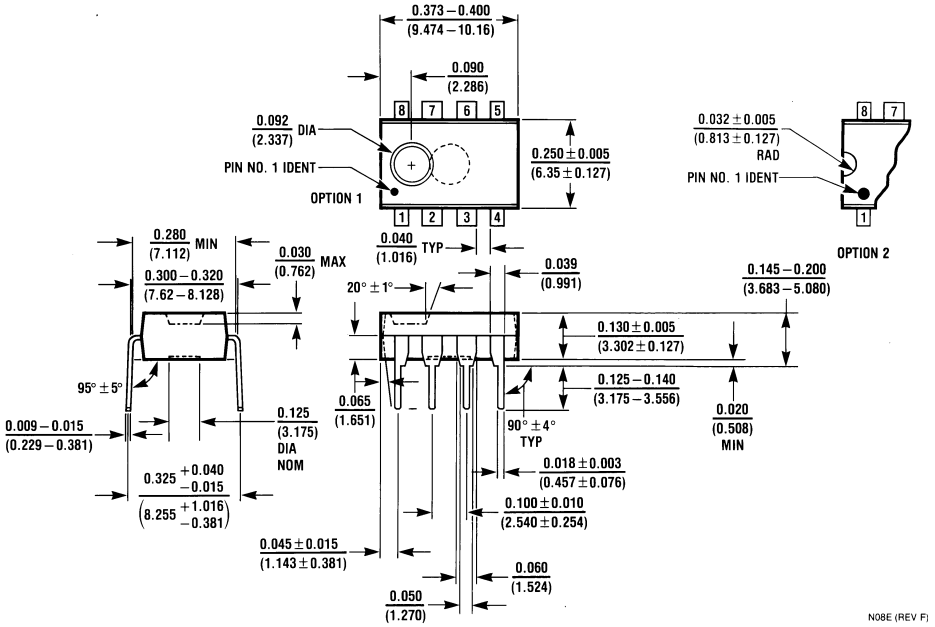


FIGURE 17. Input Current vs Input Voltage Operating Range

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS1485TM, DS1485M
NS Package Number M08A



8-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Number DS1485TN, DS1485N
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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