National Semiconductor

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DP83891 Gig PHYTER®
10/100/1000 Ethernet Physical Layer

General Description

The DP83891 is a full feature Physical Layer transceiver with integrated PMD sublayers to support 10BASE-T,100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83891 is designed for easy implementation of 10/100/1000 Mb/s Ethernet LANs. It interfaces directly to Twisted Pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3u Standard Media Independent Interface (MII) or the IEEE 802.3z Gigabit Media Independent Interface (GMII).

Applications

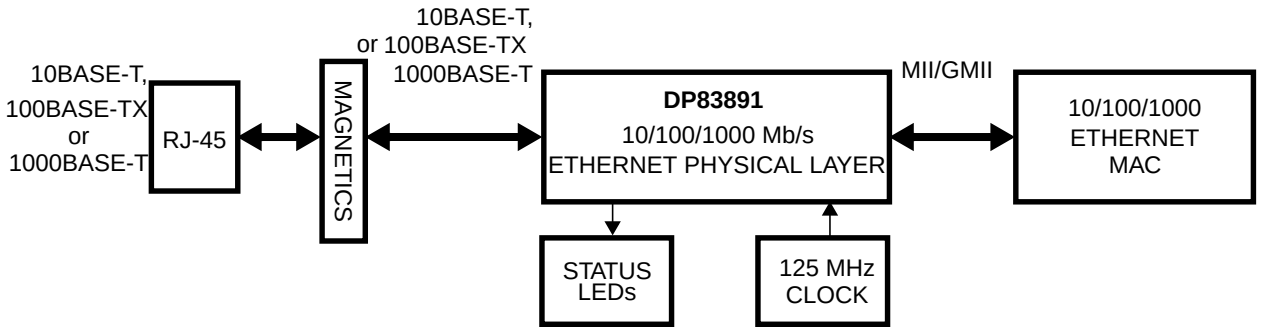
The DP83891 fits applications in:

- 10/100/1000 Mb/s capable node cards
- Switches with 10/100/1000 Mb/s capable ports
- High speed uplink ports (backbone)

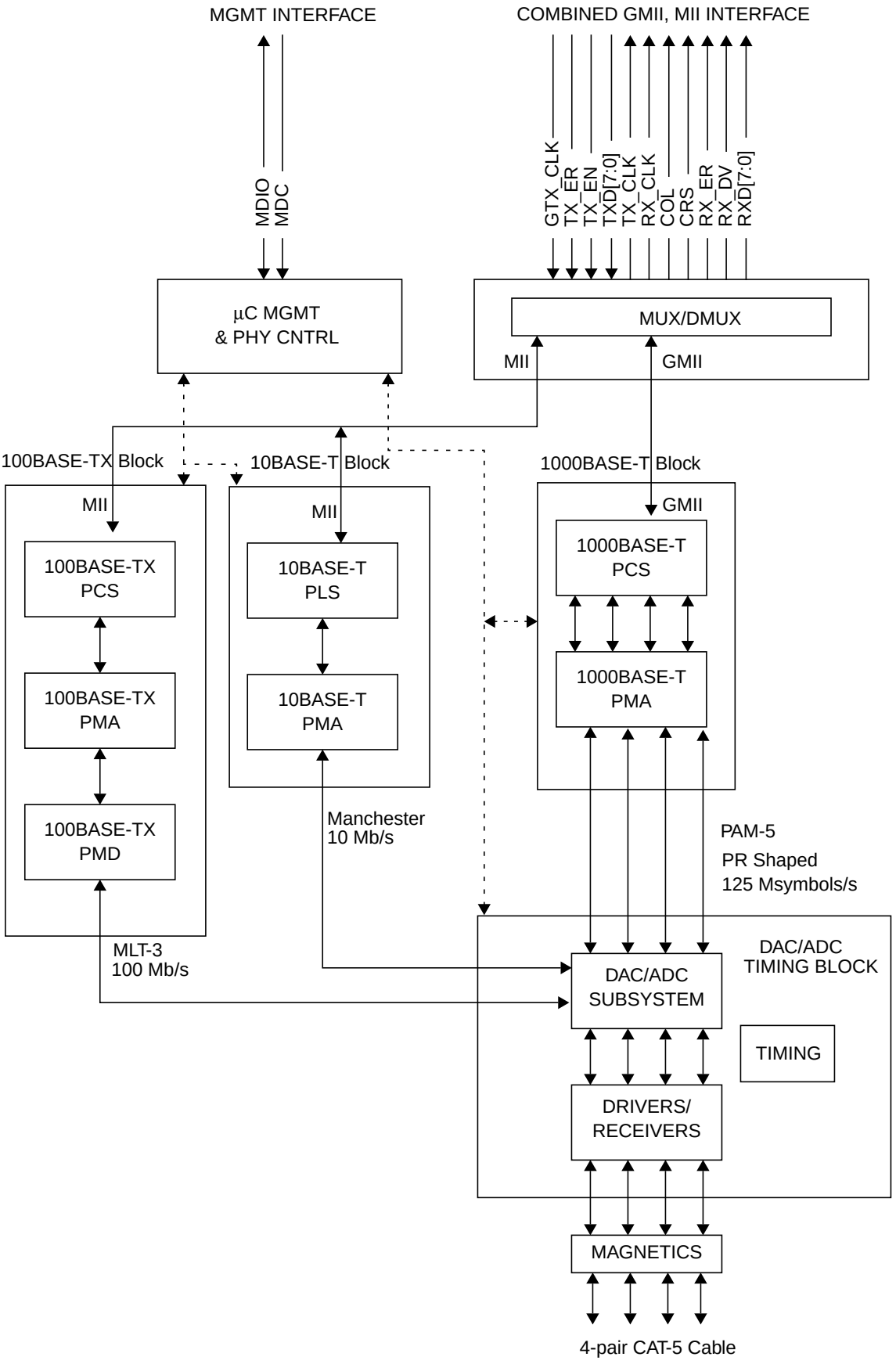
Features

- 10BASE-T,100BASE-TX and 1000BASE-T capable
- Single Quad TX-Transformer interface for all speeds
- Fully compliant to IEEE 802.3u 100BASE-TX and IEEE 802.3z/ab 1000BASE-T specifications. Fully integrated and fully compliant ANSI X3.T12 PMD physical sublayer that includes adaptive equalization and Baseline Wander compensation.
- IEEE 802.3u Auto-Negotiation and Parallel Detection
  - Fully auto-negotiates between 10, 100 and 1000 Mb/s full duplex and half duplex devices
- 3.3V MAC interfaces:
  - IEEE 802.3u MII
  - IEEE 802.3z GMII
- LED support (Link, Speed, Activity, Duplex, Collision, Auto-Negotiation, TX and RX indications)
- Management Register Set
- Single 3.3 V power supply
  - 5V tolerant I/Os
- 208-pin PQFP package

System Diagram



Block Diagram



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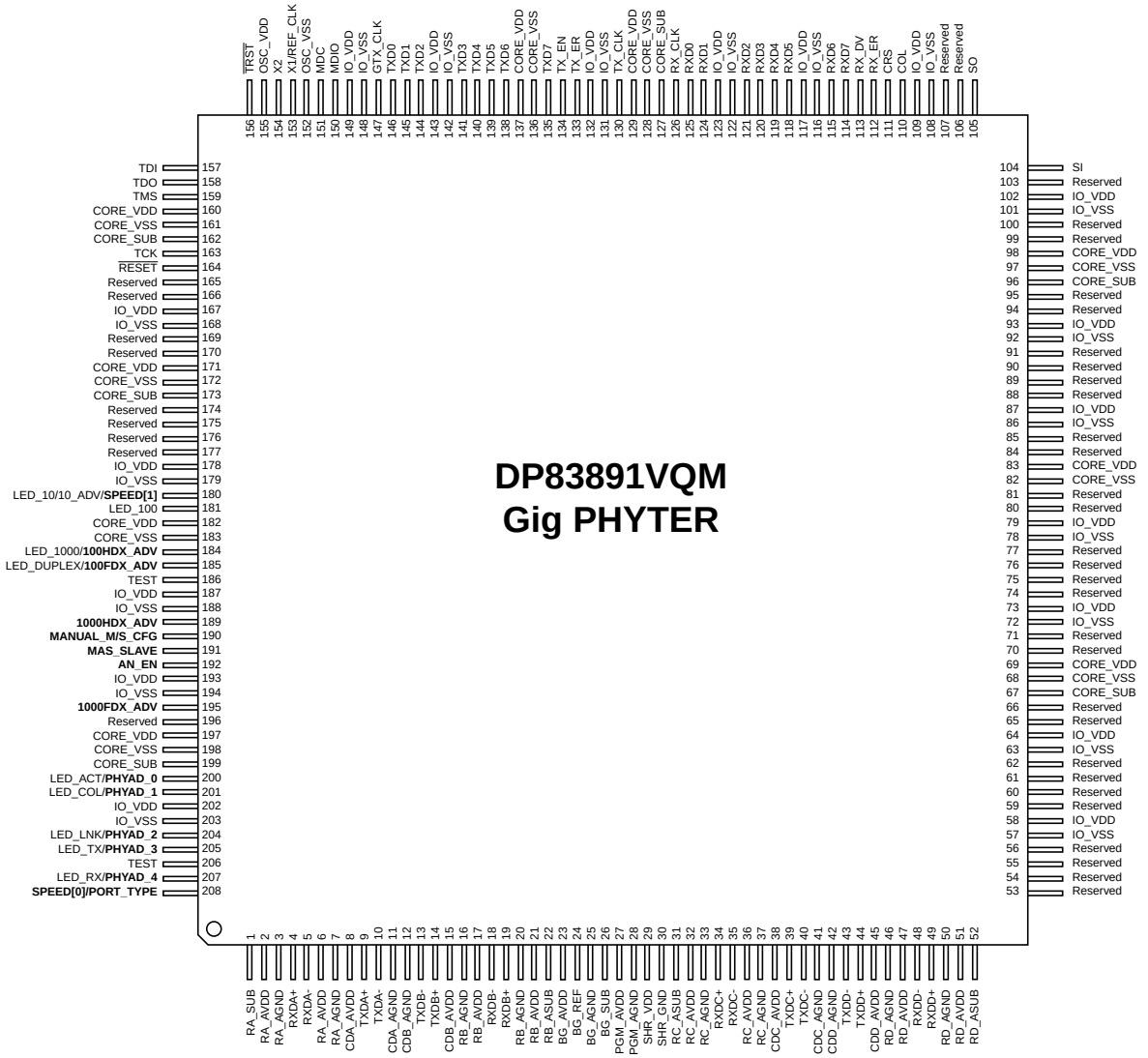
Pin Layout



Bold pin names are strap options (e.g. **AN_EN)**

208 Lead Plastic Quad Flat Pack
Order Number DP83891VQM
NS Package VQM208A

1.0 Pin Description

The DP83891 pins are classified into the following interface categories (each is described in the sections that follow):

— MAC Interface
— TP Interface
— JTAG Interface
— E^2PROM Interface
— Clock Interface
— LED Interface
— Device Configuration / Strapping Options
— Reset
— Power and Ground Pins
— Special Connect Pins

Note: Strapping pin option (**BOLD**) (e.g. **AN_EN**)

Type: I	Inputs
Type: O	Output
Type: O_Z	TRI-STATE Output
Type: I/O_Z	TRI-STATE Input_Output
Type: S	Strapping Pin
Type: PU	Pull-up
Type: PD	Pull-down

1.1 MAC Interface

Signal Name	Type	Pin #	Description
MDC	I	151	**MANAGEMENT DATA CLOCK:** Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz with no minimum clock rate.
MDIO	I/O	150	**MANAGEMENT DATA I/O:** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 1.5 kΩ pullup resistor.
CRS	O	111	**CARRIER SENSE:** Asserted high to indicate the presence of carrier due to receive or transmit activity in Half Duplex mode. This signal is not defined (LOW) for 1000BASE-T Full Duplex mode. For 100BASE-TX full duplex operation CRS is asserted only for receive activity.
COL	O	110	**COLLISION DETECT:** Asserted high to indicate detection of a collision condition (assertion of CRS due to simultaneous transmit and receive activity) in Half Duplex modes. This signal is not synchronous to either MII clock (GTX_CLK, TX_CLK or RX_CLK). This signal is not defined (LOW) for Full Duplex modes.
TX_CLK	O	130	**TRANSMIT CLOCK (100 Mb/s):** Continuous clock signal generated from REF_CLK and driven by the PHY during 100 Mb/s operation. It is used on the MII to clock all MII Transmit (data, error) signals into the PHY. The Transmit Clock frequency is constant and the frequency is 25% of the nominal MII transmit data bit rate for parallel transfers, i.e. 25 MHz for 100BASE-TX.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7	I	146 145 144 141 140 139 138 135	**TRANSMIT DATA:** These signals carry 4B data nibbles (TXD[3:0]) during 100 Mb/s MII mode and 8-bit data (TXD[7:0]) in 1000 Mb/s GMII mode. They are synchronous to the Transmit Clocks (TX_CLK, GTX_CLK). Transmit data is input enabled by TX_EN for all modes, all sourced by the controller.

Signal Name	Type	Pin #	Description
TX_EN	I	134	**TRANSMIT ENABLE:** Active high input driven by the MAC requesting transmission of the data present on the TXD lines (nibble data for 100 Mb/s mode and 8-bit data for 1000 Mb/s GMII mode.)
GTX_CLK	I	147	**GMII-TRANSMIT CLOCK:** This continuous clock signal is sourced from the upper level MAC to the PHY. Nominal frequency of 125 MHz, derived in the MAC from its 125 MHz reference clock, in most applications the same referenced clock used by the PHY.
TX_ER	I	133	**TRANSMIT ERROR:** Active high input during 100 Mb/s nibble mode and 1000 Mb/s GMII mode forcing the PHY to transmit invalid symbols. The TX_ER signal must be synchronous to the Transmit Clocks (TX_CLK and GTX_CLK). In 4B nibble mode, assertion of Transmit Error by the controller causes the PHY to issue invalid symbols followed by Halt (H) symbols until deassertion occurs. In 1000 Mb/s GMII mode, assertion causes the PHY to emit one or more code-groups that are not valid data or delimiter set in the transmitted frame.
RX_CLK	O	126	**RECEIVE CLOCK:** Provides the recovered receive clocks for different modes of operation: 2.5 MHz nibble clock in 10 Mb/s nibble mode 25 MHz nibble clock in 100 Mb/s nibble mode. 125 MHz byte clock in 1000 Mb/s GMII mode.
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7	O	125 124 121 120 119 118 115 114	**RECEIVE DATA:** These signals carry 4-bit data nibbles (RXD[3:0]) during 10/100 Mb/s MII mode and 8-bit data bytes (RXD[7:0]) in 1000 Mb/s GMII mode. They are synchronous to the Receive Clock. (RX_CLK) Receive data is driven by the PHY to the controller, and is strobed by Receive Data Valid (RX_DV) which is also sourced by the PHY.
RX_ER	O	112	**RECEIVE ERROR:** In 100 Mb/s nibble mode and 1000 Mb/s GMII mode this active high output indicates that the PHY has detected a Receive Error. The RX_ER signal must be synchronous with the Receive Clock (RX_CLK).
RX_DV	O	113	**RECEIVE DATA VALID:** Asserted high to indicate that valid data is present on the corresponding RXD[3:0] for 100 Mb/s nibble mode and RXD[7:0] in 1000 Mb/s GMII mode.

1.2 TP Interface

Signal Name	Type	Pin #	Description
TXDA+ TXDA- TXDB- TXDB+ TXDC+ TXDC- TXDD- TXDD+	O	9 10 13 14 39 40 43 44	**TRANSMIT DATA:** The TP Interface connects the DP83891 to the CAT-5 cable through a single common magnetics transformer. The Transmit (TXD) and Receive (RXD) Twisted Pair pins carry bit-serial data at 125 MHz baud rate. These differential outputs are configurable to either 100BASE-TX or 1000BASE-T signalling: 100BASE-TX: Transmission of 3-level MLT-3 data. 1000BASE-T: Transmission of 17-level PAM-5 with PR-shaping data. The DP83891 will automatically configure the common driver outputs for the proper signal type as a result of either forced configuration or Auto-Negotiation. **NOTE:** During 10/100 Mb/s operation only TXDA+ and TXDA- are active. (Transmit only--but see Section 2.12 for automatic crossover configuration.)
RXDA+ RXDA- RXDB- RXDB+ RXDC+ RXDC- RXDD- RXDD+	I	4 5 18 19 34 35 48 49	**RECEIVE DATA:** Differential receive signals. **NOTE:** During 10/100 Mb/s operation only RXDB+ and RXDB- are active (Receive Only--but see Section 2.12 for automatic crossover configuration.)

1.3 JTAG Interface

$\overline{\text{TRST}}$	I	156	**TEST RESET:** IEEE 1149.1 Test Reset pin, active low reset provides for asynchronous reset of the Tap Controller. This reset has no effect on the device registers. This pin should be tied low during regular chip operation.
TDI	I	157	**TEST DATA INPUT:** IEEE 1149.1 Test Data Input pin, test data is scanned into the device via TDI. This pin should be tied low during regular chip operation.
TDO	O	158	**TEST DATA OUTPUT:** IEEE 1149.1 Test Data Output pin, the most recent test results are scanned out of the device via TDO. This pin can be left floating if not used.
TMS	I	159	**TEST MODE SELECT:** IEEE 1149.1 Test Mode Select pin, the TMS pin sequences the Tap Controller (16-state FSM) to select the desired test instruction. This pin should be tied low during regular chip operation.
TCK	I	163	**TEST CLK:** IEEE 1149.1 Test Clock input, primary clock source for all test logic input and output controlled by the testing entity. This pin should be tied low during regular chip operation.

1.4 E^{2}PROM Interface

SDA	I/O, S, PU	189	**Serial Data:** See application note "DP83891 Gig PHYTER E^{2}PROM Usage Guide" on how to use this interface. Also see strap pin section.
SCL	I/O, S, PD	190	**SERIAL CLOCK :**See application note "DP83891 Gig PHYTER E^{2}PROM Usage Guide" on how to use this interface. Also see strap pin section.

1.5 Clock Interface

Signal Name	Type	Pin #	Description
X1/REF_CLK	I	153	**CLOCK INPUT:** 125 MHz (50 ppm)
X2	O	154	**X2:** Leave floating.

1.6 LED Interface

(See Section 2.4 on page 18 for active polarity.)

LED_RX	I/O, S, PD	207	**RECEIVE ACTIVITY LED:** The Receive LED output indicates that the PHY is receiving.
LED_TX	I/O, S, PD	205	**TRANSMIT ACTIVITY LED:** The Transmit LED output indicates that the PHY is transmitting.
LED_LNK	I/O, S, PD	204	**GOOD LINK LED STATUS:** Indicates status for Good Link the criteria for good link are: 100BASE-T: link is established as a result of an input receive amplitude compliant with TP-PMD specifications which will result in internal generation of Signal Detect. LED_LNK will assert after the internal Signal Detect has remained asserted for a minimum of 500 µs. LED_LNK will de-assert immediately following the de-assertion of the internal Signal Detect. 1000BASE-T: link is established as a result of training, auto-negotiation completed and valid 1000BASE-T link is established and reliable reception of signals transmitted from a remote PHY is possible.
LED_DUPLEX	I/O, S, PU	185	**DUPLEX LED STATUS:** If LED on, it indicates Full Duplex mode of operation, else half duplex.
LED_COL	I/O, S, PD	201	**COLLISION LED STATUS:** Indicates that the PHY has detected a collision condition (simultaneous transmit and receive activity while in Half Duplex mode).
LED_ACT	I/O, S, PU	200	**TX/RX ACTIVITY LED STATUS:** Indicates either transmit or receive activity.
LED_10	I/O, S, PD	180	**10 Mb/s SPEED LED:** If LED is on, then the current speed of operation is 10 Mb/s.
LED_100	I/O, S, PD	181	**100 Mb/s SPEED LED:** If LED is on, then the current speed of operation is 100 Mb/s.
LED_1000	I/O, S, PU	184	**1000 Mb/s SPEED LED:** If LED is on, then the current speed of operation is 1000 Mb/s.

1.7 Device Configuration Interface

Signal Name	Type	Pin #	Description
AN_EN	I/O, S, PU	192	**AUTO-NEGOTIATION ENABLE:** Input to set value of Auto-Negotiation Enable bit (register 0 bit-12). A high enables Auto-Neg and a Low disables Auto-Neg. If this pin is strapped low, then pin 184 should be strapped high.
MANUAL_M/S_CFG	I/O, S, PD	190	**MANUAL MASTER/SLAVE CONFIG ENABLE:** Input to set value of manual Master/Slave Configuration Enable bit (register 9 bit-12). A high enables Master/Slave Config and a Low disables Master/Slave Config.
MAS_SLAVE	I/O, S, PD	191	**MASTER SLAVE CONFIGURATION VALUE:** Input to set value of Master/Slave Configuration bit (register 9 bit-11). A high configures PHY to Master during Master/Slave negotiation and a Low configures PHY to Slave during Master/Slave negotiation.
1000FDX_ADV	I, S, PU	195	**AUTO_NEG 1000 FDX ADVERTISE:** The value strapped during power/on reset determines the mode of operation advertised during Auto-Negotiation. '1' advertises 1000 Mb/s full duplex capability; '0' does not.
1000HDX_ADV	I, S, PU	189	**AUTO_NEG 1000 HDX ADVERTISE:** The value strapped during power/on reset determines the mode of operation advertised during Auto-Negotiation. '1' advertises 1000 Mb/s half duplex capability; '0' does not.
100HDX_ADV	I/O, S, PU	184	**100 Mb/s HALF DUPLEX ADVERTISE:** This strap option pin determines if 100 Mb/s Half Duplex capability will be advertised during Auto-negotiation. '1' advertises this capability, '0' does not. If Auto-Negotiation is disabled by pulling pin 192 low, then this pin should be pulled high.
DUPLEX/100FDX_ADV	I/O, S, PU	185	**DUPLEX MODE SELECT/100 Mb/s FULL DUPLEX ADVERTISE:** This strap option has two functions depending on whether Auto-neg is enabled or not. If Auto-Neg disabled, then a '1' straps on full duplex mode of operation while '0' straps on half duplex mode of operation. If Auto-neg is enabled then a '1' advertises 100 Mb/s FDX capability while a '0' does not advertise 100 Mb/s FDX capability. (This bit in NOT used to advertise HDX capability during Auto-Neg. Pin 184 is used for that purpose.)

Signal Name	Type	Pin #	Description
SPEED[1]/10_ADV **SPEED[0]/PORT_TYPE**	I/O, S,PD I/O, S, PD	180 208	**SPEED SELECT/PORT_TYPE/10 Mb/s ADVERTISE:** These strap option pins have 2 different functions depending on whether Auto-Neg is enabled or not. SPEED[1:0] Auto-Neg disabled (Forced Speed mode:) 00 10BASE-T 01 100BASE-TX 10 1000BASE-T 11 Reserved SPEED[1] Auto-Neg enabled (Advertised capability:) '1' advertises 10 Mb/s capability (Both Full Duplex and Half Duplex.) '0' does not advertise 10 Mb/s capability. (Neither Full Duplex nor Half Duplex is advertised.) SPEED[0] Auto-Neg enabled (Advertised capability:) '1' Advertises Multi Node (e.g. Repeater or Switch) '0' Advertises Single Node mode. (e.g. NIC)
PHYAD_0 **PHYAD_1** **PHYAD_2** **PHYAD_3** **PHYAD_4**	I/O, S, PU I/O, S, PD I/O, S, PD I/O, S, PD I/O, S, PD	200 201 204 205 207	**PHY ADDRESS [4:0]:** The DP83891 provides five PHY address-sensing pins for multiple applications. The five PHYAD[4:0] are registered as inputs at reset with PHYAD_4 being the MSB of the 5-bit PHY address.

1.8 Reset

Signal Name	Type	Pin #	Description
$\overline{\text{RESET}}$	I	164	**RESET:** The active low $\overline{\text{RESET}}$ input allows for hard-reset, soft-reset, and TRI-STATE output reset combinations. The $\overline{\text{RESET}}$ input must be low for a minimum of 140 µs.

1.9 Power And Ground Pins

Signal Name	Pin #	Description
TTL/CMOS INPUT/OUTPUT SUPPLY		
IO_V_{DD}	58, 64, 73, 79, 87, 93, 102, 109, 117, 123, 132, 143, 149, 167, 178, 187, 193, 202	3.3 V MII I/O Supply
IO_V_{SS}	57, 63, 72, 78, 86, 92, 101, 108, 116, 122, 131, 142, 148, 168, 179, 188, 194, 203	I/O Ground
TRANSMIT/RECEIVE SUPPLY		
CD#_A_{GND}	11, 12, 41, 42	Common Driver Ground
CD#_AV_{DD}	8, 15, 38, 45	3.3 V Common Driver Supply
R#_AV_{DD}#	2, 6, 17, 21, 32, 36, 47, 51	3.3 V Receiver Analog Supply
R#_A_{GND}#	3, 7, 16, 20, 33, 37, 46, 50	Receiver Analog Ground
R#_A_{SUB}	1, 22, 31, 52	Receiver Substrate Ground

Signal Name	Pin #	Description
INTERNAL SUPPLY PAIRS		
CORE_V_{DD}	69, 83, 98, 129, 137, 160, 171, 182, 197	3.3 V Digital Supply
CORE_V_{SS}	68, 82, 97, 128, 136, 161, 172, 183, 198	Digital Ground
CORE_$_{SUB}$	67, 96, 127, 162, 173, 199	Substrate Ground
PGM_AV_{DD}	27	3.3 V PGM/CGM Supply. We recommend a low pass filter composed of a 22.1 Ω resistor and a 47 µF capacitor between the 3.3 V supply and this pin.
PGM_A_{GND}	28	PGM/CGM Ground
BG_$_{SUB}$	26	BG Substrate Ground
BG_AV_{DD}	23	3.3 V BG Supply
BG_A_{GND}	25	BG Ground
SHR_V_{DD}	29	3.3 V Share Logic Supply
SHR_$_{GND}$	30	Share Logic Ground
OSC_V_{DD}	155	3.3 V Oscillator Supply
OSC_V_{SS}	152	Oscillator Ground

1.10 Special Connect Pins

Signal Name	Pin #	Description
BG_REF	24	Internal Reference Bias (requires connection to ground via a 9.31 kΩ resistor).
TEST	186,206	These pins should be pulled-up to 3.3 V. (Note 1)
SI,SO	104,105	These two pins should be floated if not used.
Reserved (Please also see next row. There are two sets of reserved pins--one set needs to be pulled-down to ground while the other set needs to be floated.)	53-56, 59-62, 65, 66, 70, 71, 74-77, 80, 81, 84, 85, 88-91, 94, 95, 99, 100, 103,106, 107, 196	These pins are reserved. These pins are to be left floating.
Reserved	165, 166, 169, 170,174,175, 176,177	These pins are reserved. These pins are to be pulled-down to ground.

Note 1: Please see “DP83891 Design Review Guide” for details of how to pull-down unused inputs/reserved pins. In general a 2 kΩ resistor is recommended either individual used for each pin, or used to pull-down a group of pins.

Note: I = Input, O = Output, I/O = Bidirectional, Z = Tri-state output, S = Strapping pin

1.11 Package Pin Assignments/Cross Reference

Pin #	DataSheet Pin Name	Pin #	DataSheet Pin Name
1	RA_A_{SUB}	105	SO
2	RA_AV_{DD}	106	Reserved
3	RA_A_{GND}	107	Reserved
4	RXDA+	108	IO_V_{SS}
5	RXDA-	109	IO_V_{DD}
6	RA_AV_{DD}	110	COL
7	RA_A_{GND}	111	CRS
8	CDA_AV_{DD}	112	RX_ER
9	TXDA+	113	RX_DV
10	TXDA-	114	RXD7
11	CDA_A_{GND}	115	RXD6
12	CDB_A_{GND}	116	IO_V_{SS}
13	TXDB-	117	IO_V_{DD}
14	TXDB+	118	RXD5
15	CDB_AV_{DD}	119	RXD4
16	RB_A_{GND}	120	RXD3
17	RB_AV_{DD}	121	RXD2
18	RXDB-	122	IO_V_{SS}
19	RXDB+	123	IO_V_{DD}
20	RB_A_{GND}	124	RXD1
21	RB_AV_{DD}	125	RXD0
22	RB_A_{SUB}	126	RX_CLK
23	BG_AV_{DD}	127	$CORE\_{}_{SUB}$
24	BG_REF	128	$CORE\_V_{SS}$
25	BG_A_{GND}	129	$CORE\_V_{DD}$
26	$BG\_{}_{SUB}$	130	TX_CLK
27	PGM_AV_{DD}	131	IO_V_{SS}
28	PGM_A_{GND}	132	IO_V_{DD}
29	SHR_V_{DD}	133	TX_ER
30	SHR_GND	134	TX_EN
31	RC_A_{SUB}	135	TXD7
32	RC_AV_{DD}	136	$CORE\_V_{SS}$
33	RC_A_{GND}	137	$CORE\_V_{DD}$
34	RXDC+	138	TXD6
35	RXDC-	139	TXD5
36	RC_AV_{DD}	140	TXD4
37	RC_A_{GND}	141	TXD3
38	CDC_AV_{DD}	142	IO_V_{SS}
39	TXDC+	143	IO_V_{DD}

Pin #	DataSheet Pin Name	Pin #	DataSheet Pin Name
40	TXDC-	144	TXD2
41	CDC_A_{GND}	145	TXD1
42	CDD_A_{GND}	146	TXD0
43	TXDD-	147	GTX_CLK
44	TXDD+	148	IO_V_{SS}
45	CDD_AV_{DD}	149	IO_V_{DD}
46	RD_A_{GND}	150	MDIO
47	RD_AV_{DD}	151	MDC
48	RXDD-	152	OSC_V_{SS}
49	RXDD+	153	X1/REF_CLK
50	RD_A_{GND}	154	X2
51	RD_AV_{DD}	155	OSC_V_{DD}
52	RD_A_{SUB}	156	$\overline{TRST}$
53	Reserved	157	TDI
54	Reserved	158	TDO
55	Reserved	159	TMS
56	Reserved	160	$CORE\_V_{DD}$
57	IO_V_{SS}	161	$CORE\_V_{SS}$
58	IO_V_{DD}	162	$CORE\_{SUB}$
59	Reserved	163	TCK
60	Reserved	164	$\overline{RESET}$
61	Reserved	165	Reserved
62	Reserved	166	Reserved
63	IO_V_{SS}	167	IO_V_{DD}
64	IO_V_{DD}	168	IO_V_{SS}
65	Reserved	169	Reserved
66	Reserved	170	Reserved
67	$CORE\_{SUB}$	171	$CORE\_V_{DD}$
68	$CORE\_V_{SS}$	172	$CORE\_V_{SS}$
69	$CORE\_V_{DD}$	173	$CORE\_{SUB}$
70	Reserved	174	Reserved
71	Reserved	175	Reserved
72	IO_V_{SS}	176	Reserved
73	IO_V_{DD}	177	Reserved
74	Reserved	178	IO_V_{DD}
75	Reserved	179	IO_V_{SS}
76	Reserved	180	LED_10/10_ADV/SPEED [1]
77	Reserved	181	LED_100
78	IO_V_{SS}	182	$CORE\_V_{DD}$
79	IO_V_{DD}	183	$CORE\_V_{SS}$
80	Reserved	184	LED_1000/100HDX_ADV

Pin #	DataSheet Pin Name	Pin #	DataSheet Pin Name
81	Reserved	185	LED_DUPLEX/100FDX_ADV
82	CORE_V_{SS}	186	TEST
83	CORE_V_{DD}	187	IO_V_{DD}
84	Reserved	188	IO_V_{SS}
85	Reserved	189	1000HDX_ADV
86	IO_V_{SS}	190	MANUAL_M/S_CFG
87	IO_V_{DD}	191	MAS _SLAVE
88	Reserved	192	AN_EN
89	Reserved	193	IO_V_{DD}
90	Reserved	194	IO_V_{SS}
91	Reserved	195	1000FDX_ADV
92	IO_V_{SS}	196	Reserved
93	IO_V_{DD}	197	CORE_V_{DD}
94	Reserved	198	CORE_V_{SS}
95	Reserved	199	CORE_$_{SUB}$
96	CORE_$_{SUB}$	200	LED_ACT/PHYAD_0
97	CORE_V_{SS}	201	LED_COL/PHYAD_1
98	CORE_V_{DD}	202	IO_V_{DD}
99	Reserved	203	IO_V_{SS}
100	Reserved	204	LED_LNK/PHYAD_2
101	IO_V_{SS}	205	LED_TX/PHYAD_3
102	IO_V_{DD}	206	TEST
103	Reserved	207	LED_RX/PHYAD_4
104	SI	208	SPEED [0]/PORT_TYPE

2.0 Configuration

This section includes information on the various configuration options available with the DP83891. The configuration options described herein include:

— Speed/Duplex Mode Selection
— MASTER/SLAVE configuration
— Auto-Negotiation
— PHY Address and LEDs
— Isolate mode
— Loopback mode
— MII/GMII MAC interface
— Test Modes
— Clock input options
— Twisted Pair Interface
— Auto MDI / MDI-X Configuration
— Power Supply Filtering

2.1 Speed/Duplex Mode Selection

The DP83891 supports six different Ethernet protocols: 10BASE-T full duplex, 10BASE-T half duplex, 100BASE-TX full duplex, 100BASE-TX half duplex, 1000BASE-T full duplex and 1000BASE-T half duplex. Both the speed and the duplex mode of operation can be determined by either Auto-Negotiation (AN) or set by manual configuration. Both Auto-Negotiation and manual configuration can be controlled by strap values applied to certain pins during power-on/reset. They can be also controlled by access to internal registers.

2.2 Manual Configuration

2.2.1 Manual Speed/Duplex selection

For manual configuration of the speed of operation and the duplex modes, the Auto-negotiation function has to be disabled. This can be achieved by strapping AN_EN pin 192 low during power-on/reset. Auto-neg can also be disabled by writing a “0” to bit 12 of the BMCR register. (0x00). Once AN is disabled then the strap value of the SPEED[1:0] pins (180,208) will be used to determine speed of operation, and the strap value of the LED_DUPLEX pin 185 will be used to determine duplex mode.

Table 1. Non Auto-Negotiation Modes

AN_EN	SPEED [1]	SPEED [0]	Forced Mode
0	0	0	10BASE-T
0	0	1	100BASE-TX
0	1	0	1000BASE-T
0	1	1	Reserved

For all of the modes above, DUPLEX pin 185 strap value “1” selects Full Duplex, while “0” selects Half Duplex. The strap values latched on during power-on reset can be overwritten by access to the BMCR register 0x00 bits 13,12, 8 and 6.

2.2.2 Manual MASTER/SLAVE resolution

In 1000BASE-T the two link partner devices have to be configured, one of them as a MASTER and the other as a SLAVE. The MASTER device by definition uses a local clock to transmit data on the wire; while the SLAVE device uses the clock recovered from the incoming data for transmitting its own data. (The DP83891 uses the X1/Ref_CLK as the local clock for transmit purposes if configured as MASTER) The MASTER and SLAVE assignments can be manually set by using strap options or register writes.Pins 190 and 191 enable Manual Master/SLAVE selection and assign the MASTER/SLAVE value respectively. If both the link partner and the local device are manually given the same MASTER/SLAVE assignment, then an error condition will exist as indicated by bit 15 of register 0x0A. If one of the link partners is manually assigned a Master/Slave status while the other is not, then the manual assignment will take higher priority during the resolution process.

2.3 Auto-Negotiation

All 1000BASE-T PHYs are required to support Auto-negotiation. (The 10/100 Mb/s Ethernet PHYs had an option to support Auto-Negotiation, as well as parallel detecting when a link partner didn’t support Auto-neg.) The Auto-negotiation function in 1000BASE-T has four primary purposes:

— Auto-Negotiation Priority Resolution
— Auto-Negotiation MASTER/SLAVE Resolution
— Auto-Negotiaton PAUSE/ AYSMMETRICAL PAUSE Resolution
— Auto-MDIX resolution

2.3.1 Auto-Negotiation Priority Resolution

First the Auto-Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices.

Fast Link Pulse (FLP) Bursts provide the signalling used to communicate Auto-Negotiation abilities between two devices at each end of a link segment. For further detail regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3u specification. The DP83891 supports six different Ethernet protocols: 10BASE-T full duplex, 10BASE-T half duplex, 100BASE-TX full duplex, 100BASE-TX half duplex, 1000BASE-T full duplex and 1000BASE-T half duplex, so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the advertised ability of the Link Partner.

Auto-Negotiation Priority Resolution for the Gig PHYTER:

1. 1000BASE-T Full Duplex (Highest Priority)
2. 1000BASE-T Half Duplex
3. 100BASE-TX Full Duplex
4. 100BASE-TX Half Duplex
5. 10BASE-T Full Duplex
6. 10BASE-T Half Duplex (Lowest Priority)

2.3.2 Auto-Negotiation MASTER/SLAVE Resolution

The second goal of Auto-Negotiation in 1000BASE-T devices is to resolve MASTER/SLAVE configuration. If both devices have disabled manual Master/Slave configuration then MASTER priority is given to the devices which support multiport nodes. (i.e. Switches and Repeaters take higher priority over DTE single node PHYs.) Pin 208 is a strap option for advertising the Multi-node functionality. (See Table 2) If both PHYs advertise the same options then the

Master/Slave resolution is resolved by a random number generation. See IEEE 802.3ab Clause 40.5.1.2 for more details.

2.3.3 Auto-Negotiation PAUSE and Asymmetrical PAUSE Resolution

Auto-Negotiation is also used to determine the Flow Control capabilities of the two link partners. Flow control was originally introduced as a mechanism to force a busy station's Link Partner to stop sending data in full duplex mode of operation. Unlike half duplex mode of operation -- where a link partner could be forced to back off by simply causing collisions--, the full duplex operation needed a formal mechanism to slow down a link partner in the event of the receiving station's buffers becoming full. A new MAC control layer was added to handle generation and reception of Pause Frames which contained a timer indicating the amount of Pause requested. Each MAC/Controller has to advertise whether it can handle PAUSE frames, and whether they support PAUSE frames in both directions. (i.e. receive and transmit. If the MAC/Controller will only generate PAUSE frames but will not respond to PAUSE frames generated by a link partner, then this is called Asymmetrical PAUSE.) Advertisement of these capabilities can be achieved by writing a '1' to bits D10 and D11 of the Auto-Neg Advertisement register. (Address 0x04.) The link partners PAUSE capabilities can be determined from register 0x05 using these same bits. The MAC/controller has to write to and read from these registers and determine which mode of PAUSE operation to choose. The PHY layer is not involved in Pause resolution other than the simple advertising and reporting of PAUSE capabilities. (These capabilities are MAC capabilities and configured by the MAC into PHY registers.)

2.3.4 Auto-Negotiation Auto-MDIX resolution

The Gig PHYTER can determine if a "straight" or "cross-over" cable is being used to connect to the link partner and can automatically re-assing channel A and channel B to establish link with the link partner. Although not part of the Auto-Negotiation FLP exchange process, the Auto-MDIX resolution requires that Auto-Negotiation is enabled. Auto-MDIX resolution will precede the actual Auto-Negotiation process which involves exchange of FLPs to advertise capabilities. If Auto-Negotiation is not enabled, then the MDIX function can be manually configured by disabling Auto-MDIX and forcing either straight or cross-over cable configuration. See section on FAQs for details.

2.3.5 Auto-Negotiation Strap Option Control

The Auto-Negotiation function within the DP83891 can be controlled either by internal register access or by the use of the AN_EN, and various strap pin values during power-on/reset. Table below shows how the various strap pin values are used during Auto-Negotiation to advertise different capabilities.

Table 2. Auto-Negotiation Modes AN_EN = 1

Pin #	Pin Name	Comments
195	1000FDX_ADV	'1' Advertises 1000 Mb/s FDX capability.
189	1000HDX_ADV	'1' Advertises 1000 Mb/s HDX capability
185	LED_DUPLEX/ 100FDX_ADV	'1' Advertises 100 Mb/s FDX capability
184	100HDX_ADV	'1' Advertises 100 Mb/s HDX capability.
180	LED_10/ 10_ADV/ SPEED[1]	'1' Advertises 10 Mb/s FDX and HDX. '0' advertises neither FDX nor HDX 10 Mb/s capability.
208	SPEED[0]/ PORT_TYPE	'1' Advertises Multi Node functionality. (e.g. Switch or Repeater. in contrast to NIC single node operation.)

2.3.6 Auto-Negotiation Register Control

The state of AN_EN, SPEED [1:0],DUPLEX pins as well as the xxx_ADV pins during power-on/reset determines whether the Auto-negotiation is enabled and if so what specific ability (or set of abilities) are advertised as given in Table 2. These strapping option pins allow configuration options to be selected without requiring internal register access.

The Auto-Negotiation function selected at power-up or reset can be changed at any time by writing to the Basic Mode Control Register (BMCR) at address 0x00, Auto-Negotiation Advertisement Register 0x04 or to 1000BASE-T Control Register (1KTCR) 0x09.

When Auto-Negotiation is enabled, the DP83891 transmits the abilities programmed into the Auto-Negotiation Advertisement register (ANAR) at address 0x00, and 1KTCR at address 0x09 via FLP Bursts. Any combination of 10 Mb/s,100 Mb/s, 1000 Mb/s, Half-Duplex, and Full Duplex modes may be selected. The Auto-Negotiation protocol compares the contents of the ANLPAR and ANAR registers (for 10/100 Mb/s operation) and the contents of 1000BASE-T status and control registers, and uses the results to automatically configure to the highest performance protocol between the local and far-end port. The results of Auto-Negotiation may be accessed in registers BMCR (Duplex Status and Speed Status), and BMSR (Auto-Neg Complete, Remote Fault, Link).

The Basic Mode Control Register (BMCR) at address 00h provides control for enabling, disabling, and restarting the Auto-Negotiation process.

The Basic Mode Status Register (BMSR) at address 01h indicates the set of available abilities for technology types, Auto-Negotiation ability, and Extended Register Capability. These bits are permanently set to indicate the full functionality of the DP83891

The BMSR also provides status on:

— Whether Auto-Negotiation is complete (bit 5)

— Whether the Link Partner is advertising that a remote fault has occurred (bit 4)

— Whether a valid link has been established (bit 2)

The Auto-Negotiation Advertisement Register (ANAR) at address 04h indicates the Auto-Negotiation abilities to be advertised by the DP83891. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR. Updating the ANAR to suppress an ability is one way for a management agent to change (force) the technology that is used.

The Auto-Negotiation Link Partner Ability Register (ANLPAR) at address 05h is used to receive the base link code word as well as all next page code words during the negotiation.

If Next Page is NOT being used, then the ANLPAR will store the base link code word (link partner's abilities) and retain this information from the time the page is received, as indicated by a 1 in bit 1 of the ANER register (address 06h), through the end of the negotiation and beyond.

When using the next page operation, the DP83891 cannot wait for Auto-Negotiation to complete in order to read the ANLPAR because the register is used to store both the base and next pages. Software must be available to perform several functions. The ANER (register 06h) must have a page received indication (bit 1), once the DP83891 receives the first page, software must store it in memory if it wants to keep the information. Auto-Negotiation keeps a copy of the base page information but it is no longer accessible by software. After reading the base page information, software needs to write to ANNPTR (register 07h) to load the next page information to be sent. Continue to poll the page received bit in the ANER and when active read the ANLPAR. The contents of the ANLPAR will tell if the partner has further pages to be sent. As long as the partner has more pages to send, software must write to the next page transmit register and load another page.

The Auto-Negotiation Expansion Register (ANER) at address 06h indicates additional Auto-Negotiation status. The ANER provides status on:

— Whether a Parallel Detect Fault has occurred (bit 4, register address 06h.)

— Whether the Link Partner supports the Next Page function (bit 3, register address 06h.)

— Whether the DP83891 supports the Next Page function (bit 2, register address 06h). (The DP83891 does support the Next Page function.)

— Whether the current page being exchanged by Auto-Negotiation has been received (bit1, register address 06h.)

— Whether the Link Partner supports Auto-Negotiation (bit 0, register address 06h.)

The Auto-Negotiation Next Page Transmit Register (ANNPTR) at address 07h contains the next page code word to be sent. See Auto-Negotiation Next Page Transmit Register (ANNPTR) address 07h for a bit description of this register.

2.3.7 Auto-Negotiation Parallel Detection

The DP83891 supports the Parallel Detection function as defined in the IEEE 802.3u specification. Parallel Detection requires the 10/100 Mb/s receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation, yet is transmitting link signals that the 10BASE-T or 100BASE-X PMA recognize as valid link signals.

If the DP83891 completes Auto-Negotiation as a result of Parallel Detection, without Next Page operation, bits 5 and 7 within the ANLPAR register (address 05h) will be set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR will also be set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that negotiation completed via Parallel Detection by reading a zero in the Link Partner Auto-Negotiation Ability register (bit 0, register address 06h) once the Auto-Negotiation Complete bit (bit 5, register address 01h) is set. If configured for parallel detect mode and any condition other than a single good link occurs then the parallel detect fault bit will set (bit 4, register 06h).

2.3.8 Auto-Negotiation Restart

Once Auto-Negotiation has completed, it may be restarted at any time by setting bit 9 (Restart Auto-Negotiation) of the BMCR to one. If the mode configured by a successful Auto-Negotiation loses a valid link, then the Auto-Negotiation process will resume and attempt to determine the configuration for the link. This function ensures that a valid configuration is maintained if the cable becomes disconnected.

A renegotiation request from any entity, such as a management agent, will cause the DP83891 to halt any transmit data and link pulse activity until the break_link_timer expires (~1500 ms). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The DP83891 will resume Auto-Negotiation after the break_link_timer has expired by issuing FLP (Fast Link Pulse) bursts.

2.3.9 Enabling Auto-Negotiation via Software

It is important to note that if the DP83891 has been initialized upon power-up as a non-auto-negotiating device (forced technology), and it is then required that Auto-Negotiation or re-Auto-Negotiation be initiated via software, bit 12 (Auto-Negotiation Enable) of the Basic Mode Control Register must first be cleared and then set for any Auto-Negotiation function to take effect.

2.3.10 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation take approximately 2-3 seconds to complete. In addition, Auto-Negotiation with next page should take approximately 2-3 seconds to complete, depending on the number of next pages sent.

Refer to Clause 28 of the IEEE 802.3u standard for a full description of the individual timers related to Auto-Negotiation.

Auto-Negotiation Next Page Support

The DP83891 supports the optional Auto-Negotiation Next Page protocol. The ANNPTR register (address 07h) allows for the configuration and transmission of Next Page. Refer to clause 28 of the IEEE 802.3u standard for detailed information regarding the Auto-Negotiation Next Page function. This functionality is also discussed in Section 2.3.6 above.

2.4 PHY Address and LEDs

The 5 PHY address inputs pins are shared with the LED pins as shown below.

Table 3. PHY Address Mapping

Pin #	PHYAD Function	LED Function
200	PHYAD_0	ACT
201	PHYAD_1	COL
204	PHYAD_2	LNK
205	PHYAD_3	TX
207	PHYAD_4	RX

The DP83891 can be set to respond to any of 32 possible PHY addresses. (However PHY Address = 0 will put the Gig PHYTER in isolate mode.) Each DP83891 or port sharing an MDIO bus in a system must have a unique physical address.

The pull-up or pull-down state of each of the PHYAD inputs is latched (register 0x10) at system power-up/reset. For further detail relating to the latch-in timing requirements of the PHY Address pins, as well as the other hardware configuration pins, refer to the Reset timing in Section 5.7 on page 58.

Since the PHYAD strap options share the LED output pins, the external components required for strapping and LED usage must be considered in order to avoid contention.

Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. Conversely, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. Refer to Figure 1 for an example of LED & PHYAD connection to external components. In this example, the PHYAD strapping results in address 00011 (03h).

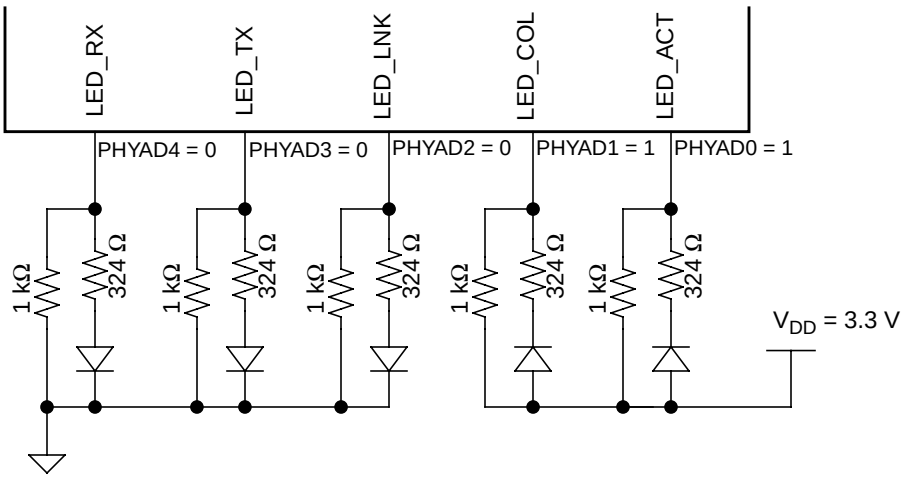


Figure 1. PHYAD Strapping and LED Loading Example

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual purpose pins.

This adaptive nature for choosing the active high or active low configuration applies to all the LED pins; not just the LED pins associated with PHYAD strap options. So all LED pins will be high active if the strap value during reset on that specific LED pin was a '0'. Else if the strap value was a '1' then the LED will be low active.

2.5 MII Isolate Mode

2.5.1 10/100 Mb/s Isolate Mode

The DP83891 can be put into MII Isolate mode by writing to bit 10 of the BMCR register.

With bit 10 in the BMCR set to one the DP83891 does not respond to packet data present at TXD[3:0], TX_EN, and TX_ER inputs and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs. The DP83891 will continue to respond to all management transactions.

While in Isolate mode, the TD± outputs will not transmit packet data but will continue to source 100BASE-TX scrambled idles or the 10 Mb/s link pulses.

2.5.2 1000 Mb/s Isolate Mode

During 1000 Mb/s operation, entering the isolate mode, will TRI-STATE the GMII outputs of the Gig PHYTER. The DP83891 will operate as normal other than this change. (i.e. it will respond to TXE, TXD signals and transmit data out on the wire.)

2.6 Loopback

The DP83891 includes a Loopback Test mode for easy board diagnostics. The Loopback mode is selected through bit 14 (Loopback) of the Basic Mode Control Register (BMCR). Writing 1 to this bit enables MII/GMII transmit data to be routed to the MII/GMII receive outputs. While in Loopback mode the data will not be transmitted onto the

media. This is true for either 100 Mb/s as well 1000 Mb/s data.

In 100BASE-TX Loopback mode the data is routed through the PCS and PMA layers into the PMD sublayer before it is looped back. Therefore, in addition to serving as a board diagnostic, this mode serves as quick functional verification of the device.

2.7 MII/GMII interface and speed of operation

The DP83891 supports 2 different MAC interfaces. MII for 100 Mb/s, GMII for 1000 Mb/s. The speed of operation determines the interface chosen. The speed can be determined by Auto-negotiation, or by strap options, or by register writes.

Auto-Negotiation Disabled:

SPEED[1:0]	Link Strapped	Controller I/F
00	10BASE-T	MII
01	100BASE-TX	MII
10	1000BASE-T	GMII

Auto-Negotiation Enabled:

Link Negotiated	Controller I/F
10BASE-T	MII
100BASE-TX	MII
1000BASE-T	GMII

2.8 Test Modes

IEEE 802.3ab specification for 1000BASE-T requires that the PHY layer be able to generate certain well defined test patterns. Clause 40 section 40.6.1.1.2 “Test Modes” describes these tests in detail. There are 4 test modes as well as the normal operation mode. These modes can be selected by writing to the 1000BASE-T control register (0x09) as shown below.

Test Mode Select:

bit 15	bit 14	bit 13	Test Mode Selected
1	0	0	= Test Mode 4
0	1	1	= Test mode 3
0	1	0	= Test Mode 2
0	0	1	= Test Mode 1
0	0	0	= Normal Operation

See IEEE 802.3ab section 40.6.1.1.2 “Test modes” for more information.

2.9 Clocks

Pin 153 is the 125 MHz clock input to the DP83891 which is used by the internal PLL to generate the various clocks needed both internally and externally. This input should come from an 125 MHz oscillator (+/- 50 ppm). Pin 154 should be left floating.

A second option for the X1 input is the reference clock which is common to the MAC (i.e. GTX_CLK pin 147). Using this option might require buffering of the clock to insure signal integrity.

The clock signal requires the same termination considerations mentioned in the MAC interface section. The clock signal might require both series source termination (R_S) at the output of the crystal and/or load termination (R_T) close to the PHY to eliminate reflections. This will depend on the distance of the clock source from the PHY clock input, as well as source impedance of the clock source, as well as the board impedance for the clock line considered as a transmission line. Typically no series or load termination is required for short traces. For long traces a series resistor is recommended. Unlike load termination, this doesn’t add to the load current. The value of the series termination resistor has to be chosen to match the line impedance. As an example, if the clock source has output impedance of 20Ω and the clock trace has transmission line impedance Zo = 50Ω then Rs = 50 - 20 = 30Ω.

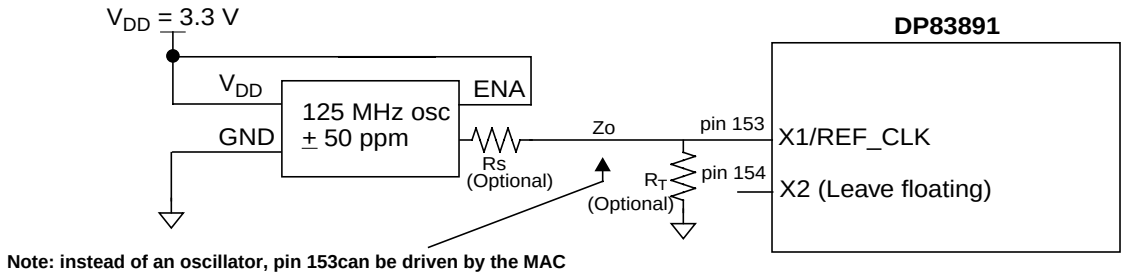
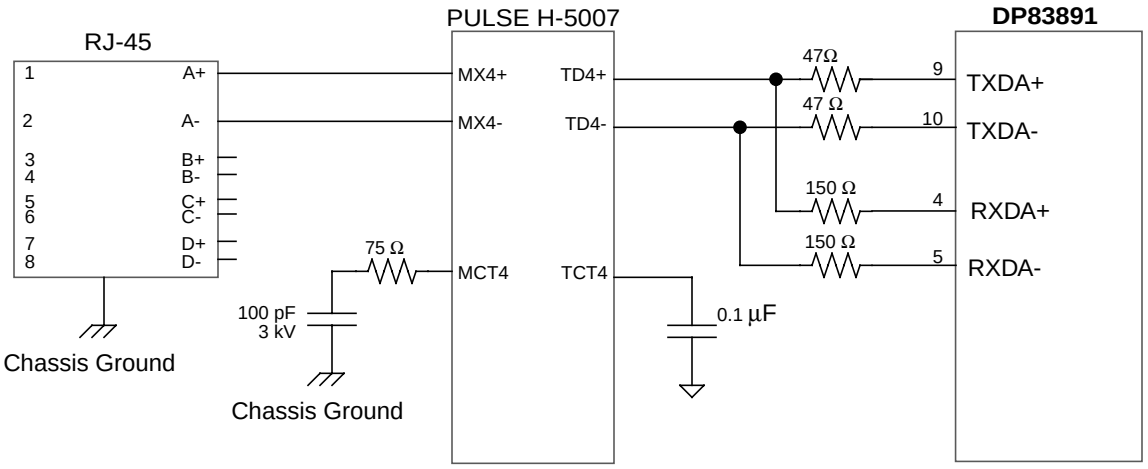


Figure 2. Clock Pin

2.10 Twisted Pair Interface

The Twisted Pair Interface consists of four differential transmit pairs (Channels A, B, C, and D) and four differential receive pairs (Channels A, B, C, and D). Each transmit pair is connected to its corresponding receive pair through 47 Ω and 150 Ω resistors respectively. (The two 47 Ω resistors in combination with the source impedance of the transmitter will form a 100 Ω differential input impedance as seen from the line. This is required to minimize reflections.) Figure 3 shows a typical connection for Channel A. Channels B, C, and D are identical. The combined transmit and receive trace then goes directly to 1:1 magnetics. We currently recommend using the Pulse H-5004 or Pulse H-5007. Both magnetics are pin for pin compatible. The H-5004 has an isolation transformer followed by a common mode choke to reduce EMI. The H-5007 has an additional auto-transformer which is center tapped. These 2 transformers as

well as other suppliers' transformers should be evaluated for best performance for each design.



Only the connections for one of the twisted pair channels is shown. Connections for channels B, C, D are similar and are shown in the Reference Design Schematics.

Figure 3. Twisted Pair/Magnetics interface (Shown only for channel A)

— Place the 47Ω 1% transmit resistors close as possible to the TXDA+/-, TXDB+/-, TXDC+/-, and TXD+/- pins

— Place the 150Ω 1% receive resistors close as possible to the RXDA+/-, RXDB+/-, RXDC+/-, and RXDD+/- pins.

— All traces to and from the twisted pair interface should have a controlled impedance of 50Ω to the ground plane. This is a strict requirement. They should be as close in length to each other as possible.

— Ideally there should be no crossovers or vias on the signal paths of these traces. See Reference Design Schematics for how this can be accomplished.

2.11 MAC Interface Layout Considerations

The DP83891 can be configured in one of two different modes:

— GMII (Gigabit Media Independent Interface) MODE: This interfaces is used to support 802.3z compliant 1000 Mb/s MACs.

— MII (Media Independent Interface) MODE: This interface is used to support 10/100 Mb/s MACs.

Only one mode can be supported at a time, since the GMII and MII share some pins in common.

These outputs are capable of driving 35 pF under worst case conditions. These outputs were not designed to drive multiple loads, connectors, backplanes, or cables. It is recommended that the outputs be series terminated through a resistor as close to the output pins as possible. The purpose of the series termination is to reduce reflections on the line. The value of the series termination and length of trace the output can drive will depend on the driver output impedance, the characteristic impedance of the PCB trace (we recommend 50Ω), the distributed trace capacitance (capacitance/inch), and the load capacitance (MAC input). For short traces, less than 0.5 inches, the series resistors may not be required, thus reducing component count. However, each specific board design should be evaluated for reflections and signal integrity to determine the need for the series terminations. As a general rule of thumb, if the trace length is less than 1/6 of the equivalent length of the rise and fall times then the series terminations might not be needed. Equivalent length of rise time = Rise time (ps) / Delay (ps/inch). Rise and fall times are required to be less than 1 ns for some GMII signals, typically being in the order of 500 ps for those pins. (i.e. RX_CLK, GTX_CLK). Delay typically = 170 ps/inch on a FR4 board. Using the above numbers we get critical trace length = (1/6) *(500/ 170) = 0.5 inches.

— Place series termination resistors as close to the pins as possible.

— Keep capacitance < 35 pF as seen by the output.

— Keep output trace lengths approximately the same length to avoid skew problems.

— Keep input trace lengths approximately the same length to avoid skew problems.

— All GMII traces should be impedance controlled. 50Ω to ground plane is recommended, but this is not a strict requirement and the board designer can experiment with different values if needed, to minimize reflections.

2.12 Automatic MDI / MDI-X Configuration

The DP83891 implements the automatic MDI / MDI-X configuration functionality as described in IEEE 802.3ab Clause 40, Section 40.8.3. This functionality eliminates the need for crossover cables between similar devices. The switching between the +/- A port with the +/- B port will be automatically taken care of, as well as switching between the +/- C port and the +/- D port.

2.13 Polarity correction

The Gig PHYTER will automatically detect and correct for polarity reversal in wiring between the +/- wires for each of the 4 ports.

2.14 Power Supply Filtering

It is suggested that the PCB have at least one solid ground plane and one solid 3.3 V plane with no breaks in either plane. The interplane capacitance between the 3.3 V and ground planes should be maximized by minimizing the distance between the two planes. Filling unused signal planes with copper and connecting them to the proper power plane will also increase the interplane capacitance. The interplane capacitance acts like a short at high frequencies to reduce supply plane impedance.

The 3.3 V supply pins come in pairs with their corresponding ground pins (e.g. a 3.3 V supply-ground pair is formed by pin 2 [RA_AV_{DD}] and pin 3 [RA_A_{GND}]). These paired pins are physically adjacent to each other. The matching pins should be bypassed with low impedance surface mount capacitors of value 0.1 µF connected directly into the power planes with vias as close as possible to the pins. This will reduce the lead length (inductance) in series with the bypass capacitor. Any increase in lead length inductance will lower the capacitor's self resonant frequency which will degrade the high frequency performance of the capacitor.

The Analog PGM supply requires special filtering to attenuate high frequencies. High frequencies will increase the jitter of the PGM. We recommend a low pass filter formed by a 18-20 Ω resistor and two capacitors in parallel. One of the capacitors should be 22 µF and the other 0.01 µF. (This will implement a single pole low pass filter with 3 dB point around 360 Hz. The max. current on this supply poin is 5 mA.) The suggested connection is shown in Figure 4.

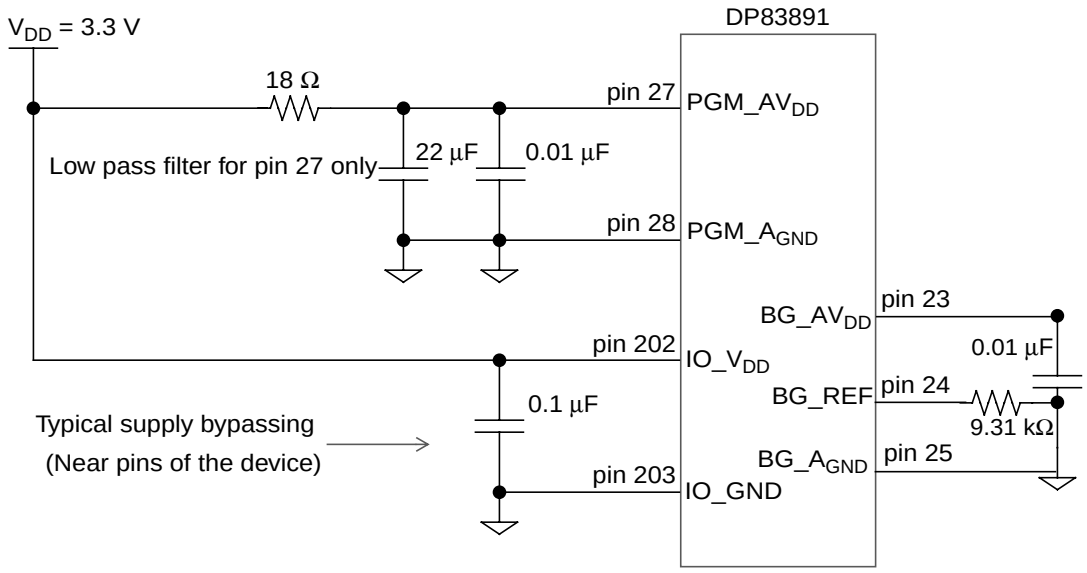


Figure 4. Example Power Supply Filtering

A 10 µF capacitor should also be placed close to the DP83891 (possibly on the bottom side of the PCB) bypassing the V_{DD} and ground planes.

For more details of how to filter supplies, please see "DP83891 Design Guide" or "DP83891 Reference Design Schematics".

In summary the following guide lines for power should be followed:

— Solid 3.3 V supply and ground planes. If there are two or more supply plane layers on the PCB, then one of these planes could be dedicated to the Analog supply pins. See Reference Design Schematics for an example.

— Make interplane capacitance between 3.3V supply and ground planes as large as possible. (i.e. Fill unused signal planes with copper and tie to appropriate power plane. Minimize thickness of separation between the ground and supply planes on the PCB.)

— Connect capacitors and IC pins directly into power planes with vias as close as possible to the IC pins.

— The PGM requires special bypassing.

3.0 Functional Description

The DP83891 is a full featured 10/100/1000 Ethernet Physical layer chip consisting of digital 10/100/1000 Mb/s core which is integrated into a single device with a common TP interface, combined MII/GMII controller interface and Mgmt. interface.

3.1 1000BASE-T Functional Description

The 1000BASE-T transceiver consisting of a PCS Transmitter, PMA Transmitter, PMA Receiver and a PCS Receiver is shown below (Figure 5.) in functional block diagram form.

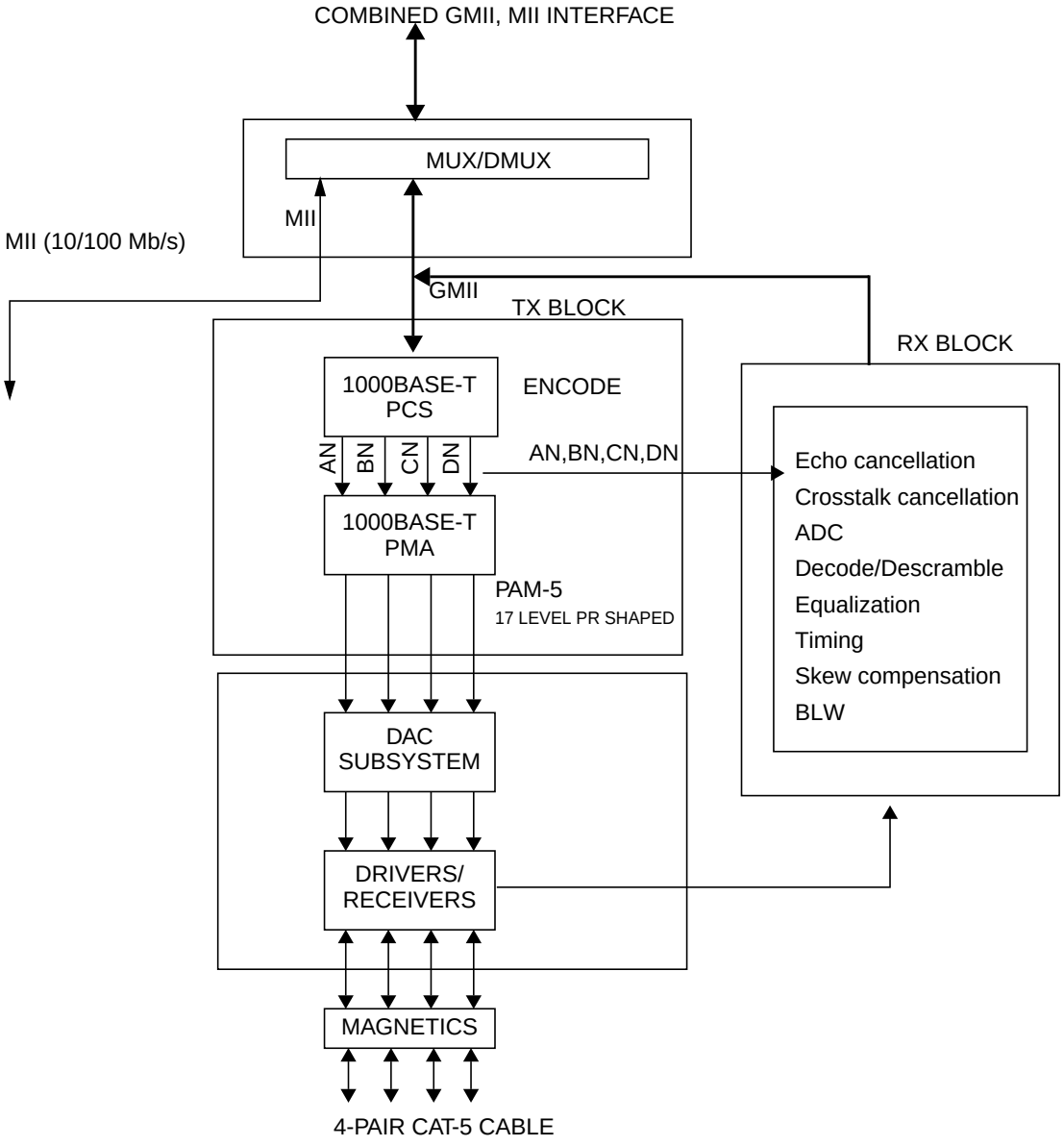


Figure 5. 1000BASE-T Functional Block Diagram

3.2 1000BASE-T PCS TX

The PCS transmitter consists of several functional blocks that convert the 8-bit TXD_n data from the GMII to PAM-5 symbols to be passed onto the PMA (Physical Medium Attachment) function. The block diagram of the PCS transmitter data path functions in Figure 6, provides an overview of each of the functional blocks within the PCS transmitter.

The transmitter consists of eight functional blocks:

— LFSR (Linear Feedback Shift Register)

— Data scrambler and symbol sign scrambler word generator

— Scrambler bit generator

— Data scrambler

— Convolutional encoder

— Bit-to-symbol quinary symbol mapping

— Sign scrambler nibble generator

— Symbol sign scrambler

The requirements for the PCS transmit functionality are also defined in the IEEE 802.3ab specification section 40.3.1.3 “PCS Transmit function”.

3.2.1 Linear Feedback Shift Register (LFSR)

The side-stream scrambler function uses a LFSR implementing one of 2 equations, based on the mode of operation being either a master or a slave. For master operation, the equation is as follows:

$g_M(x) = 1 + x^{13} + x^{33}$

For slave operation, use the equation:

$g_S(x) = 1 + x^{20} + x^{33}$

The 33-bit data output, $Scr_n[32:0]$, of this block is then fed into the data scrambler and symbol sign scrambler word generator.

3.2.2 Data and Symbol Sign Scrambler Word Generator

The word generator uses the $Scr_n[32:0]$ to generate further scrambled values. The following signals are generated: $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$.

The 4-bit $Sx_n[3:0]$ and $Sy_n[3:0]$ values are then fed into the scrambler bit generator. The 4-bit $Sg_n[3:0]$ sign values are fed into the sign scrambler nibble generator.

3.2.3 Scrambler Bit Generator

This function uses the Sx_n and Sy_n signals along with the tx_mode and tx_enable signals to generate the $Sc_n[7:0]$, which is further scrambled based on the condition of the tx_mode and tx_enable signal. The tx_mode signal can indicate sending idles (SEND_I), sending zeros (SEND_Z) or sending idles/data (SEND_N). The tx_mode signal is generated by the micro controller function. The tx_enable signal is either asserted to indicate data transmission is occurring or not asserted for no data transmission. The PCS Data Transmission Enable state machine generates the tx_enable signal.

The 8-bit $Sc_n[7:0]$ signals are then fed into the data scrambler functional block.

3.2.4 Data Scrambler

This function generates scrambled data by accepting the $TxD_n[7:0]$ data from the GMII and scrambling it based on various inputs.

The data scrambler generates the 8-bit $Sd_n[7:0]$ value, which scrambles the TxD_n data based primarily on the Sc_n values and the accompanying control signals.

All 8-bits of $Sd_n[7:0]$ are passed into the bit-to-quinary symbol mapping block, while 2-bits, $Sd_n[7:6]$, are fed into the convolutional encoder.

3.2.5 Convolutional Encoder

The encoder uses $Sd_n[7:6]$ bits and tx_enable to generate an additional data bit, which is called $Sd_n[8]$.

The one clock delayed versions $cs_{n-1}[1:0]$ are passed into the data scrambler functional block. This $Sd_n[8]$ bit is then passed into the bit-to-symbol quinary symbol mapping function.

3.2.6 Bit-to-Symbol Quinary Symbol Mapping

This function implements Table 40-1 and 40-2 Bit-to-Symbol Mapping for even and odd subsets, located in the IEEE 802.3ab specification. It takes the 9-bit $Sd_n[8:0]$ data and converts it to the appropriate quinary symbols as defined by the tables.

The output of this functional block generates the TA_n, TB_n, TC_n, and TD_n symbols, which are then passed into the symbol sign scrambler.

Before describing the symbol sign scrambler, the sign scrambler nibble generator is described, since this also feeds the symbol sign scrambler.

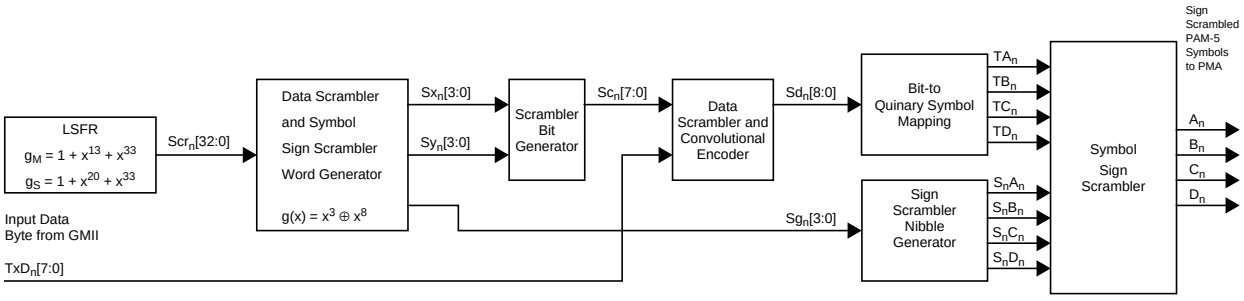


Figure 6. PCS TX Functional Block Diagram

3.2.7 Sign Scrambler Nibble Generator

This function performs some further scrambling of the sign values, $Sg_n[3:0]$, generated by the data scrambler and symbol sign scrambler word generator. This sign scrambling is dependent on the tx_enable signal.

The S_nA_n, S_nB_n, S_nC_n, and S_nD_n outputs are then fed into the symbol sign scrambler function.

3.2.8 Symbol Sign Scrambler

This function scrambles the sign of the TA_n, TB_n, TC_n, and TD_n input values from the bit-to-symbol quinary symbol mapping function, by either inverting or not inverting the signs. This is done as follows:

$A_n = TA_n \times S_nA_n$

$B_n = TB_n \times S_nB_n$

$C_n = TC_n \times S_nC_n$

$TD_n = TD_n \times S_nD_n$

The output of this functional block, which are A_n, B_n, C_n, and D_n are the sign scrambled PAM-5 symbols. They are then passed onto the PMA for further processing.

3.3 1000BASE-T PMA TX Block

The PMA transmit block shown in Figure 7 contains the following blocks:

— Partial Response Encoder

— 100/1000 DAC Line Driver

3.3.1 Partial Response Encoder

Partial Response (PR) coding (shaping) is used on the PAM-5 coded signals to spectrally shape the transmitted PAM-5 signal in order to reduce emissions in the critical frequency band ranging from 30 MHz to 60 MHz. The PR Z-transform implemented is:

$$0.75 + 0.25\ Z^{-1}$$

The result of the PR coding on the PAM-5 signal results in 17-level PAM-5 or PAM-17 signal that is used to drive a common 100/1000 DAC and line driver. (Without the PR coding each signal can have 5 levels given by $\pm 1, \pm 0.5$ and 0 V. If all combinations of the 5 levels are used for the present and previous outputs, then a simple table shows that there are 17 unique outputs levels when PR coding is used.)

Figure 7 shows the PMA Transmitter and the embedded PR encoder block with its inputs and outputs. Figure 8 shows the effect on the spectrum of PAM-5 after PR shaping.

3.3.2 100/1000 DAC Line Driver

The PAM-17 information from the PR encoder is used to drive a common 100/1000 DAC and line driver that converts digital data to suitable analog line voltages.

3.4 PMA Receiver

The PMA Receiver (the “Receiver”) consists of several functional blocks that process the four digitized voltage waveforms representing the received quartet of quinary PAM-5 symbols. The DSP processing implemented in the receiver extracts a best estimate of the quartet of quinary symbols originated by the transmitter at the far end of the CAT-5 cable and delivers them to the PCS RX block for further processing. There are four separate Receivers, one for each twisted pair.

The main processing blocks include:

— Adaptive Equalizer

— Echo and Crosstalk Cancellers

— Automatic Gain Control (AGC)

— Baseline Wander (BLW) Correction

— Slicer

3.4.1 Adaptive Equalizer

The Adaptive Equalizer compensates for the cable's non-ideal (i.e., not flat) frequency vs. attenuation characteristics which results in signal distortion. The cable attenuates the higher frequencies more than the lower frequencies, and this attenuation difference must be equalized. The Adaptive Equalizer is a digital filter with tap coefficients continually adapted to minimize the (Mean Square Error) MSE value of the slicer's error signal output. Continuous adaptation of the equalizer coefficients means that the optimum set of coefficients will always be achieved for any given length or quality of cable.

3.4.2 Echo and Crosstalk Cancellers

The Echo and Crosstalk Cancellers cancel the echo and crosstalk produced while transmitting and receiving simultaneously. Echo is produced when the transmitted signal interferes with the received signal on the same wire. Crosstalk is caused by the transmitted signal on each of the other three wire pairs interfering with the receive signal of the fourth wire pair. An Echo and Crosstalk Canceller is needed for each of the wire pairs.

3.4.3 Automatic Gain Control (AGC)

The Automatic Gain Control acts upon the output of the Echo and Crosstalk Cancellers to adjust the receiver gain. Different AGC methods are available within the chip and the optimum one is selected based on the operational state the chip (master, slave, start-up, etc.).

3.4.4 Baseline Wander (BLW) Correction

Baseline wander is the slow variation of the DC level of the incoming signal due to the non-ideal electrical characteristics of the magnetics and the inherent DC component of the transmitted waveform. The BLW correction circuit utilizes the slicer error signal to estimate and then correct for BLW.

3.4.5 Slicer

The Slicer selects the PAM-5 symbol value (+2,+1,0,-1,-2) closest to the voltage input value after the signal has been corrected for line Inter Symbol Interference (ISI), attenuation, echo, crosstalk and BLW.

The slicer produces an error output and symbol value decision output. The error output is the difference between the actual voltage input and the ideal voltage level representing the symbol value. The error output is fed back to the BLW, AGC, Crosstalk Canceller and Echo Canceller blocks to be used in their respective algorithms.

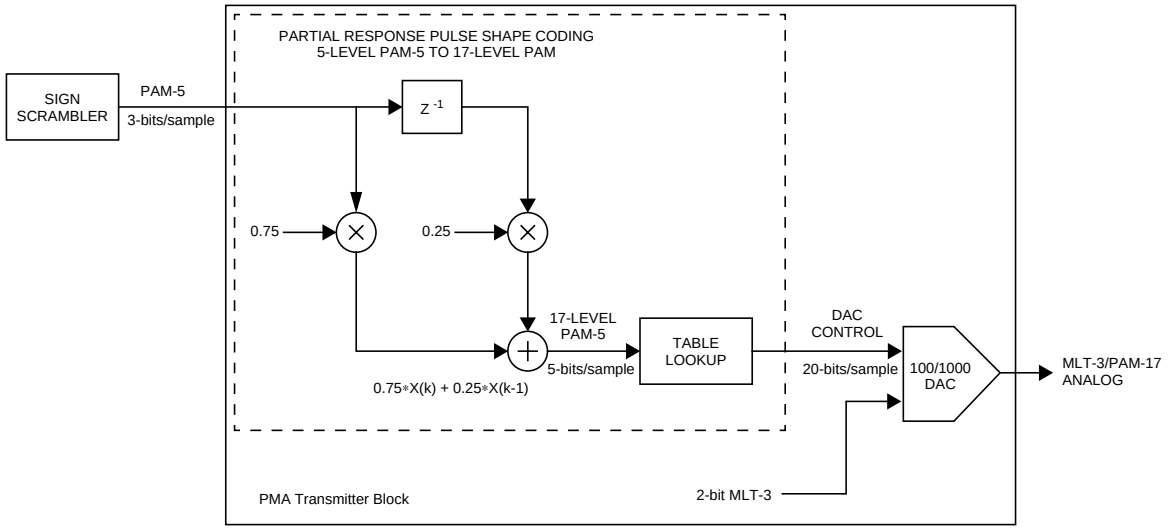


Figure 7. PMA Transmitter Block

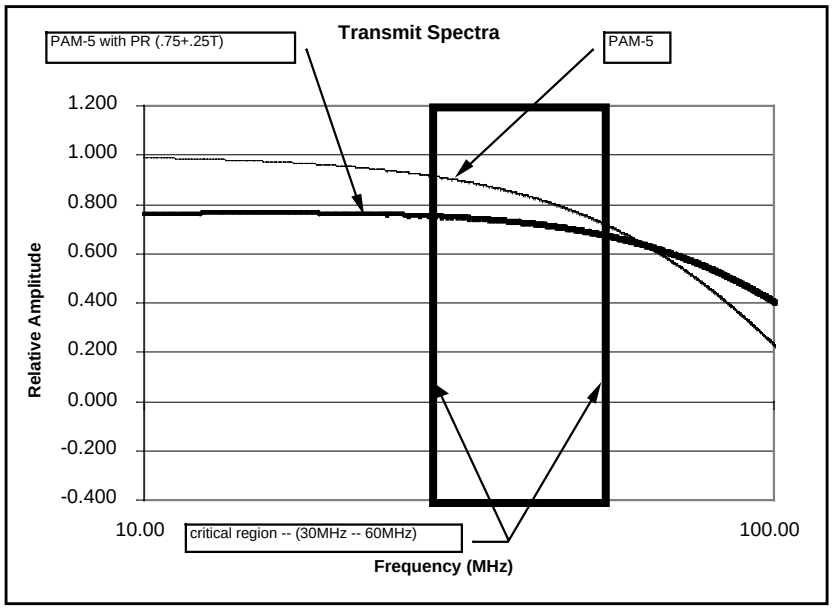


Figure 8. Effect on Spectrum of PR-shaped PAM-5 coding

3.5 1000BASE-T PCS RX

The PCS receiver consists of several functional blocks that convert the incoming quartet of quinary symbols (PAM-5) data from the PMA RX A, B, C, and D to 8-bit receive data (RXD[7:0]), data valid (RX_DV), and receive error (RX_ER) signals on the GMII. The block diagram of the 1000BASE-T Functional Block in Figure 5 provides an overview of the 1000BASE-T transceiver and shows the functionality of the PCS receiver.

The major functional blocks of the PCS Receiver include:

— Delay Skew Compensation

— Delay Skew Control

— Forward Error Correction (FEC)

— Descrambler Subsystem

— Receive State Machine

The requirements for the PCS receive functionality are also defined in the IEEE 802.3ab specification in section 40.3.1.4 “PCS Receive function”.

3.5.1 Delay Skew Compensation

This function is used to align the received data from the four PMA receivers and to determine the correct spacial ordering of the four incoming twisted pairs, i.e., which twisted pair carries A_n, which one carries B_n, etc. The de-skewed and ordered symbols are then presented to the Forward Error Correction (FEC) Decoder. The differential time or time delay skew is due to the differences in length of each of the four pairs of twisted wire in the CAT-5 cable, manufacturing variation of the insulation of the wire pairs,

and in some cases, differences in insulation materials used in the wire pairs. Correct symbol order to the FEC is required, since the receiver does not have prior knowledge of the order of the incoming twisted pairs within the CAT-5 cable.

3.5.2 Delay Skew Control

This function controls the delay skew compensation function by providing the necessary controls and selects to allow for compensation in two dimensions. The two dimensions being time and position. The time factor is the delay skew between the four incoming data streams from the PMA RX A, B, C, and D. This delay skew originates back at the input to the ADC/DAC/TIMING subsystem. Since the receiver initially does not know the ordering of the twisted pairs, correct ordering must be determined automatically by the receiver during start-up. Delay skew compensation and twisted pair ordering is part of the training function performed during start-up mode of operation.

3.5.3 Forward Error Correction (FEC) Decoder

This function decodes the quartet of quinary symbols from the PMA receivers and generates the Sd_n binary values. The FEC decoder uses a standard 8 state Trellis code operation.

The FEC decoder decodes the quartet of quinary (PAM-5) symbols and generates the corresponding Sd_n binary words. Initially, Sd_n[3:0] may not have the proper bit ordering, however, correct ordering is established by the reordering algorithm at start-up.

3.5.4 Descrambler Subsystem

The descrambler block performs the reverse scrambling function that was implemented in the transmit section. This function works in conjunction with the delay skew control. It provides the receiver generated Sd_n[3:0] bits for comparison in the delay skew control function.

3.5.5 Receive State Machine

This state machine operation is defined in IEEE 802.3ab section 40.3.1.4. In summary, it provides the necessary receive control signals of RX_DV and RX_ER to the GMII. In specific conditions, as defined in the IEEE 802.3ab specification, it will generate RXD[7:0] data.

3.6 Gigabit MII (GMII)

The Gigabit Media Independent Interface (GMII) is intended for use between Ethernet PHYs and Station Management (STA) entities and is selected by either hardware or software configuration. The purpose of this interface is to differentiate between the various media that are transparent to the MAC layer.

The GMII Interface accepts either GMII or MII data, control and status signals and routes them either to the 1000BASE-T or 100BASE-TX modules, respectively.

The mapping between GMII and MII is illustrated below in Table 4.

Table 4. GMII/MII Mapping

GMII	MII
RXD[3:0]	RXD[3:0]
RXD[4:7]	
RX_DV	RX_DV
RX_ER	RX_ER
RX_CLK	RX_CLK
	TX_CLK
TXD[3:0]	TXD[3:0]
TXD[4:7]	
TX_EN	TX_EN
TX_ER	TX_ER
GTX_CLK	
COL	COL
CRS	CRS

The GMII interface has the following characteristics:

— Supports 100/1000 Mb/s operation

— Data and delimiters are synchronous to clock references

— Provides independent 8-bit wide transmit and receive data paths

— Provides a simple management interface

— Uses signal levels that are compatible with common CMOS digital ASIC processes and some bipolar processes

— Provides for full duplex operation

The GMII interface is defined in the IEEE 802.3z document Clause 35. In each direction of data transfer, there are Data (an eight-bit bundle), Delimiter, Error, and Clock signals. GMII signals are defined such that an implementation may multiplex most GMII signals with the similar PCS service interface defined in IEEE 802.3u Clause 22.

Two media status signals are provided. One indicates the presence of carrier (CRS), and the other indicates the occurrence of a collision (COL). The GMII uses the MII management interface composed of two signals (MDC, MDIO) which provide access to management parameters and services as specified in IEEE 802.3u Clause 22.

The MII signal names have been retained and the functions of most signals are the same, but additional valid combinations of signals have been defined for 1000 Mb/s operation.

The Reconciliation sublayer maps the signal set provided at the GMII to the PLS service primitives provided to the MAC.

3.7 ADC/DAC/Timing Subsystem

The 1000BASE-T receive section consists of 4 channels, each receiving IEEE 802.3ab compliant PAM-5 coded data including Partial Response (PR) shaping at 125 MBaud over a maximum of a 100 m of CAT-5 cable. The 4 pairs of receive input pins are AC coupled through the magnetics to the CAT-5 cable. Each receive pin pair is differentially terminated into an external 100Ω resistor to match the cable

impedance. Each receive channel consists of a high precision Analog to Digital data converter (ADC) which quantizes the incoming data into a digital word at the rate of 125 Mb/s. The ADC is sampled with a clock of 125 MHz which has been recovered from the incoming data stream.

The 1000BASE-T transmit section consists of 4 channels, each transmitting IEEE 802.3ab compliant 17-level PAM-5 data at 125 M symbols/second. The 4 pairs of transmit output pins are AC coupled through the magnetics to the CAT-5 cable. Each transmit pin pair is differentially terminated into an external 100Ω resistor to match the cable impedance. Each transmit channel consists of a Digital to Analog data converter (DAC) and line driver capable of producing 17 discrete levels corresponding to the PR shaping of a PAM-5 coded data stream. Each DAC is clocked with a 125 MHz clock which is the X1/Ref clock in the MASTER mode of operation, and the recovered receive clock in the SLAVE mode of operation.

The DP83891 incorporates a sophisticated Clock Generation Module (CGM) which supports 100/1000 modes of operation with an external 125 MHz clock reference (±50 ppm). The Clock Generation module internally generates multiple phases of clocks at various frequencies to support high precision and low jitter Clock Recovery Modules (CRM) for robust data recovery, and to support accurate low jitter transmission of data symbols in the MASTER and SLAVE mode of operation.

3.8 100BASE-TX TRANSMITTER

The 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a scrambled MLT-3 125 Mb/s serial data stream. Because the 100BASE-TX TP-PMD is integrated with the 1000BASE-T, the differential output pins, TD+ /– are routed to channel A of the AC coupling magnetics.

The block diagram in Figure 9 provides an overview of each functional block within the 100BASE-TX transmit section.

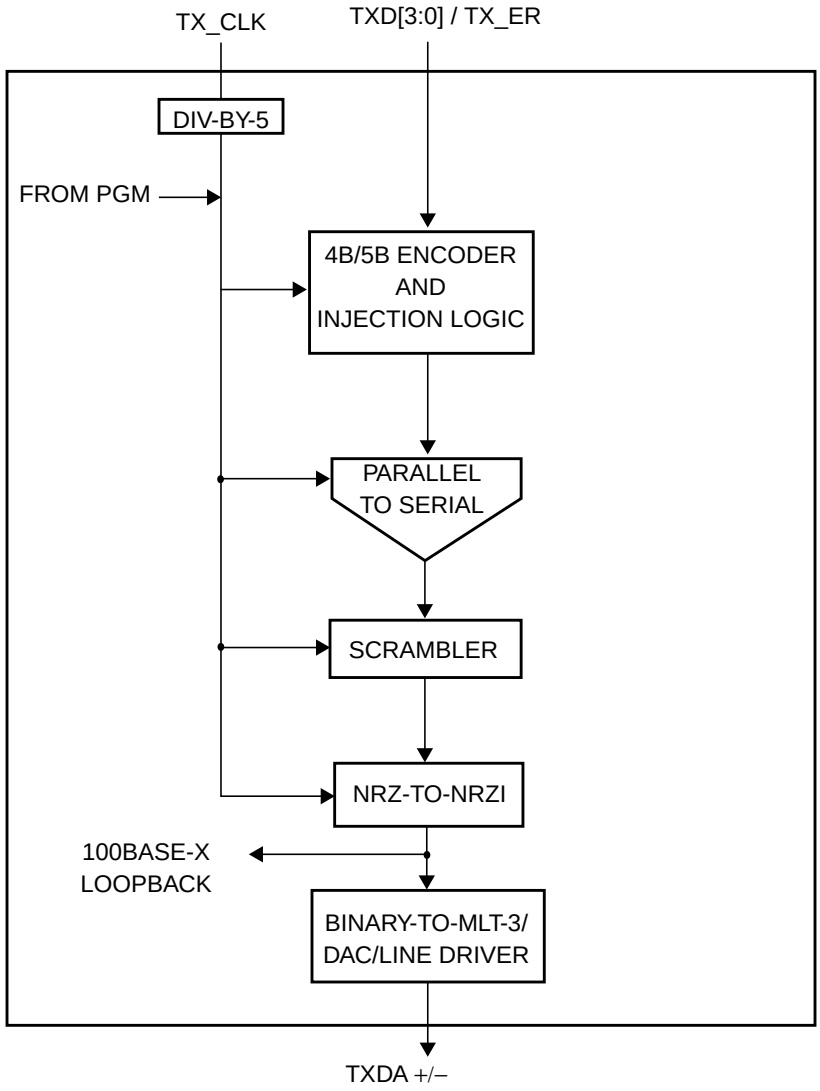


Figure 9. 100BASE-TX Transmit Block Diagram

The Transmitter section consists of the following functional blocks:

— Code-group Encoder and Injection block

— Parallel-to-Serial block

— Scrambler block

— NRZ to NRZI encoder block

— Binary to MLT-3 converter / DAC / Line Driver

The DP83891 implements the 100BASE-X transmit state machine diagram as specified in the IEEE 802.3u Standard, Clause 24.

3.8.1 Code-group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 5 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of Transmit Enable signal from the MAC, the code-group encoder injects the T/R code-group pair (01101 00111) indicating the end of frame.

After the T/R code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (reassertion of Transmit Enable).

3.8.2 Parallel-to-Serial Converter

The 5-bit (5B) code-groups are then converted to a serial data stream at 125 MHz.

3.8.3 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted pair cable (for 100BASE-TX applications). By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the PMD and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (e.g., continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORed with the serial NRZ data from the serializer block. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB. The DP83891 uses the PHY_ID (pins PHYAD [4:0]) to set a unique seed value for the scramblers. The resulting energy generated by each channel is out of phase with respect to each channel, thus reducing the overall electromagnetic radiation.

3.8.4 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data is NRZI encoded to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable. There is no ability to bypass this block within the DP83891.

Table 5. 4B5B Code-Group Encoding/Decoding

Name	PCS 5B Code-group	MII 4B Nibble Code
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000 (Note 1)
J	11000	First Start of Packet - 0101 (Note 1)
K	10001	Second Start of Packet - 0101 (Note 1)
T	01101	First End of Packet - 0000 (Note 1)
R	00111	Second End of Packet - 0000 (Note 1)
INVALID CODES		
V	00000	0110 or 0101 (Note 2)
V	00001	0110 or 0101 (Note 2)
V	00010	0110 or 0101 (Note 2)
V	00011	0110 or 0101 (Note 2)
V	00101	0110 or 0101 (Note 2)
V	00110	0110 or 0101 (Note 2)
V	01000	0110 or 0101 (Note 2)
V	01100	0110 or 0101 (Note 2)
V	10000	0110 or 0101 (Note 2)
V	11001	0110 or 0101 (Note 2)

Note 1: Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

Note 2: Normally, invalid codes (V) are mapped to 6h on RXD[3:0] with RX_ER asserted.

3.8.5 MLT-3 Converter / DAC / Line Driver

The Binary to MLT-3 conversion is accomplished by converting the serial NRZI data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then passed to a 100/1000 DAC and line driver which converts the pulses to suitable analog line voltages. Refer to Figure 10.

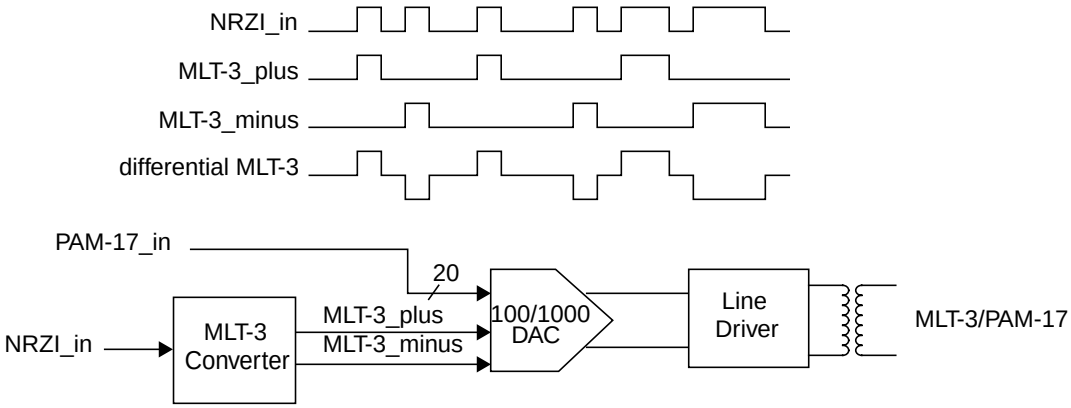


Figure 10. NRZI to MLT-3 conversion

The 100BASE-TX MLT-3 signal sourced by the TXDA+/– line driver output pins is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD Standard compliant transition times (3 ns < t_r < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83891 is capable of sourcing only MLT-3 encoded data. Binary output from the TXDA+/– outputs is not possible in 100 Mb/s mode.

3.8.6 TX_ER

Assertion of the TX_ER input while the TX_EN input is also asserted will cause the DP83891 to substitute HALT code-groups for the 5B data present at TXD[3:0]. However, the Start-of-Stream Delimiter (SSD) /J/K/ and End-of-Stream Delimiter (ESD) /T/R/ will not be substituted with HALT code-groups. As a result, the assertion of TX_ER while TX_EN is asserted will result in a frame properly encapsulated with the /J/K/ and /T/R/ delimiters which contains HALT code-groups in place of the data code-groups.

3.9 100BASE-TX RECEIVER

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mb/s serial data stream to synchronous 4-bit nibble data that is provided to the MII. Because the 100BASE-TX TP-PMD is integrated with the 1000BASE-T, the differential input data RXDB+/– is routed from channel B of the AC coupling magnetics.

See Figure 11 for a block diagram of the 100BASE-TX receive function. This provides an overview of each functional block within the 100BASE-TX receive section.

The Receive section consists of the following functional blocks:

— ADC Block
— Signal Detect
— BLW/EQ/AAC Correction
— Clock Recovery Module
— MLT-3 to NRZ Decoder
— Descrambler (bypass option)
— Serial to Parallel
— 5B/4B Decoder (bypass option)
— Code Group Alignment
— 4B/5B Decoder
— Link Integrity Monitor
— Bad SSD Detection

3.9.1 ADC Block

The DP83891 requires no external attenuation circuitry at its receive inputs, RXDB+/–. It accepts TP-PMD compliant waveforms directly, requiring only a 100Ω termination plus a simple 1:1 transformer. The analog MLT-3 signal (with noise and system impairments) is received and converted to the digital domain via an Analog to Digital Converter (ADC) to allow for Digital Signal Processing (DSP) to take place on the received signal.

3.9.2 Signal Detect

The signal detect function of the DP83891 is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard for both voltage thresholds and timing parameters.

Note: the reception of fast link pulses per IEEE 802.3u Auto-Negotiation by the 100BASE-X receiver will not cause the DP83891 to assert signal detect.

3.9.3 BLW / EQ / AAC Correction

The digital data from the ADC block flows into the DSP Block (BLW/EQ/AAC Correction) for processing. The DSP block applies proprietary processing algorithms to the received signal and are all part of an integrated DSP receiver. The primary DSP functions applied are:

— BLW can generally be defined as the change in the average DC content, over time, of an AC coupled digital transmission over a given transmission medium. (i.e. copper wire). BLW results from the interaction between the low frequency components of a transmitted bit

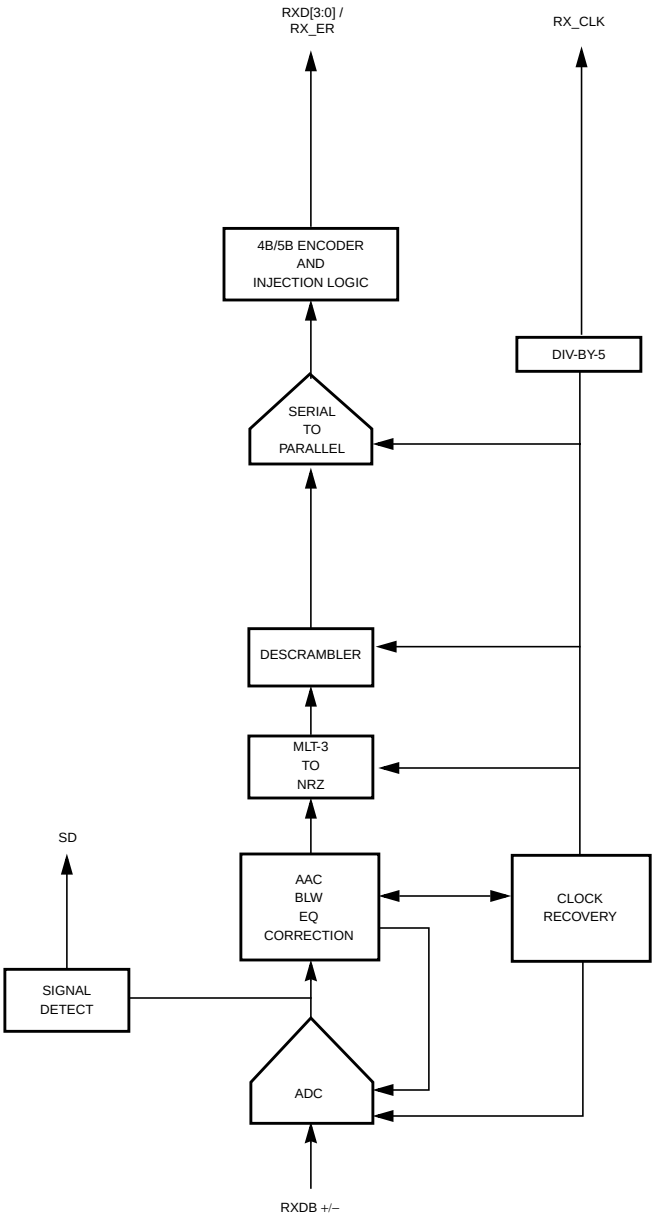


Figure 11. Receive Block Diagram

stream and the frequency response of the AC coupling component(s) within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformer then the droop characteristics of the transformer will dominate resulting in potentially serious BLW. The digital oscilloscope plot provided in Figure 12 illustrates the severity of the BLW event that can theoretically be generated during 100BASE-TX packet transmission. This event consists of approximately 800 mV of DC offset for a period of 120 µs. Left uncompensated, events such as this can cause packet loss.

— In high-speed twisted pair signalling, the frequency content of the transmitted signal can vary greatly during normal operation based primarily on the randomness of the scrambled data stream and is thus susceptible to frequency dependent attenuation (see Figure 13). This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the transmission. In order to ensure quality transmission when using MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will over-compensate for shorter, less attenuating lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

— Automatic Attenuation Control (AAC) allows the DSP block to fit the resultant output signal to match the limit characteristic of its internal decision block to ensure error free sampling.

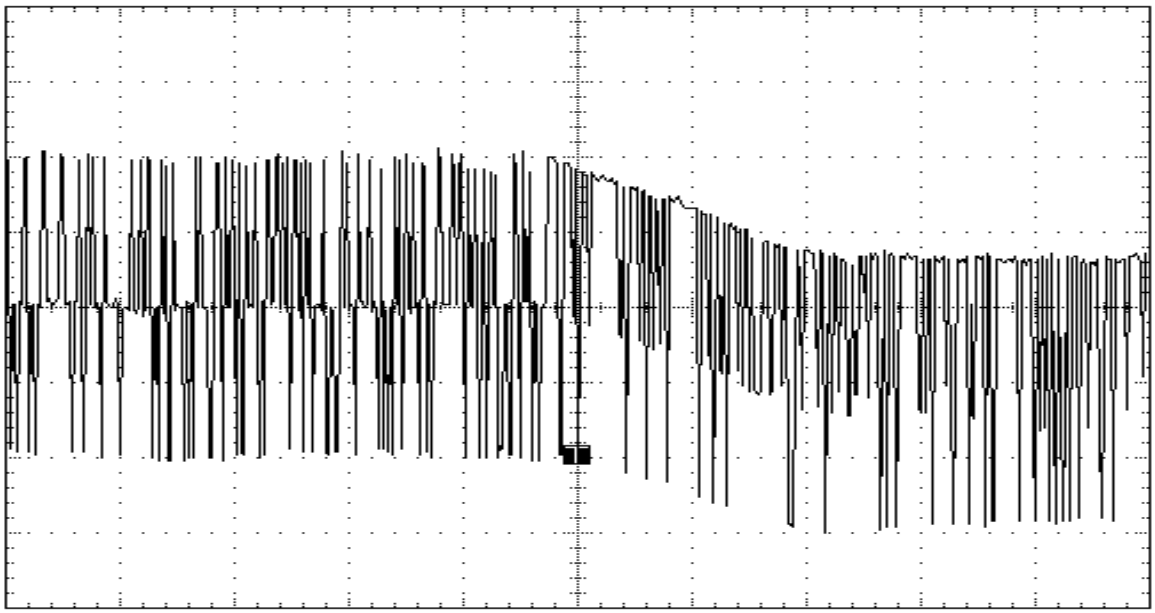


Figure 12. 100BASE-TX BLW Event

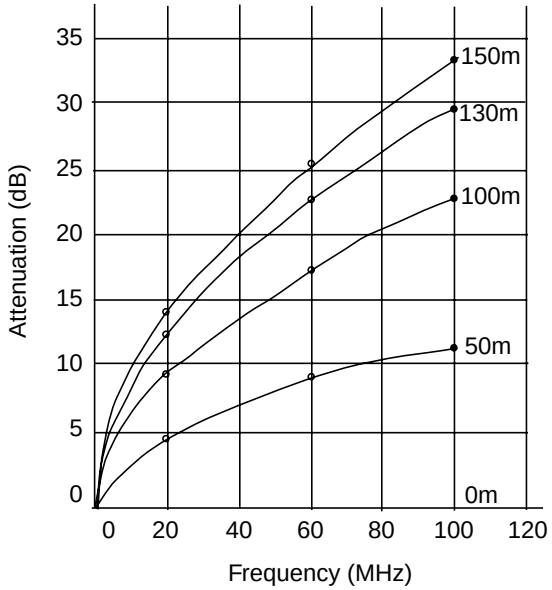


Figure 13. EIA/TIA Attenuation vs. Frequency for 0, 50, 100, 130 & 150 meters of CAT 5 cable

3.9.4 Clock Recovery Module

The Clock Recovery Module (CRM) uses the output information from the DSP Block to generate a phase corrected 125 MHz clock for the 100BASE-T receiver.

The CRM is implemented using an advanced digital Phase Locked Loop (PLL) architecture that replaces sensitive analog circuitry. Using digital PLL circuitry allows the DP83891 to be manufactured and specified to tighter tolerances.

3.9.5 MLT-3 to NRZ Decoder

The DP83891 decodes the MLT-3 information from the DSP block to binary NRZI form and finally to NRZ data.

3.9.6 Descrambler

A serial descrambler is used to de-scramble the received NRZ data. The descrambler has to generate an identical data scrambling sequence (N) in order to recover the original unscrambled data (UD) from the scrambled data (SD) as represented in the equations:

$$SD = (UD \oplus N)$$
$$UD = (SD \oplus N)$$

Synchronization of the descrambler to the original scrambling sequence (N) is achieved based on the knowledge that the incoming scrambled data stream consists of scrambled IDLE data. After the descrambler has recognized 12 consecutive IDLE code-groups, where an unscrambled IDLE code-group in 5B NRZ is equal to five consecutive ones (11111), it will synchronize to the receive data stream and generate unscrambled data in the form of unaligned 5B code-groups.

In order to maintain synchronization, the descrambler must continuously monitor the validity of the unscrambled data that it generates. To ensure this, a line state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler the hold timer starts a 722 µs countdown. Upon detection of sufficient IDLE code-groups (16 idle symbols) within the 722 µs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the line state monitor does not recognize sufficient unscrambled IDLE code-groups within the 722 µs period, the entire descrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.9.7 Serial to Parallel Converter

The 100BASE-X receiver includes a Serial to Parallel converter this operation also provides code-group alignment, and operates on unaligned serial data from the descrambler (or, if the descrambler is bypassed, directly from the MLT-3 to NRZ decoder) and converts it into 5B code-group data (5 bits). Code-group alignment occurs after the J/K code-group pair is detected. Once the J/K code-group pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.9.8 4B/5B Decoder

The code-group decoder functions as a look up table that translates incoming 5B code-groups into 4B nibbles. The code-group decoder first detects the J/K code-group pair preceded by IDLE code-groups and replaces the J/K with MAC preamble. Specifically, the J/K 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5B code-groups are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the T/R code-group pair denoting the End of Stream Delimiter (ESD) or with the reception of a minimum of two IDLE code-groups.

3.9.9 100BASE-X Link Integrity Monitor

The 100BASE-X Link monitor ensures that a valid and stable link is established before enabling both the Transmit and Receive PCS layer. Signal Detect must be valid for at least 500 μs to allow the link monitor to enter the “Link Up” state, and enable transmit and receive functions.

Signal detect can be forced active by setting Bit 4 of the ECTRL1 register 10h. Additionally, Signal Detect can be ANDed with the descrambler locked indication by setting Bit 3 of the EXTRL1 register. With bit 3 set, the descrambler “Locked” is required to enter the Link Up state, but only Signal Detect is required to maintain the link in the Link Up state.

3.9.10 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K.

If this condition is detected, the DP83891 will assert RX_ER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected.

Once at least two IDLE code groups are detected, RX_ER and CRS become de-asserted.

3.10 10BASE-T Functional Description

3.10.1 Smart Squelch

The Smart Squelch is responsible for determining when valid data is present on the RXDB+/- differential receive inputs. The Transceiver implements an intelligent receive squelch on the RX differential inputs to ensure that noise on the receive inputs will not be mistaken for a valid signal.

The squelch circuitry employs a combination of amplitude and timing measurements to determine the validity of data on the twisted pair inputs. The operation of the smart squelch is shown in Figure 14.

The signal at the start of packet is checked by the smart squelch and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will

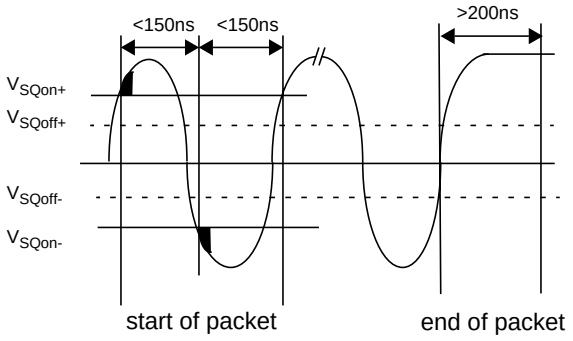


Figure 14. 10BASE-T Squelch Operation Diagram

be rejected. Once this first squelch level is overcome correctly the opposite squelch level must then be exceeded within 150 ns. Finally, the signal must exceed the original squelch level within an additional 150 ns to ensure that the input waveform will not be rejected. The checking procedure results in the loss of typically three bits at the beginning of each packet.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present. At this time, the smart squelch circuitry is reset.

Valid data is considered to be present until squelch level has not been generated for a time longer than 150 ns, indicating End of Packet.

3.10.2 Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity once valid data is detected via the Smart squelch function.

For 10 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mb/s Full Duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

3.10.3 Collision Detect and Heartbeat

A collision is detected on the twisted pair cable when the receive and transmit channels are active simultaneously while in half duplex mode.

Also after each transmission, the 10 Mb/s block will generate a Heartbeat signal by applying a 1 us pulse on the COL lines which go into the MAC. This signal is called the Signal Quality Error (SQE) and it’s function as defined by IEEE 802.3 is to assure the continued functionality of the collision circuitry.

3.10.4 Link Detector/Generator

The link generator is a timer circuit that generates a link pulse as defined by the 10 Base-T specification that will be sent by the transmitter section. The pulse which is 100ns wide is transmitted on the transmit output, every 16ms, in the absence of transmit data. The pulse is used to check the integrity of the connection to the remote MAU.

The link detection circuit checks for valid pulses from the remote MAU and if valid link pulses are not received the link detector will disable the twisted pair transmitter, receiver and collision detection functions.

3.10.5 Jabber

The Jabber function disables the transmitter if it attempts to transmit a much longer than legal sized packet. The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than 20-30ms. The transmitter is then disabled for the entire time that the ENDEC module's internal transmit is asserted. The transmitter signal has to be deasserted for approximately 400-600ms (the unjab time) before the Jabber re-enables the transmit outputs.

There is also a jabber disable bit in the 10TOPR register (bit 5), which when activated, disables the jabber function.

3.10.6 Transmit Driver

The 10 Mb/s transmit driver in the Gig PHYTER, uses the 100/1000 Mb/s common driver.

3.11 ENDEC Module

The ENDEC consists of two major blocks:

— The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester, and transmits it differentially to the transceiver, through the differential transmit driver.

— The Manchester decoder receives Manchester data from the transceiver, converts it to NRZ data and recovers clock pulses and sends them to the controller.

3.11.1 Manchester Encoder and Differential Driver

The encoder begins operation when the Transmit Enable input (TXE) goes high and converts the clock and NRZ data to Manchester data for the transceiver. For the duration of TXE remaining high, the Transmit Data (TXD) is encoded for the transmit-driver pair (TX). TXD must be valid on the rising edge of Transmit Clock (TXC). Transmission ends when TXE goes low. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

3.11.2 Manchester Decoder

The decoder consists of a differential receiver and a PLL to separate the Manchester encoded data stream into internal clock signals and data. Once the input exceeds the squelch requirements, Carrier Sense (CRS) is asserted off the first edge presented to the decoder. Once the decoder has locked onto the incoming data stream, it provides data (RXD) and clock (RXC) to the MAC.

The decoder detects the end of a frame when no more mid-bit transitions are detected. Typically, within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for at least five more bit times after CRS goes low, to guarantee the receive timings of the controller.

3.12 802.3u MII

The DP83891 incorporates the Media Independent Interface (MII) as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 100 Mb/s mode. This section describes both the serial MII management interface as well as the nibble wide MII data interface.

The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHY(s).

The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC).

3.12.1 Serial Management Register Access

The serial management MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the management interface pins MDC and MDIO for both 100/1000 Mb/s operation. The DP83891 implements all the required MII registers as well as several optional registers. These registers are fully described in Section 3. A description of the serial management access protocol follows.

3.12.2 Serial Management Access Protocol

The serial control interface consists of two pins, Management Data Clock (MDC) and Management Data Input/Output (MDIO). MDC has a maximum clock rate of 2.5 MHz and no minimum rate. The MDIO line is bi-directional and may be shared by up to 32 devices. The MDIO frame format is shown below in Table 6.

The MDIO pin requires a pull-up resistor (1.5 kΩ) which, during IDLE and turnaround, will pull MDIO high. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the DP83891 with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pull-up resistor to pull the MDIO pin high during which time 32 MDC clock cycles are provided. In addition 32 MDC clock cycles should be used to re-sync the device if an invalid start, op code, or turnaround bit is detected.

The DP83891 waits until it has received this preamble sequence before responding to any other transaction. Once the DP83891 serial management port has been initialized no further preamble sequencing is required until after a power-on/reset, invalid Start, invalid Opcode, or invalid turnaround bit has occurred.

The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of Turnaround. The addressed DP83891 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 14 shows the timing relationship between MDC and the MDIO as driven/received by the Station (STA) and the DP83891 (PHY) for a typical register read access.

For write transactions, the station management entity writes data to the addressed DP83891 thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>. Figure 15 shows the timing relationship for a typical MII register write access.

3.12.3 Serial Management Preamble Suppression

The DP83891 supports a Preamble Suppression mode as indicated by a one in bit 6 of the Basic Mode Status Register (BMSR, address 01h.) If the station management entity (i.e., MAC or other management controller) determines that all PHYs in the system support Preamble Suppression by

Table 6. Typical MDIO Frame Format

MII Management Serial Protocol	<idle><start><op code><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

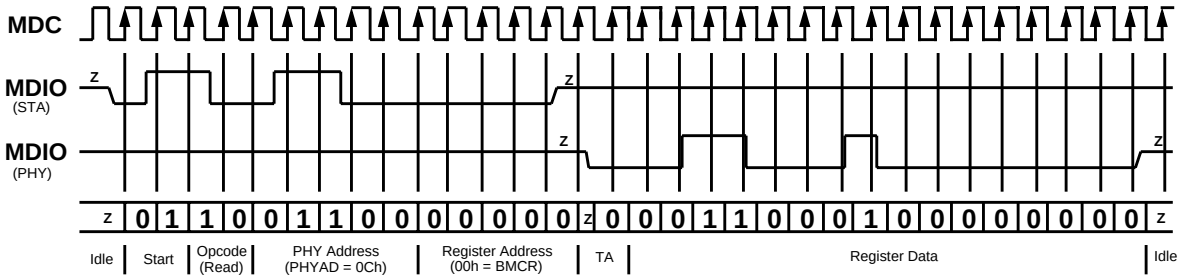


Figure 15. Typical MDC/MDIO Read Operation

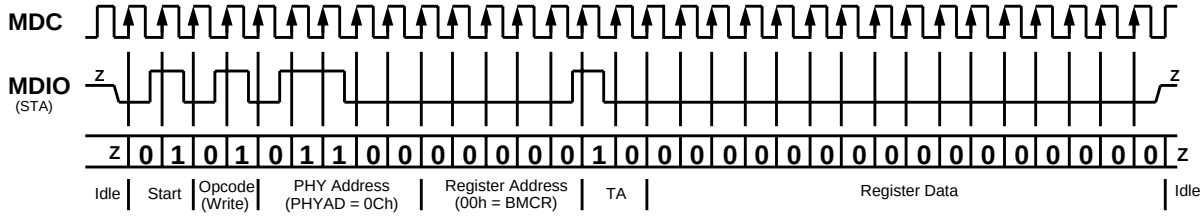


Figure 16. Typical MDC/MDIO Write Operation

returning a one in this bit, then the station management entity need not generate preamble for each management transaction.

The DP83891 requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by the mandatory pull-up resistor on MDIO in conjunction with a continuous MDC, or the management access made to determine whether Preamble Suppression is supported.

While the DP83891 requires an initial preamble sequence of 32 bits for management initialization, it does not require a full 32-bit sequence between each subsequent transaction. A *minimum of one idle bit between management transactions is required* as specified in IEEE 802.3u.

3.12.4 PHY Address Sensing

The DP83891 provides five PHY address pins, the information is latched into the ECTLR1 register (address 10h, bits [10:6]) at device power-up/reset. The DP83891 supports PHY Address strapping values 0 (<00000>) through 31 (<11111>). PHY Address 0 puts the part into Isolate Mode.

3.12.5 Nibble-wide MII Data Interface

Clause 22 of the IEEE 802.3u specification defines the Media Independent Interface. This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and indicate signals, allow for the simultaneous exchange of data between the DP83891 and the upper layer agent (MAC).

The receive interface consists of a nibble wide data bus RXD[3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at 25 MHz to support 100 Mb/s operation.

The transmit interface consists of a nibble wide data bus TXD[3:0], a transmit error flag TX_ER, a transmit enable control signal TX_EN, and a transmit clock TX_CLK operates at 25 MHz.

Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The COL signal asserts as an indication of a collision which can occur during half-duplex operation when both a transmit and receive operation occur simultaneously.

3.12.6 Collision Detect

For Half Duplex, a 100BASE-TX collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

3.12.7 Carrier Sense

Carrier Sense (CRS) may be asserted during 100 Mb/s operation when a valid link (SD) and two non-contiguous zeros are detected on the line.

For 100 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 100 Mb/s Full Duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

3.12.8 MII Isolate Mode

The DP83891 can be set to Isolate Mode by setting bit 10 in the BASIC MODE Control Register (00h) to 1.

With bit 10 in the BMCR set to one, the DP83891 does not respond to packet data present at TXD[3:0], TX_EN, and TX_ER inputs and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs. The DP83891 will continue to respond to all serial management transactions over the MDIO/MDC lines.

While in Isolate mode, the TXD+/– outputs are dependent on the current state of Auto-Negotiation. The DP83891 can Auto-Negotiate or parallel detect to a specific technology depending on the receive signal at the RXD+/– inputs. A valid link can be established for RXD even when the DP83891 is in Isolate mode.

It is recommended that the user have a basic understanding of Clause 22 of the 802.3u standard.

3.13 Status Information

There are 9 pins that are available to convey status information to the user through LEDs. The 9 pins indicate link status, collision status, duplex status, activity, device speed indication, and separate indications for Receive (RX) and transmit (TX) for the device.

LED_LNK status indicates Good Link Status for 100BASE-TX and 1000BASE-T.

100BASE-T: link is established as a result of an input receive amplitude compliant with TP-PMD specifications which will result in internal generation of Signal Detect. LED_LNK will assert after the internal Signal Detect has remained asserted for a minimum of 500 µs. LED_LNK will de-assert immediately following the de-assertion of the internal Signal Detect.

1000BASE-T: link is established as a result of training, Auto-Negotiation completed and valid 1000BASE-T link is established and reliable reception of signals transmitted from a remote PHY.

LED_COL status indicates that the PHY has detected a collision condition (simultaneous transmit and receive activity while in Half Duplex mode).

LED_ACT status indicates Receive or Transmit activity.

LED_10, LED_100, LED_1000 indicate the device speed:

LED_10	10 BASE-T
LED_100	100BASE-TX
LED_1000	1000BASE-T

LED_TX indicates that the PHY is transmitting.

LED_RX indicates that the PHY is receiving.

LED_DUPLEX on indicates that the Gig PHYTER is in Full-Duplex mode of operation.

4.0 Register Block

4.1 Register Definitions

Register maps and address definitions are given in the following tables:

Table 7. Register Block - DP83891 Register Map

Offset		Access	Tag	Description
Hex	Decimal			
0x00	0	RW	BMCR	Basic Mode Control Register
0x01	1	RO	BMSR	Basic Mode Status Register
0x02	2	RO	PHYIDR1	PHY Identifier Register #1
0x03	3	RO	PHYIDR2	PHY Identifier Register #2
0x04	4	RW	ANAR	Auto-Negotiation Advertisement Register
0x05	5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register
0x06	6	RW	ANER	Auto-Negotiation Expansion Register
0x07	7	RW	ANNPTR	Auto-Negotiation Next Page TX
0x08	8	RW	ANNPRR	Auto-Negotiation Next Page RX
0x09	9	RW	1KTCR	1000BASE-T Control Register
0x0A	10	RO	1KSTSR	1000BASE-T Status Register
0x0B-0x0E	11-14	RO	Reserved	Reserved
0x0F	15	RO	1KSCR	1000BASE-T Extended Status Register
0x10	16	RW	Strap_Reg	Strap Options Register
0x11	17	RO	PHY_SUP	PHY Support
0x12-0x14	18-20	RO	Reserved	Reserved
0x15	21	RW	MDIX_sel	MDIX select
0x16	22	RW	Expand_mem	Expanded Memory Access
0x17-0x1C	23-28	RO	Reserved	Reserved
0x1D	29	RW	Exp_mem_dat	Expanded Memory Data
0x1E	30	RW	Exp_mem_add	Expanded Memory Address
0x1F	31	RO	Reserved	Reserved

In the register definitions under the ‘Default’ heading, the following definitions hold true:

— RW = **R**ead **W**rite access
— RO = **R**ead **O**nly access
— L(H) = **L**atched and **H**eld until read, based upon the occurrence of the corresponding event
— SC = Register sets on event occurrence and **S**elf-**C**lears when event ends
— P = Register bit is **P**ermanently set to a default value
— COR = **C**lear **O**n **R**ead
— Strap[x] = Default value read from **Strap**ped value at device pin at Reset, where x may take the values:
[0] internal pull-down
[1] internal pull-up
[Z] no internal pull-up or pull-down, floating

4.2 Register Map

Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 0 (0x00) Basic Mode Control Register (BMCR)	Reset 0	Loopback 0	Speed [1] Selection Strap / 1 1	Auto-Neg Enable Strap / 1 1	Power Down 0	Isolate 0	Restart Auto-Neg 0	Duplex Mode Strap / 1	Collision Test 0	Speed[0] Selection Strap / 1 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 1 (0x01) Basic Mode Status Register (BMSR)	100BASE-T4 0	10BASE-TX Full-Duplex 1	10BASE-TX Half-Duplex 1	10BASE-T Full-Duplex 0	10BASE-T Half-Duplex 0	10BASE-T2 Full-Duplex 0	10BASE-T2 Half-Duplex 0	1000BASE-T Ext'd Status 1	Reserved 0	Preamble Suppression 1	Auto-Neg Complete 0	Remote Fault 0	Auto-Neg Ability 1	Link Status 0	Jabber Detect 0	Extended Capability 1
Register 2 (0x02) PHY Identifier Register #1 (PHYIDR1)	OUI_MSB[15] 0	OUI_MSB[14] 0	OUI_MSB[13] 1	OUI_MSB[12] 0	OUI_MSB[11] 0	OUI_MSB[10] 0	OUI_MSB[9] 0	OUI_MSB[8] 0	OUI_MSB[7] 0	OUI_MSB[6] 0	OUI_MSB[5] 0	OUI_MSB[4] 0	OUI_MSB[3] 0	OUI_MSB[2] 0	OUI_MSB[1] 0	OUI_MSB[0] 0
Register 3 (0x03) PHY Identifier Register #2 (PHYIDR2)	OUI_LSB[15] 0	OUI_LSB[14] 1	OUI_LSB[13] 0	OUI_LSB[12] 1	OUI_LSB[11] 1	OUI_LSB[10] 1	VMDR_MDL[5] 0	VMDR_MDL[4] 0	VMDR_MDL[3] 0	VMDR_MDL[2] 1	VMDR_MDL[1] 0	VMDR_MDL[0] 1	MDL_REV[3] 0	MDL_REV[2] 0	MDL_REV[1] 0	MDL_REV[0] 0
Register 4 (0x04) Auto-Neg Advertisement Register (ANAR)	Next Page 1	Reserved 0	Remote Fault 0	Reserved 0	ASY_PAUSE 0	PAUSE 0	T4 0	TX_FD 1	TX_HD 1	10_FD 0	10_HD 0	PSB[4] 0	PSB[3] 0	PSB[2] 0	PSB[1] 0	PSB[0] 1
Register 5 (0x05) Auto-Neg Link Partner Ability Register (ANLPAR)	Next Page 0	ACK 0	Remote Fault 0	Reserved 0	ASY_PAUSE 0	PAUSE 0	T4 0	100_TX_FD 0	100_TX 0	10_FD 0	10 0	PSB[4] 0	PSB[3] 0	PSB[2] 0	PSB[1] 0	PSB[0] 0
Register 6 (0x06) Auto-Neg Expansion Register (ANER)	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	PDF 0	LP_NP Able 0	NP_Able 1	Page _RX 0	LP_AN Able 0
Register 7 (0x07) Auto-Neg NP TX Register (ANNPTR)	Next Page 1	Reserved 0	Message Page 1	ACK2 0	TOG_TX 0	NP_M[10] 0	NP_M[9] 0	NP_M[8] 0	NP_M[7] 0	NP_M[6] 0	NP_M[5] 0	NP_M[4] 0	NP_M[3] 0	NP_M[2] 0	NP_M[1] 0	NP_M[0] 0
Register 8 (0x08) Auto-Neg NP RX Register (ANNPRR)	Next Page 0	Reserved 0	Message Page 0	ACK3 0	TOG_RX 0	NP_M[10] 0	NP_M[9] 0	NP_M[8] 0	NP_M[7] 0	NP_M[6] 0	NP_M[5] 0	NP_M[4] 0	NP_M[3] 0	NP_M[2] 0	NP_M[1] 0	NP_M[0] 0
Register 9 (0x09) 1000BASE-T Control Register (1KTCR)	Test Mode[1] 0	Test Mode[2] 0	Test Mode[3] 0	Master/Slave Config Enable Strap / 0	Master/Slave Config Value Strap / 0	Repeater DTE 0	1000BASE-T Full-Duplex 1	1000BASE-T Half-Duplex 1	ASM_DIR 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 10 (0x0A) 1000BASE-T Status Register (1KSTSR)	Master/Slave Manual Config Fault 0	Config. Re-solved to Master 0	Local Receiver Status 0	Remote Receiver Status 0	LP1000T FD 0	LP 1000T 0	ASM_DIR 0	Reserved 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0
Register 15 (0x0F) 1000BASE-T Extended Status Register (1KSCR)	1000BASE-T Full-Duplex 0	1000BASE-T Half-Duplex 0	1000BASE-T Full-Duplex 1	1000BASE-T Half-Duplex 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 16 (0x10) Strap Option Register (Strap_reg)	PHY_ADD [4] 0	PHY_ADD [3] 0	PHY_ADD [2] 0	PHY_ADD [1] 0	PHY_ADD [0] 1	Reserved 0	Reserved 0	AN_Ena 1	M/S value 0	M/S Manual 0	Reserved 0	Sel_Duplex 1	Reserved 0	Reserved 0	Sel_Speed [1] 0	Sel_Speed [0] 0
Register 167(0x11) PHY Support Register (PHY_SUP)	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Speed_Res [1] 0	Speed_Res [0] 0	Link_Res 0	Duplex_Res 0	Reserved 0

Key: Bit Name / Read/Writable / Default Value — Bit Name / Read Only / Value

Table 8. Basic Mode Control Register (BMCR) address 0x00

Bit	Bit Name	Default	Description
15	Reset	0, RW/SC	**Reset:** 1 = Initiate software Reset / Reset in Process. 0 = Normal operation. This bit sets the status and control registers of the PHY to their default states. This bit, which is self-clearing, returns a value of one until the reset process is complete (approximately 1.2 ms for reset duration). Reset is finished once the Auto-Negotiation process has begun or the device has entered it's forced mode.
14	Loopback	0, RW	**Loopback:** 1 = Loopback enabled. 0 = Normal operation. The loopback function enables MII/GMII transmit data to be routed to the MII/GMII receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 500 µs "dead time" before any valid data will appear at the MII receive outputs in 100 Mb/s operation.
13	Speed[0]	Strap Pin 208, RW	**Speed Select:** When Auto-Negotiation is disabled, bits 6 and 13 select device speed selection per table below: Speed[1] / Speed[0] / Speed Enabled 1 / 1 = Reserved 1 / 0 = 1000 Mb/s 0 / 1 = 100 Mb/s 0 / 0 = 10 Mb/s The default value of this bit is = to the strap value of pin 208 during reset/power-on IF the AN_EN is low.
12	AN_ENable	Strap [1], RW	**Auto-Negotiation Enable:** 1 = Auto-Negotiation Enabled - bits 6, 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled - bits 6, 8 and 13 determine the link speed and mode.
11	Power_Down	0, RW	**Power Down:** 1 = Power down (only Management Interface and logic active.) 0 = Normal operation.
10	Isolate	0, RW	**Isolate:** 1 = Isolates the Port from the MII with the exception of the serial management. When this bit is asserted, the DP83891 does not respond to TXD[3:0], TX_EN, and TX_ER inputs, and it presents a high impedance on TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CRS outputs. 0 = Normal operation.
9	Restart_AN	0, RW, SC	**Restart Auto-Negotiation:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation.

Table 8. Basic Mode Control Register (BMCR) address 0x00

Bit	Bit Name	Default	Description
8	Duplex	Strap [1], RW	**Duplex Mode:** 1 = Full Duplex operation. Duplex selection is allowed only when Auto-Negotiation is disabled (bit 12 = 0). 0 = Half Duplex operation.
7	Collision Test	0, RW	**Collision Test:** 1 = Collision test enabled. 0 = Normal operation. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TX_EN.
6	Speed[1]	Strap Pin 180, RW	**Speed Select:** See description for bit 13. The default value of this bit is = to the strap value of pin 180 during reset/power-on IF the AN_EN is low.
5:0	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.

Table 9. Basic Mode Status Register (BMSR) address 0x01

15	100BASE-T4	0, RO	**100BASE-T4 Capable:** 1 = Device able to perform 100BASE-T4 mode. 0 = Device not able to perform 100BASE-T4 mode. DP83891 does not support 100BASE-T4 mode and bit should always be read back as “0”.
14	100BASE-TX Full Duplex	1, RO	**100BASE-TX Full Duplex Capable:** 1 = Device able to perform 100BASE-TX in full duplex mode. 0 = Device unable to perform 100BASE-TX in full duplex mode.
13	100BASE-TX Half Duplex	1, RO	**100BASE-TX Half Duplex Capable:** 1 = Device able to perform 100BASE-TX in half duplex mode. 0 = Device unable to perform 100BASE-TX in half duplex mode.
12	10BASE-T Full Duplex	1, RO	**10BASE-T Full Duplex Capable:** 1 = Device able to perform 10BASE-T in full duplex mode. 0 = Device unable to perform 10BASE-T in full duplex mode.
11	10BASE-T Half Duplex	1, RO	**10BASE-T Half Duplex Capable:** 1 = Device able to perform 10BASE-T in half duplex mode. 0 = Device unable to perform 10BASE-T in half duplex mode. .
10	100BASE-T2 Full Duplex	0, RO	**100BASE-T2 Full Duplex Capable:** 1 = Device able to perform 100BASE-T2 **Full Duplex** mode. 0 = Device unable to perform 100BASE-T2 **Full Duplex** mode. DP83891 does not support 100BASE-T2 mode and bit should always be read back as “0”.
9	100BASE-T2 Half Duplex	0, RO	**100BASE-T2 Half Duplex Capable:** 1 = Device able to perform 100BASE-T2 **Half Duplex** mode. 0 = Device unable to perform 100BASE-T2 **Full Duplex** mode. DP83891 does not support 100BASE-T2 mode and bit should always be read back as “0”.

Table 9. Basic Mode Status Register (BMSR) address 0x01

8	1000BASE-T Extended Status	1, RO	**1000BASE-T Extended Status Register:** 1 = Device supports Extended Status Register 0x0F (15). 0 = Device does not supports Extended Status Register 0x0F (15).
7	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.
6	Preamble Suppression	1, RO	**Preamble suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround.
5	Auto-Negotiation Complete	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process complete, and contents of registers 5, 6, 7, & 8 are valid. 0 = Auto-Negotiation process not complete.
4	Remote Fault	0, RO	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	Auto-Negotiation Ability	1, RO	**Auto Configuration Ability:** 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	Link Status	0, RO	**Link Lost Since Last Read Status:** 1 = Link was good since last read of this register. (10/100/1000 Mb/s operation). 0 = Link was lost since last read of this register. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read via the management interface. This bit doesn't indicate the link status, but rather if the link was lost since last read. For actual link status, either this register should be read twice, or register 0x11 bit 2 should be read.
1	Jabber Detect	0, RO	**Jabber Detect:** Set to 1 if 10BASE-T Jabber detected locally. 1 = Jabber condition detected. 0 = No Jabber.
0	Extended Capability	1, RO	**Extended Capability:** 1 = Extended register capable.

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83891. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. National's IEEE assigned OUI is 080017h.

Table 10. PHY Identifier Resister #1 (PHYIDR1) address 0x02

Bit	Bit Name	Default	Description
15:0	OUI_MSB	<0010_0000_0000_0000>, RO	**OUI Most Significant Bits**: Bits 3 to 18 of the OUI (080017h) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

Table 11. PHY Identifier Resister #2 (PHYIDR2) address 0x03

Bit	Bit Name	Default	Description
15:10	OUI_LSB	<01_0111>, RO	**OUI Least Significant Bits:** Bits 19 to 24 of the OUI (080017h) are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	6'b <00_0101>, RO	**Vendor Model Number:** The six bits of vendor model number are mapped to bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	4'b <0000>, RO	**Model Revision Number:** Four bits of the vendor model revision number are mapped to bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation.

Table 12. Auto-Negotiation Advertisement Register (ANAR) address 0x04

Bit	Bit Name	Default	Description
15	NP	0, RO	**Next Page Indication:** 0 = Next Page Transfer not desired. 1 = Next Page Transfer desired.
14	Reserved	0, RO	**Reserved by IEEE:** Writes ignored, Read as 0.
13	RF	0, RO	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault. 0 = No Remote Fault detected.
12	Reserved	0, RO	**Reserved for Future IEEE use:** Write as 0, Read as 0.
11	ASY_PAUSE	0, RO (See "User Information Sheet" on how to set this bit.)	**Asymmetrical PAUSE:** 1 = MAC/Controller supports Asymmetrical Pause direction. 0 = MAC/Controller does not support Asymmetrical Pause direction.
10	PAUSE	0, RW	**PAUSE:** 1 = MAC/Controller supports Pause frames. 0 = MAC/Controller does not support Pause frames.
9	T4	0, RO	**100BASE-T4 Support:** 0 = No support for 100BASE-T4.
8	TX_FD	Strap Pin 185, 1, RW	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the local device. 0 = 100BASE-TX Full Duplex not supported. The default value of this bit is = to the strap value of pin 185 during reset/power-on IF the AN_EN is high.
7	TX_HD	Strap Pin 184, 1, RW	**100BASE-TX Support Half Duplex:** 1 = 100BASE-TX Half Duplex is supported by the local device. 0 = 100BASE-TX Half Duplex not supported. The default value of this bit is = to the strap value of pin 184 during reset/power-on IF the AN_EN is high.
6	10_FD	Strap Pin 180, 0, RW	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported. 0 = 10BASE-T Full Duplex is not supported. The default value of this bit is = to the strap value of pin 180 during reset/power-on IF the AN_EN is high.

Table 12. Auto-Negotiation Advertisement Register (ANAR) address 0x04

Bit	Bit Name	Default	Description
5	10_HD	0, RW	**10BASE-T Half Duplex Support:** 1 = 10BASE-T Half Duplex is supported. 0 = 10BASE-T Half Duplex is not supported.
4:0	PSB	<00001>, RO	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3.

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. .

Table 13. Auto-Negotiation Link Partner Ability Register (ANLPAR) address 0x05

Bit	Bit Name	Default	Description
15	NP	0, RO	**Next Page Indication:** 0 = Link Partner does not desire Next Page Transfer. 1 = Link Partner desires Next Page Transfer.
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word 0 = Not acknowledged. The Device's Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts. Software should not attempt to write to this bit.
13	RF	0, RO	**Remote Fault:** 1 = Remote Fault indicated by Link Partner. 0 = No Remote Fault indicated by Link Partner.
12	Reserved	0, RO	**Reserved for Future IEEE use:** Write as 0, read as 0.
11	ASY_PAUSE	0, RO	**Asymmetrical PAUSE:** 1 = Link Partner supports Asymmetrical Pause direction. 0 = Link Partner does not support Asymmetrical Pause direction.
10	PAUSE	0, RO	**PAUSE:** 1 = Link Partner supports Pause frames. 0 = Link Partner does not support Pause frames.
9	T4	0, RO	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the Link Partner. 0 = 100BASE-T4 not supported by the Link Partner.
8	TX_FD	0, RO	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the Link Partner. 0 = 100BASE-TX Full Duplex not supported by the Link Partner.
7	TX	0, RO	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the Link Partner. 0 = 100BASE-TX not supported by the Link Partner.
6	10_FD	0, RO	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the Link Partner. 0 = 10BASE-T Full Duplex not supported by the Link Partner.

Table 13. Auto-Negotiation Link Partner Ability Register (ANLPAR) address 0x05

Bit	Bit Name	Default	Description
5	10	0, RO	**10BASE-T Support:** 1 = 10BASE-T is supported by the Link Partner. 0 = 10BASE-T not supported by the Link Partner.
4:0	PSB	<00000>, RO	**Protocol Selection Bits:** Link Partners's binary encoded protocol selector.

This register contains additional Local Device and Link Partner status information.

Table 14. Auto-Negotiate Expansion Register (ANER) address 0x06

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	**Reserved by IEEE:** Writes ignored, Read as 0.
4	PDF	0, RO	**Parallel Detection Fault:** 1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.
3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** 1 = Link Partner does support Next Page. 0 = Link Partner supports Next Page negotiation.
2	NP_ABLE	1, RO	**Next Page Able:** 1 = Indicates local device is able to send additional "Next Pages".
1	PAGE_RX	0, RO	**Link Code Word Page Received:** 1 =Link Code Word has been received, cleared on read of this register. 0 = Link Code Word has not been received.
0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able:** 1 = Indicates that the Link Partner supports Auto-Negotiation. 0 = Indicates that the Link Partner does not support Auto-Negotiation.

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 15. Auto-Negotiation Next Page Transmit Register (ANNPTR) address 0x07

Bit	Bit Name	Default	Description
15	NP	1, RW	**Next Page Indication:** 0 = No other Next Page Transfer desired. 1 = Another Next Page desired.
14	Reserved	0, RO	**Reserved by IEEE**: Writes ignored, read as 0.
13	MP	1, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RO	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.

Table 15. Auto-Negotiation Next Page Transmit Register (ANNPTR) address 0x07

Bit	Bit Name	Default	Description
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was logic 0. 0 = Value of toggle bit in previously transmitted Link Code Word was logic 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<000_0000_1000>, RO	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 16. Auto-Negotiation Next Page Receive Register (ANNPRR) address 0x08

Bit	Bit Name	Default	Description
15	NP	0, RO	**Next Page Indication:** 0 = No other Next Page Transfer desired. 1 = Another Next Page desired.
14	Reserved	0, RO	**Reserved by IEEE**: Writes ignored, read as 0.
13	MP	0, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK3	0, RO	**Acknowledge3:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge3 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was logic 0. 0 = Value of toggle bit in previously transmitted Link Code Word was logic 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<0000 0000 000>, RO	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Reserved for future use as defined in Annex 28C of IEEE 802.3u.

Table 17. 1000BASE-T Control Register (1KTCR) address 0x09

Bit	Bit Name	Default	Description
15:13	Test Mode	0, RW	**Test Mode Select:** **bit 15 bit 14 bit 13 Test Mode Selected** 1 0 0 = Test Mode 4 0 1 1 = Test mode 3 0 1 0 = Test Mode 2 0 0 1 = Test Mode 1 0 0 0 = Normal Operation See IEEE 802.3ab section 40.6.1.1.2 “Test modes” for more information.
12	Master/Slave Manual Config Enable	Strap Pin 190, 0,RW	**Enable Manual Master/Slave Configuration:** 1 = Enable Manual Master/Slave Configuration control. 0 = Disable Manual Master/Slave Configuration control. The default value of this bit is = to the strap value of pin 190 during reset/power-on.
11	Master/Slave Config Value	Strap Pin 191, 0,RW	**Advertise Master/Slave Configuration Value:** 1 = Advertise PHY as MASTER when register 09h bit 12 = 1. 0 = Advertise PHY as SLAVE when register 09h bit 12 = 1. The default value of this bit is = to the strap value of pin 191 during reset/power-on.
10	Repeater/DTE	Strap Pin 208, 0, RO	**Advertise Device Type: Multi or single port** 1 = Repeater or Switch (DP83891 does not support Repeater mode). 0 = DTE. The default value of this bit is = to the strap value of pin 208 during reset/power-on IF the AN_EN pin is high.
9	1000BASE-T Full Duplex	Strap Pin 195, 1, RW	**Advertise 1000BASE-T Full Duplex Capable:** 1 = Advertise DTE as 1000BASE-T Full Duplex Capable. 0 = Advertise DTE as not 1000BASE-T Full Duplex Capable. The default value of this bit is = to the strap value of pin 195 during reset/power-on IF the AN_EN pin is high.
8	1000BASE-T Half Duplex	Strap Pin 189, 1, RW	**Advertise 1000BASE-T Half Duplex Capable:** 1 = Advertise DTE as 1000BASE-T Half Duplex Capable. 0 = Advertise DTE as not 1000BASE-T Half Duplex Capable. The default value of this bit is = to the strap value of pin 189 during reset/power-on IF the AN_EN pin is high.
7:0	Reserved	0, RW	**Reserved by IEEE:** Writes ignored, Read as 0.

This register provides status for 1000BASE-T link.

Table 18. 1000BASE-T Status Register (1KSTSR) address 0x0A (10’d)

Bit	Bit Name	Default	Description
15	Master-Slave Manual Config Fault	0, RO	**MASTER/SLAVE manual configuration fault detected:** 1 = MASTER/SLAVE manual configuration fault detected. 0 = No MASTER/SLAVE manual configuration fault detected.
14	MS_Config_Results	0, RO	**MASTER SLAVE Configuration Results:** 1 = Configuration resolved to MASTER. 0 = Configuration resolved to SLAVE.

Table 18. 1000BASE-T Status Register (1KSTSR) address 0x0A (10'd)

Bit	Bit Name	Default	Description
13	Local Receiver Status	0, RO	**Local Receiver Status:** 1 = OK. 0 = Not OK.
12	Remote Receiver Status	0, RO	**Remote Receiver Status:** 1 = OK. 0 = Not OK.
11	LP_1000T_FD	0, RO	**Link Partner 1000T Full Duplex:** 1 = Link Partner capable of 1000BASE-T Full Duplex. 0 = Link Partner not capable of 1000BASE-T Full Duplex.
10	LP_1000T_HD	0, RO	**Link Partner 1000T Half Duplex:** 1 = Link Partner capable of 1000BASE-T Half Duplex. 0 = Link Partner not capable of 1000BASE-T Half Duplex.
9	LP_ASM_DIR	0, RO	**Link Partner ASM_DIR Capable:** 1 = Link Partner **Asymmetric Pause Direction** capable. 0 = Link Partner not **Asymmetric Pause Direction** capable.
8	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.
7:0	IDLE Error Count (MSB)	0, RO	**IDLE Error Count**

Note: Registers 0x0B - 0x0E are Reserved by IEEE.

Table 19. 1000BASE-T Extended Status Register (1KSCR) address 0x0F (15'd)

Bit	Bit Name	Default	Description
15	1000BASE-X_FD	0, RO	**1000BASE-X Full Duplex Support:** 1 = 1000BASE-X is supported by the local device. 0 = 1000BASE-X is not supported. DP83891 does not support 1000BASE-X and bit should always be read back as "0".
14	1000BASE-X _DH	0, RO	**1000BASE-X Half Duplex Support:** 1 = 1000BASE-X is supported by the local device. 0 =1000BASE-X is not supported. DP83891 does not support 1000BASE-X and bit should always be read back as "0".
13	1000BASE-T_FD	1, RO	**1000BASE-T Full Duplex Support:** 1 = 1000BASE-T is supported by the local device. 0 =1000BASE-T is not supported.
12	1000BASE-T_HD	1, RO	**1000BASE-T Half Duplex Support:** 1 = 1000BASE-T is supported by the local device. 0 =1000BASE-T is not supported.
11:0	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.

The register below summarizes all the strap options.

Table 20. Strap Option Register (Strap_reg) address 0x10 (16'd)

Bit	Bit Name	Default	Description
15:11	PHY_Address 4:0	00001, RO	**PHY Address:** Strap option pins 200,201,204,205, and 207. Changeable only through restrapping and resetting the device.
10:9	Reserved		**Reserved:**

Table 20. Strap Option Register (Strap_reg) address 0x10 (16'd)

Bit	Bit Name	Default	Description
8	AN enable	1, RO	**Auto-negotiation Enable:** Strap option pin 192. This value could be overwritten by changing bit 12 of register 0x00. However this bit will retain the original strapped value, regardless of changes to bit 12 of register 0x00.
7	Master/Slave value	0, RO	**Master/Slave Value:** Strap option pin 191. This value could be overwritten by changing bit 11 of register 0x09.
6	Manual M/S config	0, RO	**Manual Master/Slave Configuration Enable:** Strap option pin 191. This value could be overwritten by changing bit 12 of register 0x09.
5	Reserved		**Reserved:**
4	Sel_ Duplex	1, RO	**Duplex Select:** Strap option pin 185. This value could be overwritten by changing bit 8 of register 0x00.
3:2	Reserved		**Reserved:**
1:0	Sel_Speed 1:0	00, RO	**Speed Select:** Strap option pins 180 and 208 respectively. This value could be overwritten by changing bits 6 and 13 of register 0x00.

Table 21. PHY Support Register (PHY_Sup) address 0x11 (17'd)

Bit	Bit Name	Default	Description
15:5	Reserved		**Reserved:**
4:3	Speed_Status 1:0	Strap or AN determined value, RW	**Speed Resolved:** These two bits indicate the speed of operation as determined by Auto-negotiation or as set by manual configuration. Speed[1] Speed[0] Speed of operation 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s
2	Link-up_Status	0, RW	**Link status:** '1' indicates that a good link is established, '0' indicates no link.
1	Duplex_Status	0, RW	**Duplex status:** '1' indicates that the current mode of operation is full duplex. '0' indicates that the current mode of operation is half duplex.
0	Reserved		**Reserved:**

Table 22. MDIX_sel address 0x15 (21'd)

Bit	Bit Name	Default	Description
15:1	Reserved		**Reserved:**
0	MDIX_sel	0	**MDIX_sel:** If Auto-MDIX selection is disabled, then this bit can be used to set for either cross-over or straight cable operation: 1 = Cross-over channels A and B. (i.e. the cable is straight) 0 = Don't cross-over channels A and B. (i.e. the cable is cross-over)

Table 23. Expand_mem address 0x16 (22'd)

Bit	Bit Name	Default	Description
15:0	Expanded Memory Modes		**Expanded Memory Modes:** Allows access to expanded memory and sets the mode of access. Also see registers 0x1D and 0x1E and the FAQ section.

Table 24. Exp_mem_data address 0x1D (29'd)

Bit	Bit Name	Default	Description
15:0	Expanded Memory Data	RW	**Expanded Memory Data:** Data to be written to or read from expanded memory.

Table 25. Exp_mem_add address 0x1E (30'd)

Bit	Bit Name	Default	Description
15:0	Expanded Memory Address	RW	**Expanded Memory Address:** Pointer to the address in expanded memory

5.0 Electrical Specifications

Absolute Maximum Ratings

Supply Voltage (V_{DD})	-0.5 V to 4.2 V
Input Voltage (DC_{IN})	-0.5 V to V_{DD} + 0.5 V
Output Voltage (DC_{OUT})	-0.5 V to V_{DD} + 0.5 V
Storage Temperature	-65˚C to 150˚C
ESD Protection	1000 V

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.*

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply voltage (V_{DD})	3.15	3.3	3.45	V
Ambient Temperature (T_A)			TBD (Note 1)	˚C
REF_CLK Input Freq. Stability (over temperature)	-50		+50	ppm
REF_CLK Input Duty Cycle	35		65	%
Center Frequency (f_c)		125		MHz

Note 1: See application note: “DP83891 Temperature Guide”

Thermal Characteristics

	Max	Units
Maximum Case Temperature	TBD	˚C
Theta Junction to Case (T_{jc})	1.16	˚C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - No Airflow @ 8.0 W	8.7	˚C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - 225 LFPM Airflow @ 8.0 W	6.6	˚C / W

5.1 DC Electrical Specification

Symbol	Pin Types	Parameter	Conditions	Min	Typ	Max	Units
V_{IH} GMII inputs	I I/O I/O_Z	Input High Voltage	V_{DD} = 3.3 V	2.0 (Note 1)			V
V_{IL} GMII inputs	I I/O I/O_Z	Input Low Voltage	V_{DD} = 3.3 V			0.8	V
V_{IH} non-GMII inputs	I I/O I/O_Z	Input High Voltage	V_{DD} = 3.3 V	2.0			V
V_{IL} non-GMII inputs	I I/O I/O_Z	Input Low Voltage	V_{DD} = 3.3 V			0.8	V
I_{IH}	I I/O I/O_Z	Input High Current	$V_{IN} = V_{DD}$ $V_{DD} = V_{DD(max)}$			10	µA
I_{IL}	I I/O I/O_Z	Input Low Current	V_{IN} = 0 V $V_{DD} = V_{DD(max)}$			10	µA
R strap	Strap	PU/PD internal resistor value.			35-65		kΩ
R strap	JTAG	PU/PD internal resistor value.			20-40		kΩ

Symbol	Pin Types	Parameter	Conditions	Min	Typ	Max	Units
V_{OL} GMII outputs	O, I/O I/O_Z	Output Low Voltage	I_{OL} = 1.0 mA $V_{DD} = V_{DD(min)}$	Gnd		0.5	V
V_{OH} GMII outputs	O, I/O I/O_Z	Output High Voltage	I_{OH} = -1 mA $V_{DD} = V_{DD(min)}$	2.1		3.6	V
V_{OL} non-GMII outputs	O, I/O I/O_Z	Output Low Voltage	I_{OL} = 4 mA $V_{DD} = V_{DD(min)}$	Gnd		0.4	V
V_{OH} non-GMII outputs	O, I/O I/O_Z	Output High Voltage	I_{OH} = -4 mA $V_{DD} = V_{DD(min)}$	2.4			V
V_{OL}	LED	Output Low Voltage	I_{OL} = 2.5 mA			0.4	V
V_{OH}	LED	Output High Voltage	I_{OH} = -2.5 mA	2.4			V
I_{OZ1}	I/O _Z	TRI-STATE Leakage	$V_{OUT} = V_{DD}$			10	µA
I_{OZ2}	I/O_Z	TRI-STATE Leakage	V_{OUT} = GND			-10	µA
R_{INdiff}	RXD_B±	Differential Input Resistance	see Test Conditions section		2.4		kΩ
V_{TXD_100}	TXD_A±	100 M Transmit V_{DIFF}	see Test Conditions section		1		V peak differential
V_{TXDsym}	TXD_A±	100 M Transmit Voltage Symmetry	see Test Conditions section		±2		%
V_{TXD_1000-2}	TXD#±	1000 M Transmit V_{DIFF} (Note 2)	see Test Conditions section		0.75		V peak differential
V_{TXD_1000-1}	TXD#±	1000 M Transmit V_{DIFF} (Note 3)	see Test Conditions section		0.375		V peak differential
C_{IN1}	I	CMOS Input Capacitance			8		pF
C_{OUT1}	O, I/O I/O_Z	CMOS Output Capacitance			8		pF
I_{dd1000}	Supply	1000BASE-T (Full Duplex)	see Test Conditions section		2.8		A
I_{dd100}	Supply	100BASE-TX (Full Duplex)			800 (Note 4)		mA

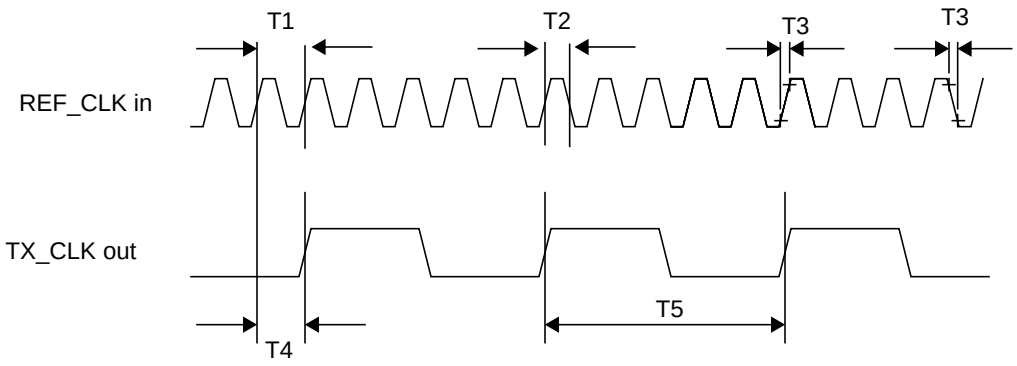
Note 1: See User Information Section for IEEE 802.3z GMII specifications.

Note 2: IEEE test mode 1, points A and B as described in Clause 40, section 40.6.1.2.1

Note 3: IEEE test mode 1, points C and D as described in Clause 40, section 40.6.1.2.1

Note 4: 100 Mb/s IDD is not tested. 800 mA is the typical value, given for informative purposes.

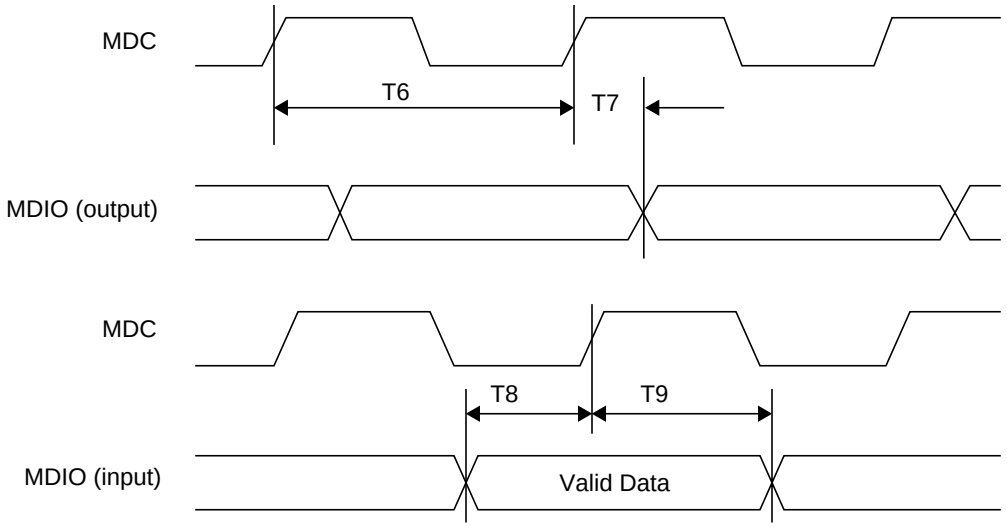
5.2 PGM Clock Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T1	REF_CLK frequency		-50		+50	125 MHz+/- ppm
T2	REF_CLK Duty Cycle		40		60	%
T3	REF_CLK t_R/t_F	10% to 90%		200-500		ps
T4	REF_CLK to TX_CLK Delay		-3 (Note 1)		+3	ns
T5	TX_CLK Duty Cycle		40		60	%

Note 1: Guaranteed by design. Not tested.

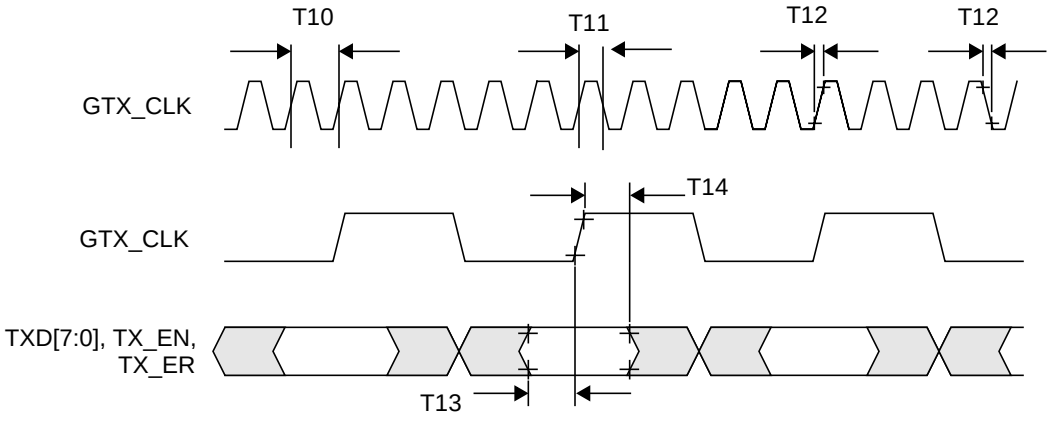
5.3 Serial Management Interface Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T6	MDC Frequency				2.5	MHz
T7	MDC to MDIO (Output) Delay Time		0		300	ns
T8	MDIO (Input) to MDC Setup Time		10			ns
T9	MDIO (Input) to MDC Hold Time		10			ns

5.4 1000 Mb/s Timing

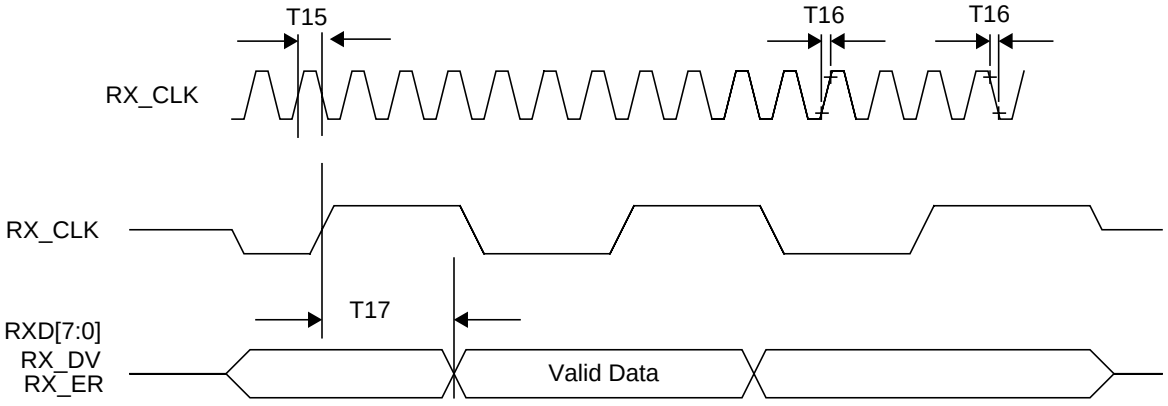
5.4.1 GMII Transmit Interface Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T10	GTX_CLK Stability (Note 5)		-100		+100	ppm
T11	GTX_CLK Duty Cycle		40		60	%
T12	GTX_CLK t_R/t_F (Note 5)	Note 1,4			1	ns
T13	Setup from valid TXD, TX_EN and TXER to ↑ GTX_CLK	Note 2,4	2.0			ns
T14	Hold from ↑ GTX_CLK to invalid TXD, TX_EN and TXER	Note 3,4	0.0			ns

Note 1: t_r and t_f are measured from $V_{IL\_AC(MAX)}$ = 0.7V to $V_{IH\_AC(MIN)}$ = 1.9V.
Note 2: t_{setup} is measured from data level of 1.9 V to clock level of 0.7 V for data = '1'; and data level = 0.7 V to.clock level 0.7 V for data = '0'
Note 3: t_{hold} is measured from clock level of 1.9 V to data level of 1.9 V for data = '1'; and clock level = 1.9 V to.data level 0.7 V for data = '0
Note 4: GMII Receiver input template measured with "GMII point-to-point test circuit", see Test Conditions Section
Note 5: Guaranteed by design. Not tested.

5.4.2 GMII Receive Timing

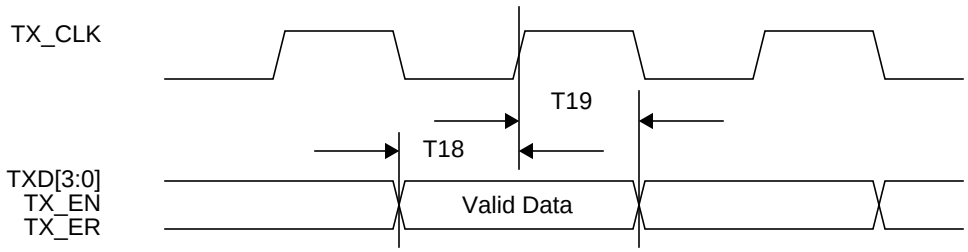


Parameter	Description	Notes	Min	Typ	Max	Units
T15	RX_CLK Duty Cycle		40		60	%
T16	RX_CLK t_R/t_F (Note 5)	Note 1, 4			1	ns
T17	↑ RX_CLK to RXD, RX_DV and RX_ER delay	Note 2, 3, 4	0.5		5.5	ns

Note 1: t_r and t_f are measured from $V_{IL\_AC(MAX)}$ = 0.7V to $V_{IH\_AC(MIN)}$ = 1.9V.
Note 2: $t_{delay\ max}$ is measured from clock level of 0.7 V to data level of 1.9 V for data = '1'; and clock level = 0.7 V to.data level 0.7 V for data = '0
Note 3: $t_{delay\ min}$ is measured from clock level of 1.9 V to data level of 1.9 V for data = '1'; and clock level = 1.9 V to.data level 0.7 V for data = '0
Note 4: GMII Receiver input template measured with "GMII point-to-point test circuit", see Test Conditions Section
Note 5: Guaranteed by design. Not tested.

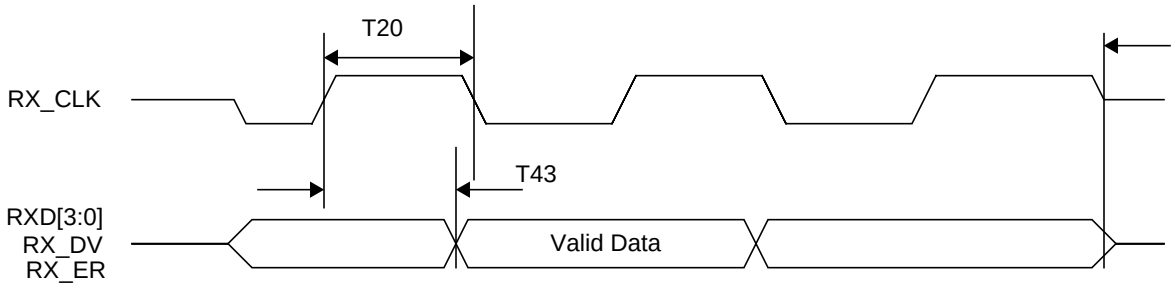
5.5 100 Mb/s Timing

5.5.1 100 Mb/s MII Transmit Timing



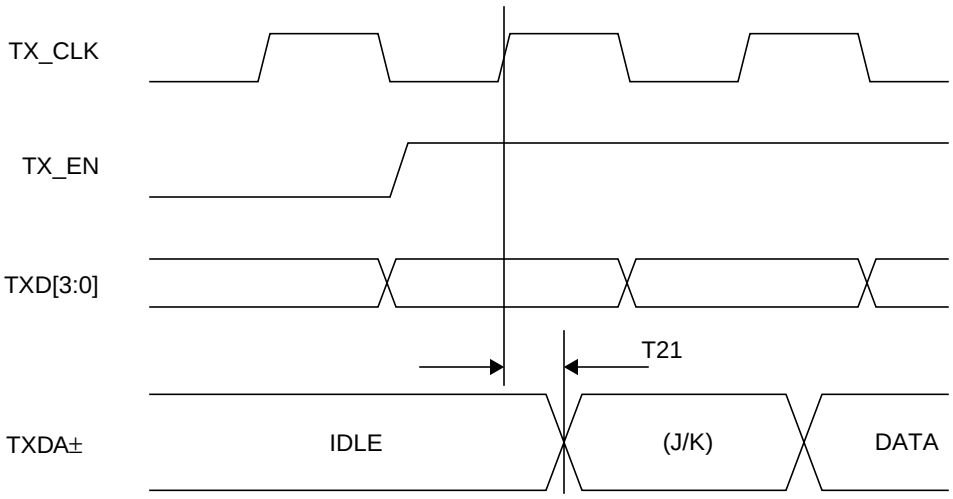
Parameter	Description	Notes	Min	Typ	Max	Units
T18	TXD[3:0], TX_EN, TX_ER Setup to ↑ TX_CLK		10			ns
	TXD[4:0] Setup to ↑ TX_CLK		10			ns
T19	TXD[3:0], TX_EN, TX_ER Hold from ↑ TX_CLK		-1			ns
	TXD[4:0] Hold from ↑ TX_CLK	100 Mb/s Symbol Mode	-1			ns

5.5.2 100 Mb/s MII Receive Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T43	↑ RX_CLK to RXD[3:0], RX_DV, RX_ER Delay		10		30	ns
T20	RX_CLK Duty Cycle		35		65	%

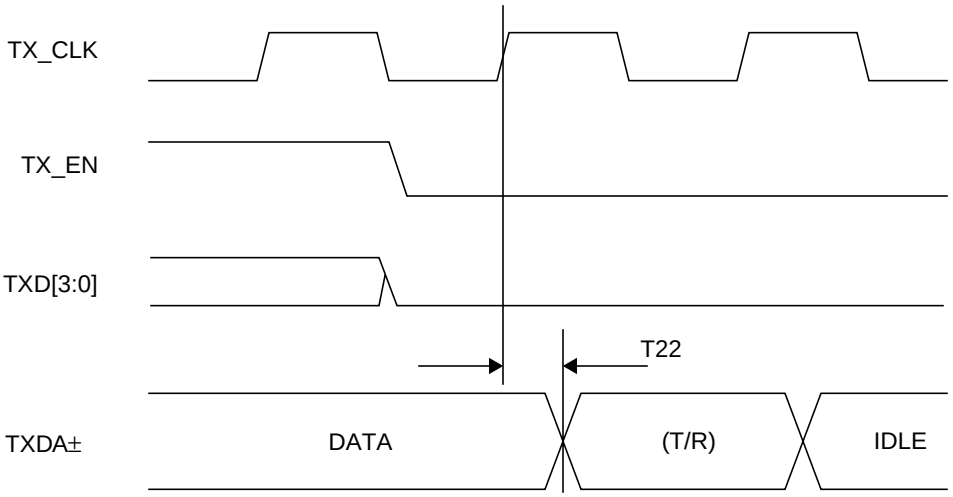
5.5.3 100BASE-TX Transmit Packet Latency Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T21	↑ TX_CLK to TXDA± latency				6.0	bits
		100 Mb/s Symbol Mode			6.0	bits

Note 1: For normal 100 mb/s mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the “J” code group as output from the TXDA± pins. 1 bit time = 10 ns in 100 Mb/s mode. For Symbol mode, because TX_EN has no meaning, latency is measured from the first rising edge of TX_CLK occurring after the assertion of a data nibble on the Transmit MII to the first bit (MSB) of that nibble as output from the TXDA± pins.

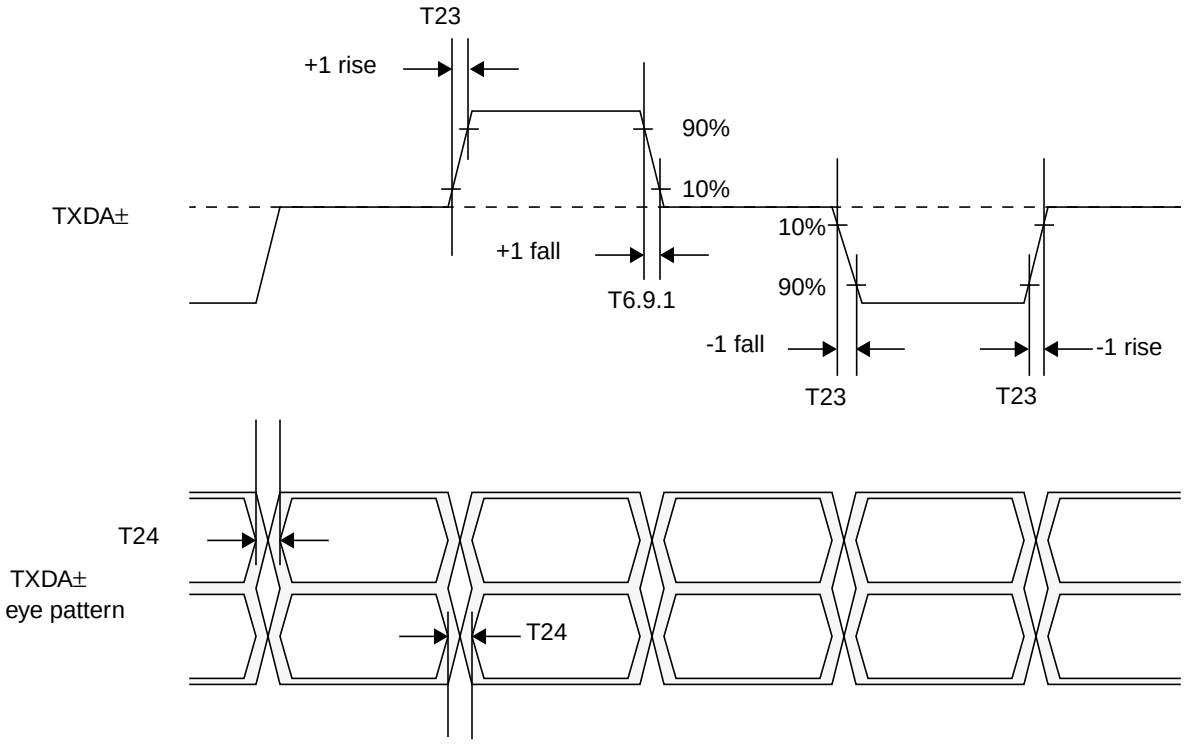
5.5.4 100BASE-TX Transmit Packet Deassertion Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T22	TX_CLK to TXDA± Idling				6.0	bits
		100 Mb/s Symbol mode			6.0	bits

Note 1: Deassertion is determined by measuring the time from the first rising edge of TX_CLK occurring after the deassertion of TX_EN to the first bit of the “T” code group as output from the TXDA± pins. For Symbol mode, because TX_EN has no meaning, Deassertion is measured from the first rising edge of TX_CLK occurring after the deassertion of a data nibble on the Transmit MII to the last bit (LSB) of that nibble when it deasserts on the wire. 1 bit time = 10 ns in 100 Mb/s mode.

5.5.5 100BASE-TX Transmit Timing ($t_{R/F}$ & Jitter)

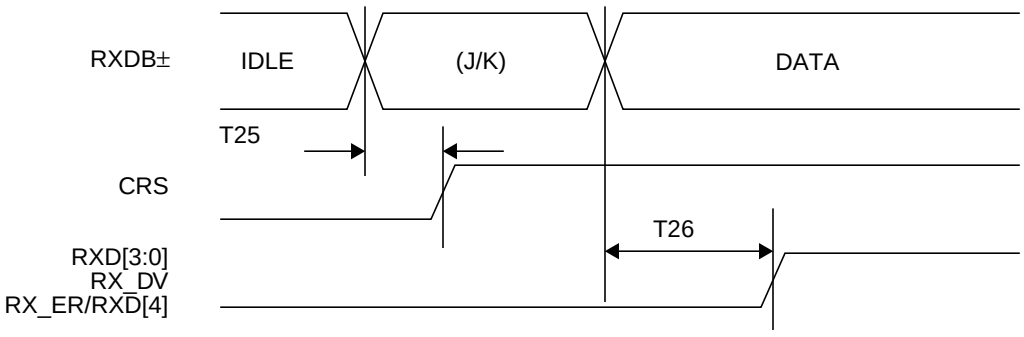


Parameter	Description	Notes	Min	Typ	Max	Units
T23	100 Mb/s TXDA± t_R and t_F	see Test Conditions section	3	4	5	ns
	100 Mb/s t_R and t_F Mismatch			500		ps
T24	100 Mb/s TXDA± Transmit Jitter				1.4	ns

Note: Normal mismatch is the difference between the maximum and minimum of all rise and fall times.

Note: Rise and fall times taken at 10% and 90% of the +1 or -1 amplitude.

5.5.6 100BASE-TX Receive Packet Latency Timing



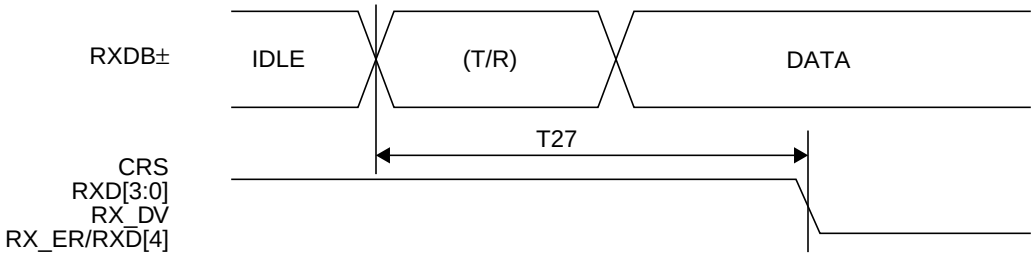
Parameter	Description	Notes	Min	Typ	Max	Units
T25	Carrier Sense ON Delay				17.5	bits
T26	Receive Data Latency				21	bits
		100 Mb/s Symbol mode			12	bits

Note: Carrier Sense On Delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.

Note: 1 bit time = 10 ns in 100 Mb/s mode.

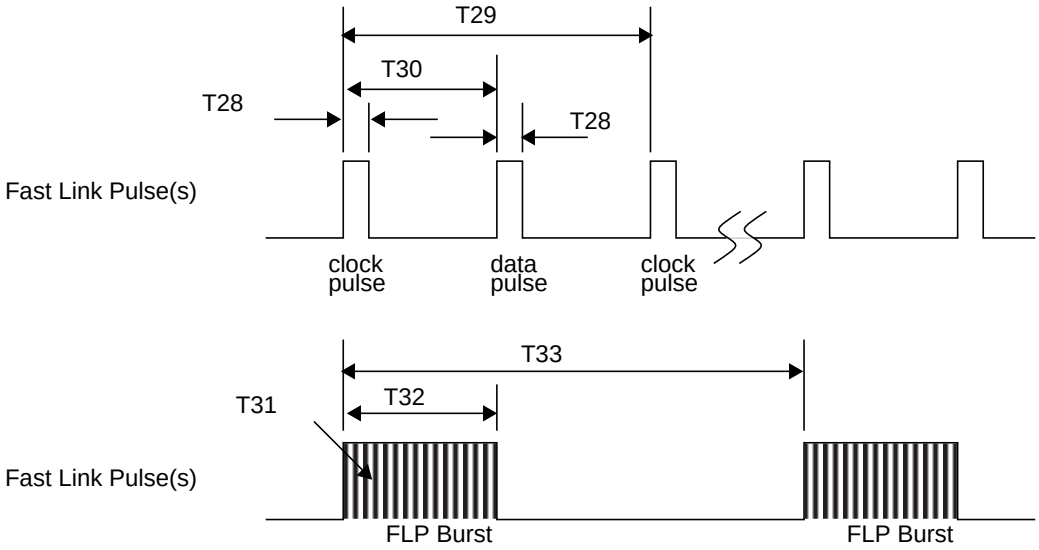
Note: RXDB± voltage amplitude is greater than the Signal Detect Turn-On Threshold Value.

5.5.7 100BASE-TX Receive Packet Deassertion Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T27	Carrier Sense OFF Delay				21.5	bits

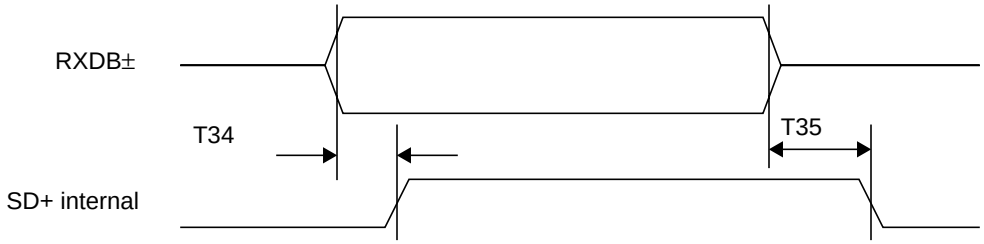
5.6 Auto-Negotiation Fast Link Pulse (FLP) Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T28	Clock/Data Pulse Width			100		ns
T29	Clock Pulse to Clock Pulse Period		111	125	139	µs
T30	Clock Pulse to Data Pulse Period	Data = 1	55.5	62.5	69.5	µs
T31	Number of Pulses in a Burst		17		33	#
T32	Burst Width			2		ms
T33	FLP Burst to FLP Burst Period		8		24	ms

Note 1: These specifications represent both transmit and receive timings.

5.6.1 100BASE-TX Signal Detect Timing

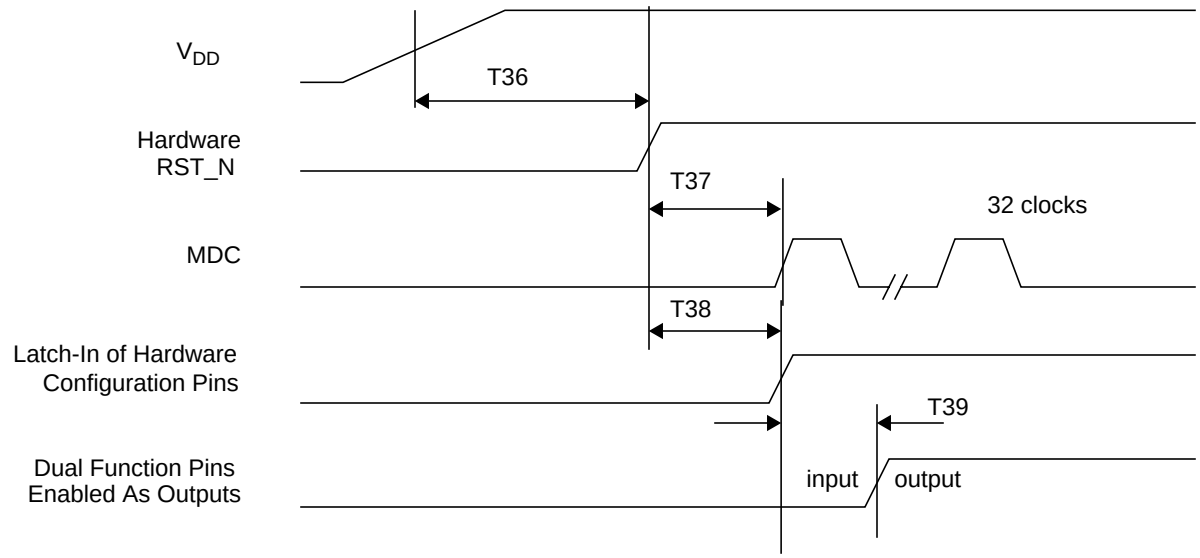


Parameter	Description	Notes	Min	Typ	Max	Units
T34	SD Internal Turn-on Time				1	ms
T35	SD Internal Turn-off Time				300	µs

Note 1: The SD internal signal is available as an external signal in Symbol mode.

Note 2: The signal amplitude at RXDB± is TP-PMD compliant.

5.7 Reset Timing



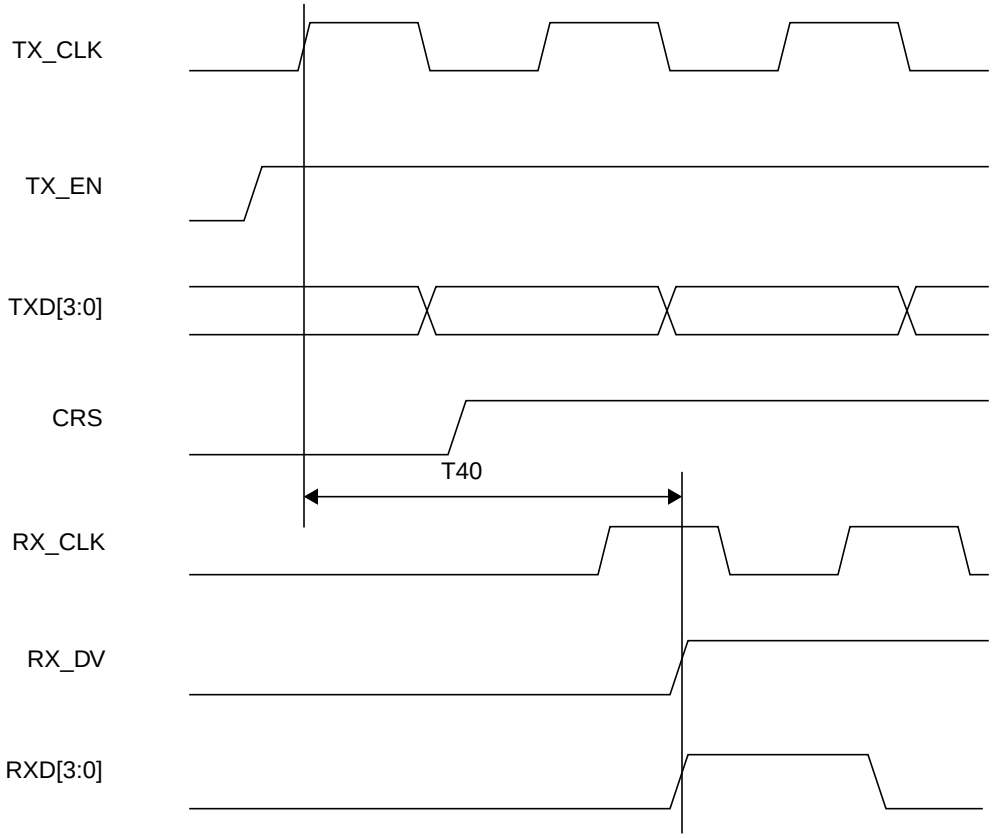
Parameter	Description	Notes	Min	Typ	Max	Units
T36	Hardware RESET Pulse Width		140			µs
T37	Post RESET Stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization		3		µs
T38	Hardware Configuration Latch-in Time from the Deassertion of RESET (either soft or hard)	Hardware Configuration Pins are described in the Pin Description section		3		µs
T39	Hardware Configuration pins transition to output drivers	It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver		50		ns

Note 1: Software Reset should be initiated no sooner then 500 µs after power-up or the deassertion of hardware reset.

Note 2: It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver.

Note 3: The timing for Hardware Reset Option 2 is equal to parameter T1 plus parameter T2 (501 µs total).

5.8 Loopback Timing



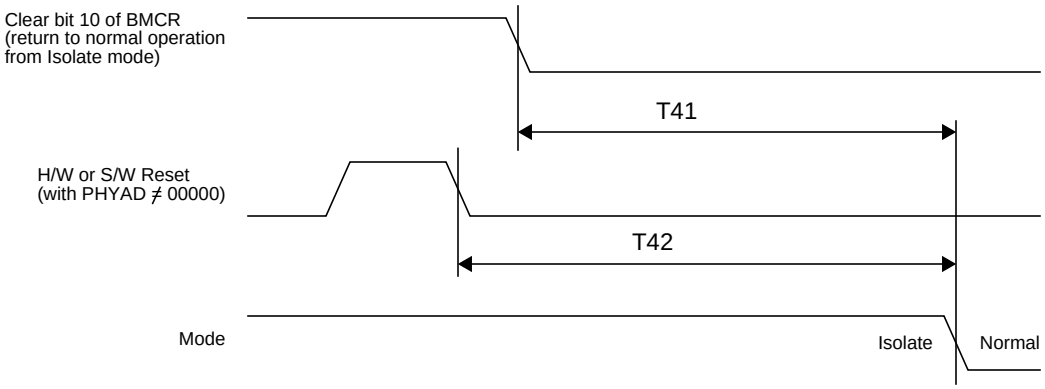
Parameter	Description	Notes	Min	Typ	Max	Units
T40	TX_EN to RX_DV Loopback	100 Mb/s			240	ns

Note 1: Due to the nature of the descrambler function, all 100BASE-X Loopback modes will cause an initial “dead-time” of up to 550 µs during which time no data will be present at the receive MII outputs. The 100BASE-X timing specified is based on device delays after the initial 550 µs “dead-time”.

Note 2: During loopback (all modes) both the TD± outputs remain inactive by default.

Note 3: The TD± outputs of the DP83891 can be enabled or disabled during loopback operation via the LBK_XMT_EN bit (bit 0 of the LBR register).

5.9 Isolation Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T41	From software clear of bit 10 in the BMCR register to the transition from Isolate to Normal Mode				100	µs
T42	From Deassertion of S/W or H/W Reset to transition from Isolate to Normal mode				500	µs

6.0 Test Conditions

This section contains information relating to the specific test environments, (including stimulus and loading parameters), used for the DP83891. These test conditions are categorized by pin/interface type in the following subsections:

— CMOS Outputs i.e., GMII/MII and LEDs

— TXD± Outputs sourcing 100BASE-TX

— TXD± Outputs sourcing 1000BASE-T

Additionally, testing conditions for Idd measurements are included.

6.1 CMOS Outputs (GMII/MII and LED)

Each of the GMII/MII and LED outputs are loaded with a controlled current source to either ground or V_{DD} for testing V_{OH}, V_{OL}, and AC parametrics. The associated capacitance of this load is 50 pF. The diagram in Figure 16 illustrates the test configuration.

It should be noted that the current source and sink limits are set to 4.0 mA when testing/loading the GMII/MII output pins. The current source and sink limits are set to 2.5 mA when testing/loading the LED output pins.

6.2 TXD± Outputs (sourcing 100BASE-TX)

When configured for 100BASE-TX operation, these differential outputs source scrambled 125 Mb/s data at MLT-3 logic levels. These outputs are loaded as illustrated in Figure 17. Note that the transmit amplitude and rise/fall time measurements are made across the secondary of the transmit transformer as specified by the IEEE 802.3u Standard.

6.3 TXD± Outputs (sourcing 1000BASE-T)

When configured for 1000BASE-T operation, the differential outputs (4-pairs) source Pattern-1 (see below) at 125 Mb/s using PAM-17 levels. The outputs are loaded as illustrated in Figure 18. Note that the transmit amplitude and rise/fall time measurements are made across the secondary of the transmit transformer as specified by the IEEE 802.3ab/D5.1 Specification.

Pattern 1:

{{+2 followed by 127 0 symbols}, {-2 followed by 127 0 symbols}, {+1 followed by 127 0 symbols}, {-1 followed by 127 0 symbols}, (128 +2 symbols, 128 -2 symbols}, {1024 0 symbols}}

6.4 Idd Measurement Conditions

The DP83891 Gig PHYTER is currently tested for total device Idd under three operational modes:

— 100BASE-TX Full Duplex (max packet length / min IPG)

— 1000BASE-T Full Duplex (max packet length / min IPG)

The device loading described in each of the preceding sections is present during Idd test execution.

6.5 GMII Point-to-Point Test Conditions

In order to meet the requirements to support point-to-point links RX_CLK must comply with the potential template shown in Figure 20 using the test circuit in Figure 21.

6.6 GMII Setup and Hold Test Conditions

In order to meet the requirements to support point-to-point links GMII drivers (RXD[7:0], RX_DV, RX_ER) must comply with the potential template shown in Figure 20 using the test circuit in Figure 21 and meet the setup and hold times specified in Figure 5.4.2 GMII Receive Timing.

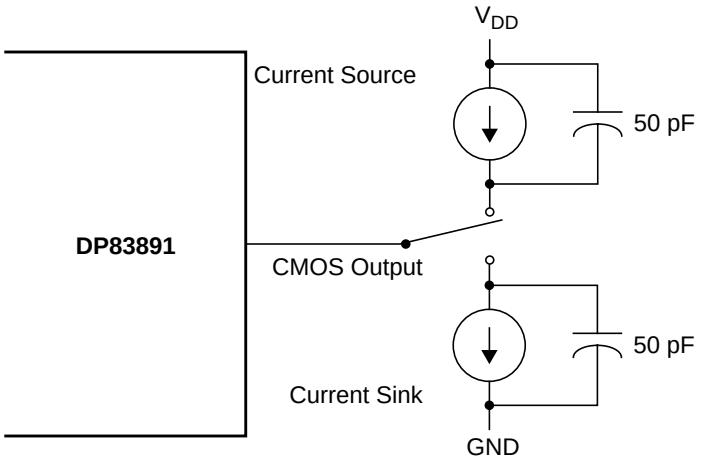


Figure 17. CMOS Output Test Load

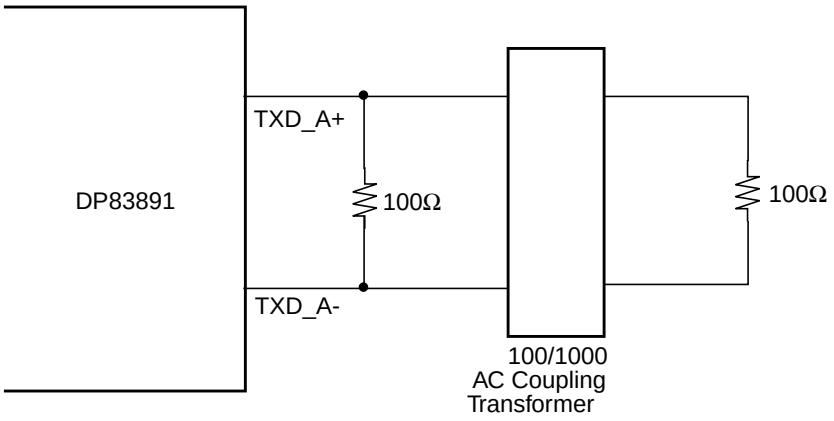


Figure 18. 100 Mb/s Twisted Pair Load (zero meters)

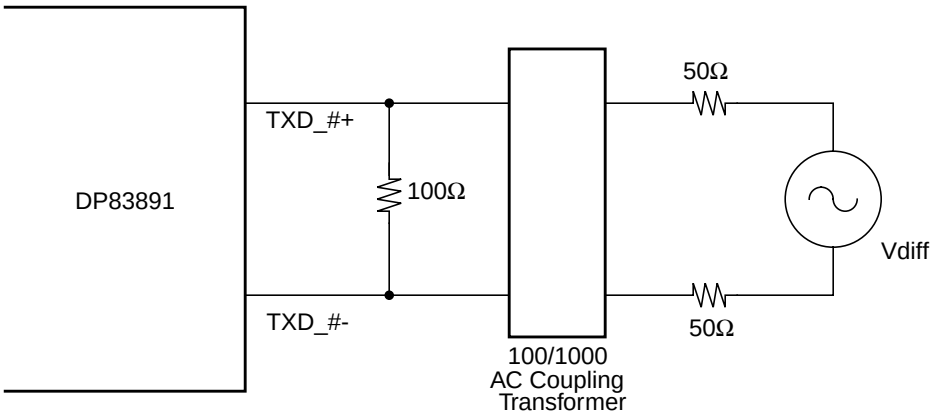


Figure 19. 1000 Mb/s Twisted Pair Load (zero meters)

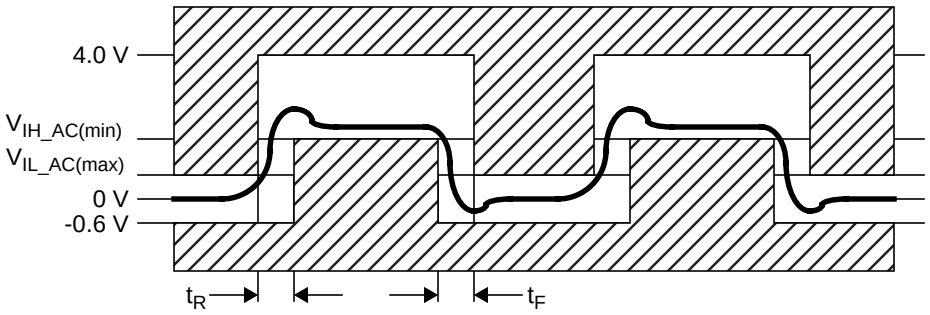


Figure 20. GMII Receiver Input Potential Template

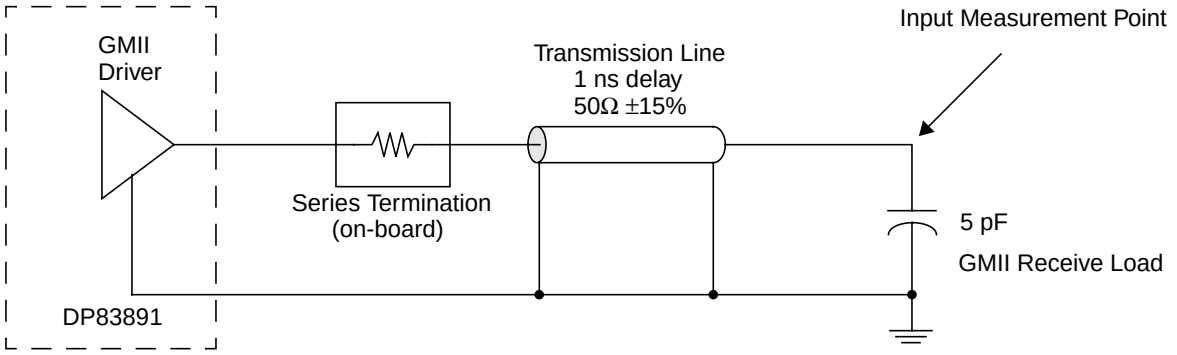


Figure 21. GMII Point-to-Point Test Circuit

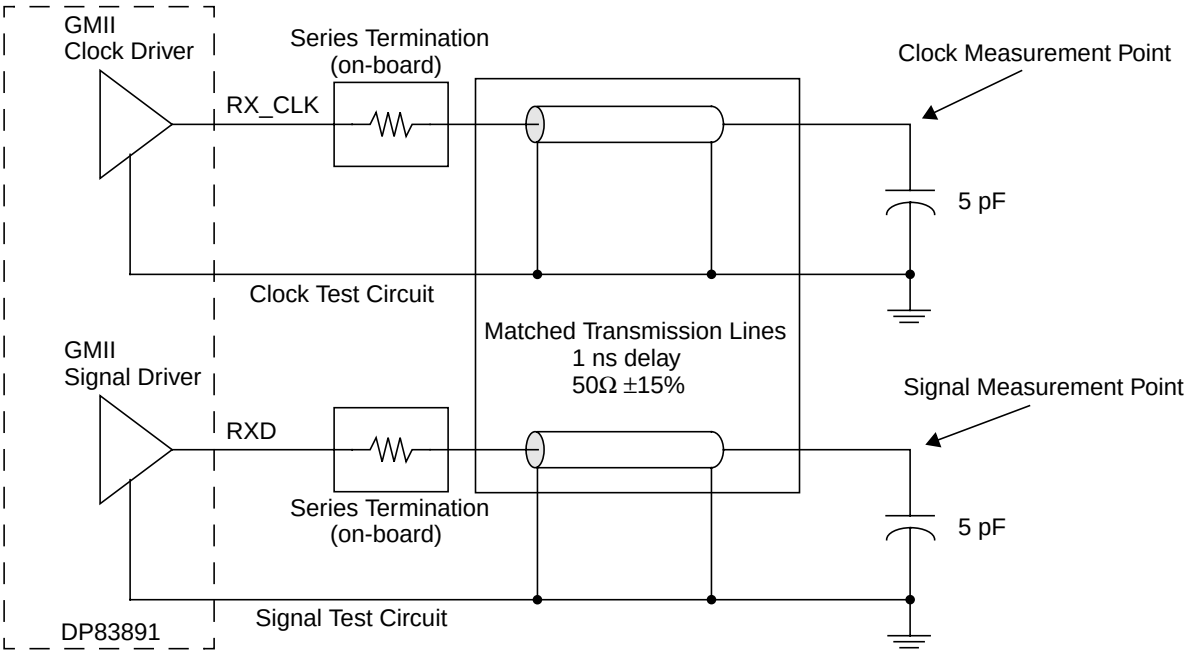


Figure 22. GMII Setup and Hold Time Test Circuit

7.0 User information

7.1 GMII VIH/VIL Levels

Issue:

GMII inputs require standard TTL VIH/VIL levels.

Description:

The IEEE 802.3z specification, Clause 35, lists VIH/VIL levels for the GMII interface as being 1.7/0.9 V respectively. The DP83891 has standard TTL level I/O buffers, which require VIH min. = 2.0 V and VIL max. = 0.8 V.

Compatibility:

VIH/VIL levels of 2.0/0.8 V are compatible with the IEEE 802.3z specification, Clause 35 required VOH/VOL levels:

VOH min = 2.1 V VIH = 2.0 V (margin = 100 mV)

VOL max = 0.5 V VIL = 0.8 V (margin = 300 mV)

Impact:

The noise margin is reduced compared to IEEE compliant VIH and VIL levels which would have allowed 400 mV margin:

VOH min. = 2.1 V - VIH min. = 1.7 V => 400 mV margin and

VOL max = 0.5 V - VIL max = 0.9 V => 400 mV margin.

Die Revision Plan:

The VIH/VIL levels will be IEEE compliant in the next generation low power EN GigPHYTER DP83861.

7.2 GMII Hold Time

Issue:

GMII t_h =0.5 ns.

Description:

The IEEE specification 802.3z, Clause 35, states that the PHY receiving the TX_D, TX_EN, and TX_ER signals should require a maximum hold time = 0 ns with respect to the rising edge of GTX_CLK. The DP83891 requires a hold time of 0.5 ns.

Compatibility:

IEEE 802.3z specification, Clause 35 states that the MAC or controller outputting the TX_D, TX_EN and TX_ER signals has to supply a minimum "thold" = 0.5 ns which is sufficient hold time for the Gig PHYTER. However the timing margin is reduced to 0 ns, compared to an IEEE compliant receiver, which will have a margin of 0.5 ns.

Impact:

The timing margin is reduced compared to IEEE compliant t_h specification = 0 ns.

IEEE compliant t_h (margin) = t_h (output) -t_h (input) = 0.5 ns - 0 ns = 0.5 ns

DP83891 t_h(margin) = t_h (output) - t_h (input) = 0.5 ns - 0.5 ns = 0.0 ns

Die Revision Plan:

The hold time requirement will be IEEE compliant in the next generation low power EN GigPHYTER DP83861.

7.3 MII RX timing

Issue:

MII receive signal timing has a minimum clock to out delay of 3 ns.

Description:

The IEEE 802.3u specification, Clause 22 requires that the PHY outputting the RXD, RX_DV, and RX_ER signals, hold these signals for a minimum time of 10 ns, with respect to the rising edge of RX_CLK. The DP83891 holds these signals for ~= 3 ns. (This minimum hold time specification is also known as minimum output delay for RXD, etc.)

Compatibility:

Typically the MAC or controller receiving the RXD, RX_DV, and RX_ER signals will require a hold time of 0 ns max. Since the DP83891 supplies 3 ns of hold time, the MAC should be able to latch the data correctly.

Impact:

If there are significant differences in the path delays for the RX_CLK and RXD, etc. signals, then the MAC or controller might have less margin for hold time compared to IEEE compliant 10 ns hold time.

Die Revision Plan:

There are no plans for a change, as the original MII specs were written for support of external MII cables, and they are not applicable for GMII/MII interface.

7.4 10 Mb/s VOD

Issue:

10 Mb/s VOD levels are not IEEE compliant.

Description:

The IEEE 802.3 specification, Clause 14, requires that the 10 Mb/s output levels are within the following limits:

VOD = 2.2 - 2.8 V peak-differential, when terminated by a 100Ω resistor directly at the RJ-45 outputs.

The DP83891 10 Mb/s outputs levels are typically 1.58 V peak-differential.

Compatibility:

IEEE 802.3 specification, Clause 14, requires that a 10 Mb/s PHY should be able to correctly receive signal levels of Vin = 585 mV peak-differential. It also requires that any signal which is less than 300 mV peak-differential should be rejected by the PHY. The Gig PHYTER VOD level of 1.58 V peak- differential is received at the link partner with magnitudes exceeding Vin = 585 mV peak differential for cables up to 150 m. (Both CAT3 and CAT5 cables).

Impact:

In 10 Mb/s operation, the Gig PHYTER can receive and transmit up to 187 meters using CAT5 cable, and up to 150 meters using CAT3 cable. Hence there is no impact on the receive ability of the link partner due to the reduced levels of VOD transmitted by the Gig PHYTER.

Die Revision Plan:

There are no plans to change the 10 Mb/s VOD levels. Both the standard 10/100 link partners and the Gig PHYTER have no problems working over 150 m of CAT3 cable and 187 m of CAT5 cable during 10 Mb/s mode of operation.

7.5 Low VDD, High Temperature Sensitivity

Issue:

The DP83891 needs heatsinks and fans for temperature cooling, and might not work at the 0 -70 ˚C ambient temperature range if the supply voltage is low.

Description:

The application note “Gig PHYTER Temperature Guide” describes in detail the temperature specifications and cooling required for the DP83891. Special attention has to be given to guarantee that the actual VDD levels seen at the device pins don’t fall below VDD = 3.3 V, to guarantee operation over a wide temperature range.

7.5.1 Compatibility:

The DP83891 is specified for the commercial temperature range of 0 -70 ˚C ambient. However at low VDD values (VDD < nominal 3.3 V) the Gig PHYTER may no longer work over this range. Suggested operation temperature range is 0 -70 ˚C case temperature.

Impact:

The DP83891 will require heatsinks and fans to help with cooling as described in the application note “Gig PHYTER Temperature Guide”

Die Revision Plan:

The low voltage sensitivity at high temperature, will be fixed in the next generation low power EN GigPHYTER DP83861; thus guaranteeing operations over the 0 - 70 ˚C ambient temperature range. The EN Gig PHYTER will have significantly less power consumption, hence not requiring heatsinks and fans.

7.6 Software Download Required

Issue:

The Gig PHYTER requires firmware downloads.

Description:

Software to be downloaded will be supplied to the OEMs. Application note "DP83891 GigPHYTER E^2PROM Usage Guide" discusses usage of a serial E^2PROM to download firmware into multiple GigPHYTERs using a single E^2PROM. A second option for downloading firmware is through the management interface. (MDC/MDIO). A separate application note will be written explaining this second method of firmware upgrading.

Compatibility:

N/A

Impact:

The DP83891 will require software downloads, for full functionality as described in the datasheet.

Die Revision Plan:

The next generation DP83861 EN GigPHYTER will not require firmware downloads. However, further enhancements to the firmware might be made available to the users, to address new issues. See the FAQ section of the datasheet discussing some of the reasons why firmware updates might be beneficial.

7.7 GMII/MII Isolate Mode

Issue:

If the DP83891 is put into isolation mode it will actually be in power down mode.

Description:

IEEE specifications 802.3u and 802.3z, Clauses 22, require that a PHY which is put into isolation should ignore all activity on the twisted pair wire and on the MAC interface with the exception of MDC/MDIO management signalling. (It has to still respond to MDC/MDIO signals so that it can be put out of isolate mode by a register write to bit 10 of the Basic Mode Control Register.)

When the Gig PHYTER is put into isolate mode by writing bit 10 of the above register, it will actually go into power down mode. (IEEE 802.3u requires that bit 11 of the Basic Mode Control Register be used to put a device in power down mode. Gig PHYTER also goes into power down mode if this bit is set.)

Compatibility:

The IEEE specs have two separate modes called "isolate" and "power down." The Gig PHYTER in effect has only one of these modes which is "power down." However, the IEEE 802.3u Clause 22 says that: "The specific behavior of a PHY in the power down mode state is implementation specific." In power down mode the Gig PHYTER goes into a low power mode of operation and also isolates the GMII/MII interface as required by the isolate function. So this mode incorporates the requirements of both IEEE modes and therefore should not be a compatibility issue.

Impact:

No impact on operation.

Die Revision Plan:

The next revision DP83861 EN GigPHYTER will have two separate functions as defined by "isolate" and "power down" bit definitions of the IEEE specifications. The isolate function will only isolate the PHY without putting it into a low power mode.

7.8 Asymmetrical PAUSE

Issue:

The Asymmetrical PAUSE advertise bit (register 0x04, bit 11) is Read Only.

Description:

IEEE 802.3ab has assigned bit 11 of the Auto-Negotiation Technology Ability Advertisement Register to indicate Asymmetrical PAUSE capability. But in Gig PHYTER, this bit is a read only bit, with default value of zero. However, Asymmetrical PAUSE capability can still be advertised by writing to another register as described below.

Compatibility:

The Asymmetrical PAUSE advertise bit will be at a register location different from that specified by the IEEE. However, GigPHYTER can still advertise Asymmetrical PAUSE and can detect link partner's Asymmetrical PAUSE ability as shown in register 0x05.

Impact:

The following software register writes will be required if Asymmetrical PAUSE needs to be advertised:

Write to register 0x16 the value 0x0D

Write to register 0x1E the value 0x8084

Write to register 0x1D the value 0x0001

Please note that the order of the writes is important. Register 0x1E is a pointer to the internal expanded addresses. Register 0x1D contains the data to be written to or read from the internal address pointed by register 0x1E. The contents of register 0x1E automatically increments after each read or write to register 0x1D. Therefore, if one wants to confirm that the data write was successful, one should re-write register 0X1E with the original address and then read register 0X1D.

Die Revision Plan:

A future rev of Gig PHYTER will use register 0x04, bit 11 to advertise Asymmetrical PAUSE.

7.9 10 Mb/s Capability Bits

Issue:

The 10 Mb/s Full Duplex and Half Duplex capability is not shown correctly in register 0x01.

Description:

Register 0x01, bits 12 and 11 indicate the 10BASE-T Full Duplex and 10BASE-T Half Duplex capabilities of a PHY as specified by IEEE 802.3u Clause 22. The Gig PHYTER has both capabilities but these register bits don't show these capabilities. These are read only bits. However, the GigPHYTER will correctly advertise 10 Mb/s capabilities using the Auto-Negotiation advertisement register.

Compatibility:

No compatibility issues. However the higher level software needs to know that the Gig PHYTER is 10 Mb/s capable.

Impact:

There should be no effect on 10 Mb/s operation: The Gig PHYTER will correctly advertise 10 Mb/s capabilities using the Auto-Negotiation advertisement register; it will also correctly determine its link partners 10 Mb/s capability. The Gig PHYTER can also be forced to operate in 10 Mb/s mode. However the higher level software should NOT read bits 11 and 12 of register 0x01 to determine the 10 Mb/s capability of the Gig PHYTER. It should be told that Gig PHYTER is 10 Mb/s capable.

Die Revision Plan:

No plans for a fix exists. The work around suggested above is sufficient.

7.10 LED Pulse Stretching

Issue:

Some of the LED pulses are not stretched, and short time duration events might not be visible.

Description:

Typically the human eye can't sense LED activity which lasts for short durations. To make short duration events visible, the LED pulses have to be stretched in time to at least 50 ms. For the Activity, RX, TX and COL LEDs, the DP83851 turns on the LED only during the duration of the event and turns off the LED after the event is over.

Compatibility:

Driving the LEDs directly from the GigPHYTER will result in short events not being visible. To solve this problem, the LED can either be driven by the MAC/controller or by LED chips which can stretch timing.

Impact:

Short duration events like collisions, will not be noticeable when observing the LEDs. Similarly when there is a lot of TX/RX activity with small interframe gaps, the LEDs will appear to be on continuously, and not blink indicating interframe gaps.

Die Revision Plan:

Next generation low power EN GigPHYTER DP83861 will implement LED pulse stretching.

7.11 Forced 10 Mb/s mode

Issue:

When GigPHYTER is forced into 10 Mb/s operation it will falsely indicate good link when there is no link.

Description:

When forced into 10 Mb/s operation, the DP83891 Link LED will always be on, even if there is no link. However register 0x11 bit 2 will indicate correct link status. Register 0x01 bit 2 will also indicate correctly when link is lost.

Compatibility:

N/A

Impact:

In forced 10 Mb/s mode of operation, the correct link status can be obtained by reading register 0x01 bit 2. The Link LED should not be used to determine link status.

Die Revision Plan:

Next generation low power EN GigPHYTER DP83861 will correctly indicate link status, in forced 10 Mb/s mode.

7.12 PHY Address

Issue:

The PHY address can't be changed by register write.

Description:

The DP83891 PHY addresses have to be assigned by using strap options as indicated in the datasheet. Once the part comes out of reset or power-up, then the strap options for the address are latched and they can't be changed by management control.

Compatibility:

N/A

Impact:

If PHY address 0x00 is used as a strap option, this address will put the GigPHYTER into power down mode. After power on the Gig PHYTER can be put into regular operation by resetting bit 10 and 11 of the Basic Mode Control Register.

Typically in some applications, the PHY will come up with PHY address = 0x00 on power-up (due to strap options being set for address zero). This approach has the advantage that none of the PHYs, accidentally, will send garbled data on the line or to the MAC before it had a chance to properly initialize and is ready for operation.

(The Gig PHYTER default address setting, with all PHY Address pins floating, is 00001.)

Die Revision Plan:

There are no plans for a change. As explained above, there is no impact.

7.13 TX_TCLK

Issue:

The DP83891 doesn't support the TX_TCLK clock, which is used in some test modes.

Description:

The IEEE 802.3ab specification requires that the actual clock source used to transmit data on the CAT5 cable, be made available for some of the test modes. Clause 40, section 40.6.1.1.2 describes the test modes, and defines TX_TCLK. This clock is used to make transmit jitter measurements as described in section 40.6.1.2.5.

GigPHYTER doesn't provide this clock.

Compatibility:

The TX_TCLK signal is required in certain test modes by the 802.3ab specification. However it's not used for regular operation.

Impact:

The transmit jitter tests can't use the TX_TCLK signal. Instead, the waveform transmitted on the cable should be used to trigger the scope. There is no impact to the regular 1000BASE-T operation.

Die Revision Plan:

Next generation low power EN GigPHYTER DP83861 will have this signal available during some of the test modes.

8.0 Gig PHYTER Frequently Asked Questions:

Q1: What is the difference between TX_CLK, TX_TCLK, and GTX_CLK?

A1: All the 3 clocks above are related to transmitting data. However, their functions are completely different:

TX_CLK: This is used for 10/100 Mb/s transmit activity. It has two separate functions:

— It's used to synchronize the data sent by the MAC and to latch this data into the PHY.

— It's used to clock transmit data on the twisted pair.

The TX_CLK is an output of the PHY and is part of the MII interface as described in IEEE 802.3u specification, Clause 28.

GTX_CLK: This is used for 1000 Mb/s transmit activity. It has only one function:

— It's used to synchronize the data sent by the MAC and to latch this data into the PHY.

The GTX_CLK is NOT used to transmit data on the twisted pair wire. For 1000 Mb/s operation, the Master PHY uses the X1 clock to transmit data on the wire, while the Slave PHY uses the clock recovered from the channel A receiver, as the transmit clock for all four pairs.

The GTX_CLK is an output of the MAC and is part of the GMII interface as described in IEEE 802.3z specification, Clause 35.

TX_TCLK: This is used for 1000 Mb/s transmit activity. It has only one function:

— It's used in "Test Modes 2 & 3" to measure jitter in the data transmitted on the wire.

As explained above during the discussion of GTX_CLK, either the X1 clock or the clock recovered from received data is used for transmitting data; depending on whether the PHY is a MASTER or a SLAVE. TX_TCLK represents the actual clock being used to transmit data.

The TX_TCLK is an output of the PHY and can be enabled to come out on pin 192 (during Test Mode 2 and 3 it is automatically enabled). This is a requirement from the IEEE 802.3ab specification, Clause 40.6.1.2.5. (This clock is only available in the next generation Enhanced GigPHYTER DP83861)

Q2: What happens to the TX_CLK during 1000 Mb/s operation? Similarly what happens to RXD[4:7] during 10/100 Mb/s operation?

A2: As mentioned in **A1** above, TX_CLK is not used during the 1000 Mb/s operation, and the RXD[4:7] lines are not used for the 10/100 operation. These signals are outputs of the GigPHYTER. To simplify the MII/GMII interface, these signals are driven actively to a zero volt level. This eliminates the need for pull-down resistors which would have been needed if these pins were left floating during no use.

Q3: What happens to the TX_CLK and RX_CLK during Auto-Negotiation and during idles?

A3: During Auto-Negotiation the GigPHYTER drives a 25 MHz clock on the TX_CLK and RX_CLK lines. In 10 Mb/s mode, these lines are driven by a 2.5 MHz clock during idles. In 100 Mb/s mode they are driven by a 25 MHz clock during idles. In 1000 Mb/s mode they are driven by a 125 MHz clock during idles.

Q4: Why doesn't the GigPHYTER complete Auto-Negotiation if the link partner is a forced 1000 Mb/s PHY?

A4: IEEE specifications only define "parallel detection" for 10/100 Mb/s operation. Parallel detection is the name given to the Auto-Negotiation process where one of the link partners is Auto-Negotiating while the other is in forced 10 or 100 Mb/s mode. In this case, it's expected that the Auto-Negotiating PHY establishes half-duplex link, at the forced speed of the link partner.

However, for 1000 Mb/s operation this parallel detection mechanism is not defined. Instead, any 1000BASE-T PHY can establish 1000 Mb/s operation with a link partner for the following two cases:

— When both PHYs are Auto-Negotiating,

— When both PHYs are forced 1000 Mb/s and when one of the PHYs is manually configured for MASTER and the other is manually configured for SLAVE.

Q5: My two Gig PHYTERs won't talk to each other, but they talk to another vendor's PHY.

A5: Avoid using Manual Master/Slave Configuration. If all PHYs on a switch box are configured for the same Master/Slave value, then they can't talk to each other, because one of the link partners has to be a slave while the other has to be a Master.

Q6: You advise not to use Manual Master/Slave configuration. How come it's an option?

A6: Manual Master/Slave configuration is similar to manual forcing of 10 or 100 Mb/s operation. The only way it can work is if both link partners are forced to compatible speed of operation, or if at least one of them is Auto-Negotiating. Since there is no way of knowing ahead of time, if the link partner will also use hardwired manual Master/Slave setting, there is no way to guarantee that there won't be a conflict (i.e both PHYs are assigned Master, or both PHYs are assigned Slave value.)

Some applications automatically hardwire a switch for Master and a Node card for a Slave status. However this is wrong, since most of the early use for 1000BASE-T is for switch to switch backplane uplink ports, and hence this will result in the both link partners assigned to Master status. This will cause a conflict and prevent establishment of link.

Q7: How can I write to GigPHYTER expanded address or RAM locations? Why do I need to write to these locations?

A7: The following functions require access to expanded address:

— Asymmetric Pause Advertise

— Auto MDIX Disable

— Force 10 Mb/s Good Link

— Disable 10 Mb/s Jabber

— Read Latest Firmware Revision

— Read ROM Revision

Typically this kind of functionality should be available by direct register writes. The next generation EN GigPHYTER DP83861 will have these options controllable, in a simple manner by direct register writes. Gig PHYTER requires

reads and writes to RAM to accomplish these tasks. As a sample procedure, we show how to advertise Asymmetrical PAUSE:

The following software register writes will be required if Asymmetrical PAUSE needs to be advertised:

— 1)Power down the GigPHYTER (i.e. set bit 11, register 0x00. This is to make sure that during RAM writes, the standard operation of the part doesn't interfere with what we are writing to the RAM.)

— 2) Write to register 0x16 the value 0x000D (This allows access to expanded access for 8 bit read/write)

— 3) Write to register 0x1E the value 0x8084

— 4) Write to register 0x1D the value 0x0001

— 5) Take the GigPHYTER out of power down mode (i.e. reset bit 11 of register 0x00.)

Note that the order of the writes is important. Register 0x1E is a pointer to the internal expanded addresses. Register 0x1D contains the data to be written to or read from the internal address pointed by register 0x1E. The contents of register 0x1E automatically increments after each read or write to register 0x1D. Therefore, if one wants to confirm that the data write was successful, one should re-write register 0X1E with the original address and then read register 0X1D.

All register writes are 16 bits. However the RAM data is 8 bits wide. In the 8 bit read/write mode as described above in step 2, the lowest 8 bits of the register will be written to the RAM location pointed by register 0x1E.

For each one of the desired functions listed above (e.g. disable jabber), steps 1,2, and 5 have to be followed. Depending on the exact functionality required a different register location and different data value have to be entered at steps 3) and 4).

Q8: What specific addresses and values do I have to use for each of the functions mentioned in Q7 above?

A8:

— **Advertise Asymmetrical Pause:** address 0x8084, value 0x01

— **Disable Auto MDIX**: address 0x808B, value 0x03. (The default value is 0x00 which enables Auto MDIX) After disabling Auto MDIX, the MDIX value can be set through normal 16 bit register access, to register 0x15, bit 0. If bit 0 is set to '1', the GigPHYTER will crossover channels A and B. If this bit is a '0', then the GigPHYTER will not crossover channels A and B.

— **Force 10 Mb/s Good Link**: address 0x02C0, bit 2 set. (Default bit 2 = '0')

— **Disable 10 Mb/s Jabber Function**: address 0x02C0, bit 5 set. (Default bit 5 = '0')

— **Read Latest Firmware Revision:** addresses 0x8402 and 0x8403 contain a two character revision number. These are ASCII coded characters: The latest version of GigPHYTER DP83891 will have rev code = "09"which corresponds to "0" =0x30 and "9" = 0x39.

— **Read Latest Hardware (ROM) Revision:** addresses 0xD002 and 0xD003 contain a two character revision number. These are ASCII coded characters: Production version of GigPHYTER DP83891 will have rev code = "3B" which corresponds to "3" =0x33 and "B" = 0x42.

— **E^2PROM checksum:** RAM location 0x83FE contains the value of the computed checksum, and RAM location 0x83FF contains the checksum indicated by the firmware which was loaded.

Q9: How can I do firmware updates? What are some of the benefits of the firmware updates?

A9: Firmware updates have many uses. Some of these uses are:

— If future bugs are discovered, they could be fixed (or work arounds implemented) using firmware updates. Typically for hardwired PHYs without the firmware update option, the customer has to "live with the bug", or try to implement a software work around.

— Enhancements and additional functionality can be added to the GigPHYTER. For example, the GigPHYTER might be able to detect cable length and indicate this length in a register. These functions are not implemented in hardware at this time, and they will be added as enhancements using firmware updates.

To update firmware there are two options:

1) Use E^2PROM. This is described in the Application Note "DP83891 GigPHYTER E^2PROM Usage Guide." (Available now.) National Semiconductor will supply the .HEX files needed to program the serial E^2PROM devices.

2) Using the driver and/or management interface (MDC/MDIO). An application note on this method will be available soon. Basically the procedure will be similar to what is described in answer 7. The main difference is that 16 bit read/write mode will be used. As discussed earlier in answer 7, all register writes are 16 bits. However the RAM data is 8 bits wide. In the 8 bit read/write mode as described earlier, the lowest 8 bits of register 0x1D will be written to the RAM location pointed by register 0x1E. This is sufficient for single register writes and this mode was used to make the necessary RAM write in answer 7. However for loading the entire 14 KB of RAM, this method is not efficient. Since each MDC/MDIO read/write accesses a 16 bit register, it is more efficient to use one MII register write, and let the internal software break this into two 8 bit RAM writes. To achieve this, we will program a 16 bit read/write mode into register 0x16, instead of the earlier 8 bit mode as described in answer 7. In this mode each 16 bit write into register 0x1D, is broken into 2 internal 8 bit RAM writes. The internal hardware will automatically, increment the RAM address pointer register 0x1E after each 8 bit write. It will first use the lowest 8 bits of register 0x1D to write to the RAM location pointed by register 0x1E. Then it will increment the address pointed by 0x1E by one, and write the most significant 8 bits of 0x1D into the next RAM location. This is all transparent to the user, who only has to set the 16 bit read/write mode as described in step 2 below and then do regular 16 bit MDC/MDIO writes.

— 1)Power down the GigPHYTER (i.e. set bit 11, register 0x00. This is to make sure that during RAM writes, the standard operation of the part doesn't interfere with what we are writing to the RAM.)

— 2) Write to register 0x16 the value 0x0006 (This allows access to expanded access for 16 bit read/write)

— 3) Write to register 0x1E the value 0x8400. (The starting address of RAM)

— 4) Write to register 0x1D the desired value. The higher 8 bits of this register will be written into location pointed by register 0x1E above. Then the location pointed to by reg-

ister 0x1E will be incremented by one, automatically, to point to the next location. Next, the 8 least significant bits of register 0x1D will be written to the RAM location pointed by register 0x1E.

(The values to be written to all the RAM locations will be supplied by National Semiconductor in a .HEX file.)

— 5) Write to register 0x1D the next desired value.

— 6) Continue repeating step 5 for all data to be written as shown in the .HEX file to be supplied by National Semiconductor.

— 7) Write 0x8400 to register 0x1F. This starts execution of down loaded code at address 0x8400.

— 8)Wait for 1.024 ms. (i.e. no MDC/MDIO access for 1.024 ms)

— 9) Read register 0x00 (This read is needed to clear an interrupt problem.)

— 10) Take the GigPHYTER out of power down mode (i.e. reset bit 11 of register 0x00.)

—

Q10: How long does Auto-Negotiation take?

A10: Two GigPHYTERs typically complete Auto-Negotiation and establish 1000 Mb/s operation within 5 seconds. 1000BASE-T Auto-Negotiation process takes longer than the 10/100 Mb/s. One of the reasons for this is the use of Next Page exchanges during 1000 Mb/s negotiation.

Q11: I know I have good link, but register 0x01, bit 2 "Link Status" doesn't contain value = '1' indicating good link.

A11: This bit is defined by IEEE 802.3u Clause 22. It indicates if the link was lost since the last time this register was read. Its name is (given by IEEE) is perhaps misleading and it will be better named as "Link lost" bit. If the actual present link status is desired, then either this register should be read twice, or register 0x11 bit 2 should be read. Register 0x11 shows the actual status of link, speed, and duplex regardless of what was advertised or what has happened in the interim.

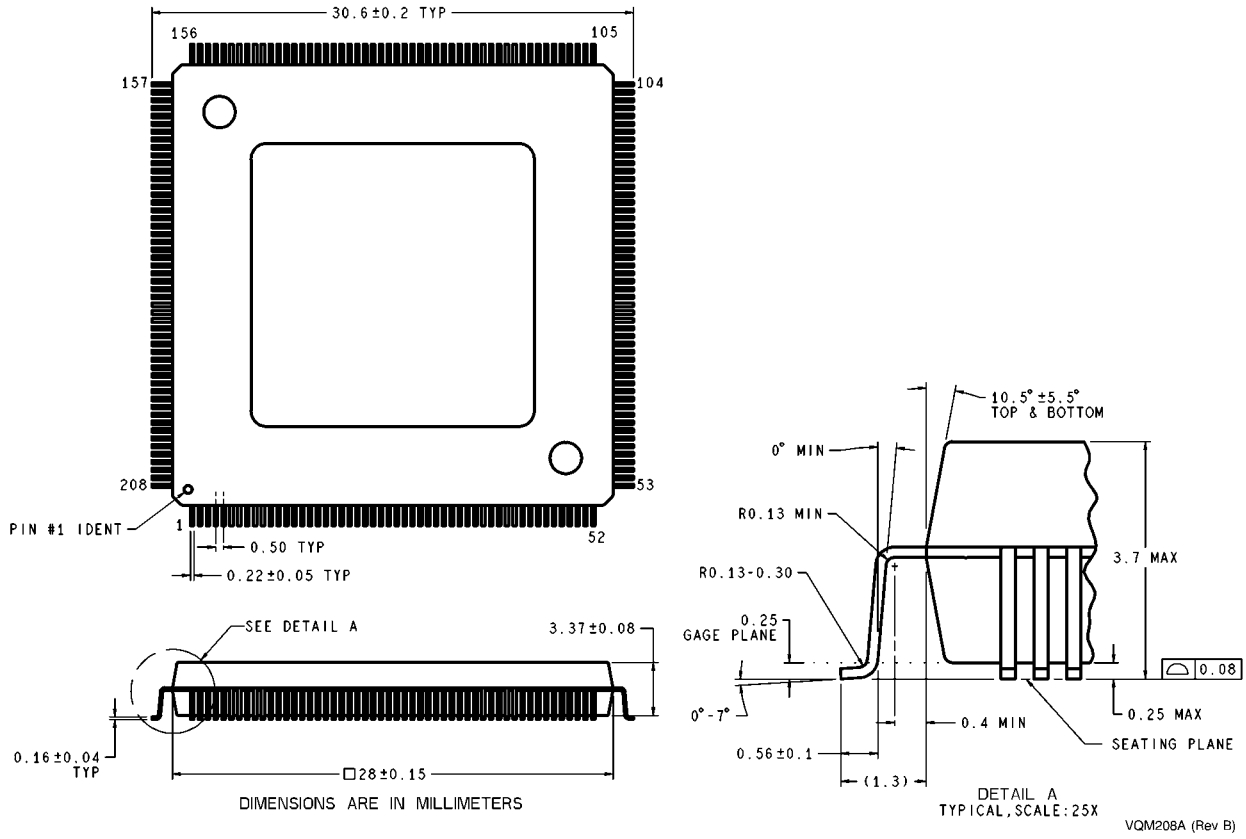
Q12: I have forced 100 Mb/s operation but the 100 Mb/s speed LED doesn't come on.

A12: Speed LEDs are actually an AND function of the speed and link status. Regardless of whether the speed is forced or Auto-Negotiated, there has to be good link, before the speed LEDs will come on.

Q13: Your reference design shows pull-up or pull-down resistors attached to certain pins, which conflict with the pull-up or pull-down information specified in the datasheet?

A13: The pull-up or pull-down information specified in the pin description section of the datasheet, indicate if there is an internal pull-up or pull-down resistor at the IO buffer used for that specific pin. These resistors are between 25 - 65 kΩ. They will determine the default strap value if the pin is floated. If the default value is desired to be overwritten, then an external 1 kΩ pull-up or pull-down resistor can be used.

9.0 Physical Dimensions inches (millimeters) unless otherwise noted



208 Lead Plastic Quad Flat Pack
Order Number DP83891VQM
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