

DP83862 Dual GigPHYTER®

10/100/1000 Ethernet Physical Layer

General Description

The DP83862 is a full featured dual Physical Layer transceiver with integrated PMD sublayers to support 10BASE-T, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83862 is designed using advanced DSP technology. Its robust performance and error free operation beyond IEEE specifications ensure its rapid deployment to replace existing 10/100 networking equipment. In addition, the DP83862 is fully interoperable with existing Gigabit solutions in the marketplace. It uses state of the art 0.18 μm , 1.8 V CMOS technology, fabricated at National's South Portland, Maine Facilities.

The DP83862 is designed for easy implementation of 10/100/1000 Mb/s Ethernet LANs. Each port interfaces directly to Twisted Pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3u Standard Media Independent Interface (MII) or the IEEE 802.3z Gigabit Media Independent Interface (GMII). It also supports the reduced pin count serial GMII (SGMII) interface. (8 pins per port.)

Applications

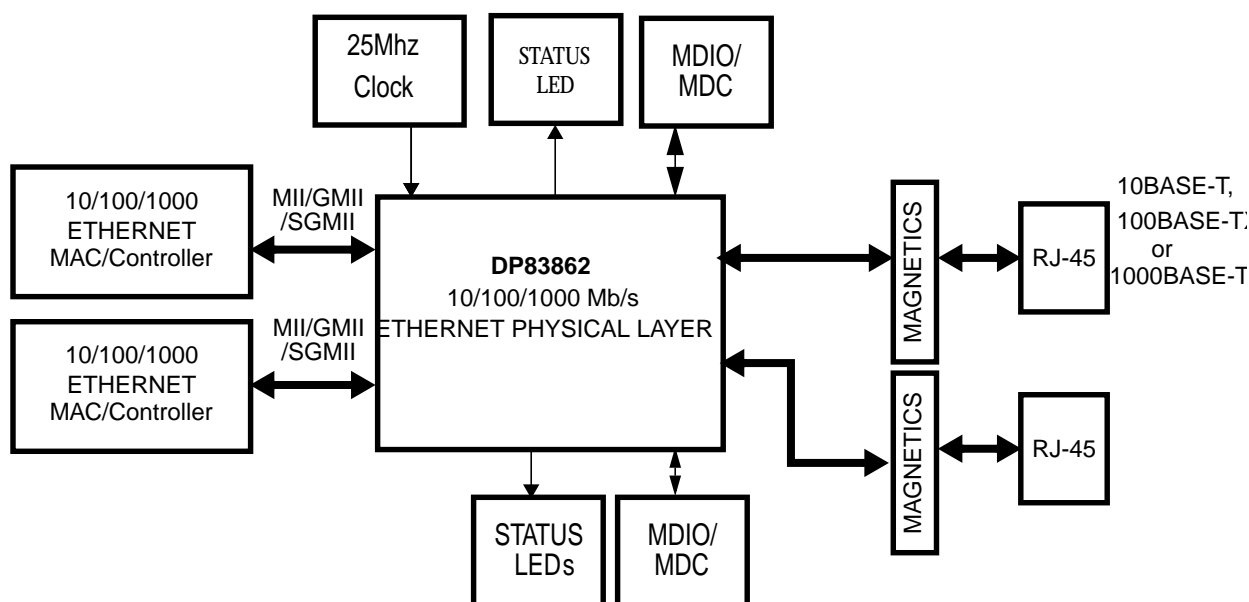
The DP83862 fits applications in:

- Switches with 10/100/1000 Mb/s capable ports

Features

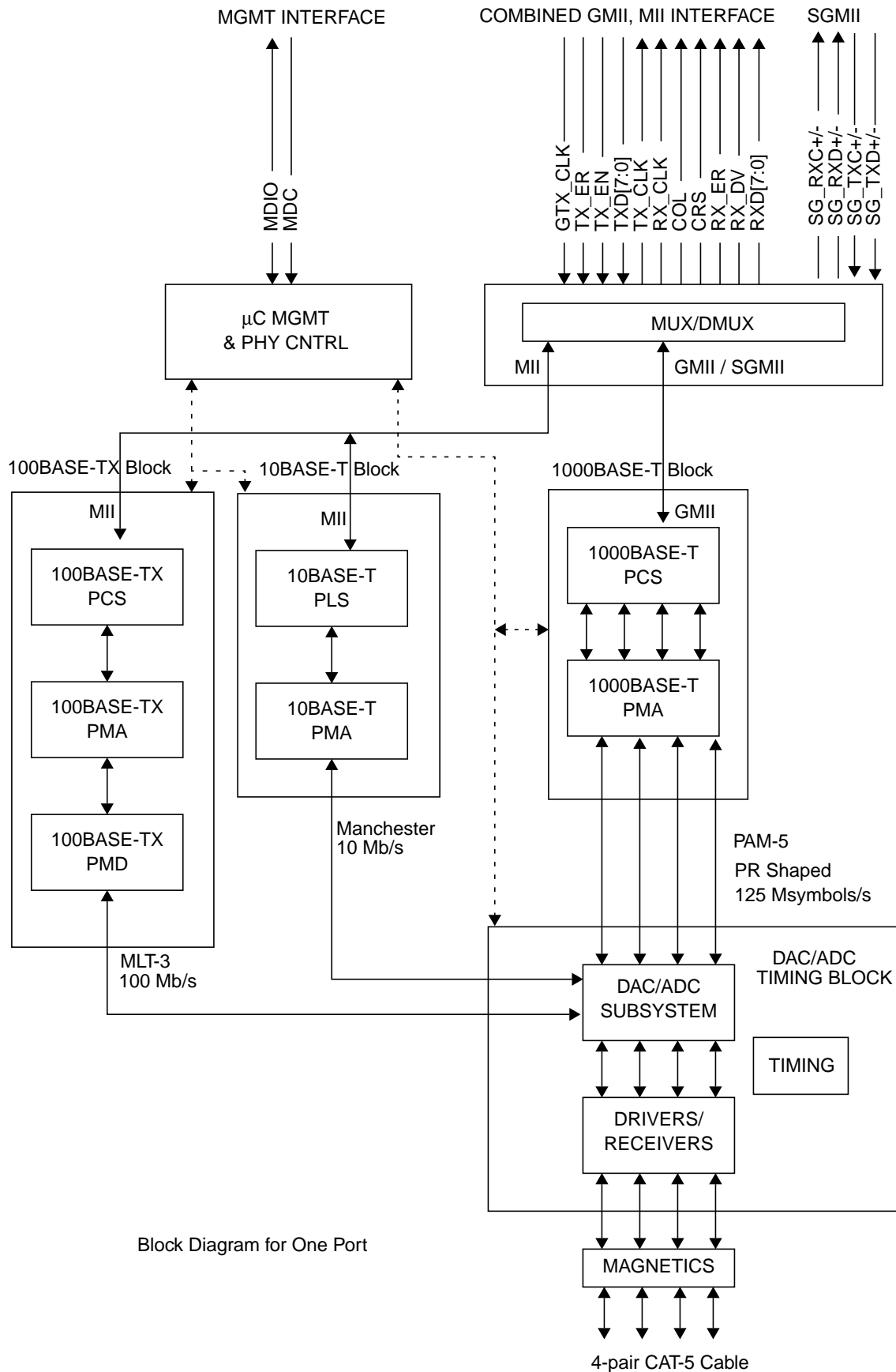
- 10BASE-T, 100BASE-TX and 1000BASE-T capable
- Adaptive equalization and Baseline Wander compensation.
- IEEE 802.3u Auto-Negotiation and Parallel Detection
 - Fully auto-negotiates between 1000 Mb/s, 100 Mb/s, and 10 Mb/s full duplex and half duplex devices
- 3.3 V MAC interfaces:
 - IEEE 802.3u MII
 - IEEE 802.3z GMII
 - Serial GMII (SGMII)
- LED support (Link, Speed, Activity, Collision, TX and RX indications)
- Supports Auto-MDIX at all speeds
- Management Register Set
- Supports a 25 MHz oscillator for reference clock
- Requires only two power supplies 1.8 V & 3.3 V
- 432 pin BGA package

System Diagram



Phyter® is a trademark of National Semiconductor Corporation.

Block Diagram (Showing One Port)



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