DRIC-DVC-102

3 Channel D/R Integrated Circuit

FEATURES

- Programmable Time Delay of Analog Signals
- Capture and Loop Playback after Trigger
- Up To 3 Analog Channels
- Playback Data At Reduced Rates
- 175 ms Maximum Delay With External Memory
- Single 5 Volt Supply
- 100 Lead Thin Quad Flat Pack
- Available In Die Form

APPLICATIONS

- Munitions Testing
- Industrial Instrumentation
- Store And Forward Data Acquisition
- System Health Monitoring

GENERAL DESCRIPTION

The 3 Channel Delay/Repeater (D/R) IC provides three channels of delayed or delayed and repeated analog signals with a bandwidth range of 0 to 60 KHz. The D/R provides up to 20 ms of time delay in 5 ms increments on-chip. A maximum delay of 175 ms can be supported using an external commercial-off-the-shelf (COTS) SRAM.

A block diagram of the 3 Channel D/R IC is shown in Figure 1. It uses a mixed signal implementation where three independent analog-to-digital (A/D) converters with 12-bit accuracy are used to sample the input signal waveform. The 60 KHz signal bandwidth is approximately 40 percent of the sample rate. This meets the Nyquist criteria and allows for anti-alias filter rolloff.

The digitized outputs of the A/D converters (12 bits at 150 KSPS) are bussed and written to the internal memory (3 channels x 12 bits x 150 KSPS x 0.02 sec = 108 Kbits) or external memory interface (256K x 8 bits SRAM).

After the data is read from memory, it is fed into three independent digital-to-analog (D/A) converters for signal reconstruction. Output filters remove spurs generated by the D/A converters.

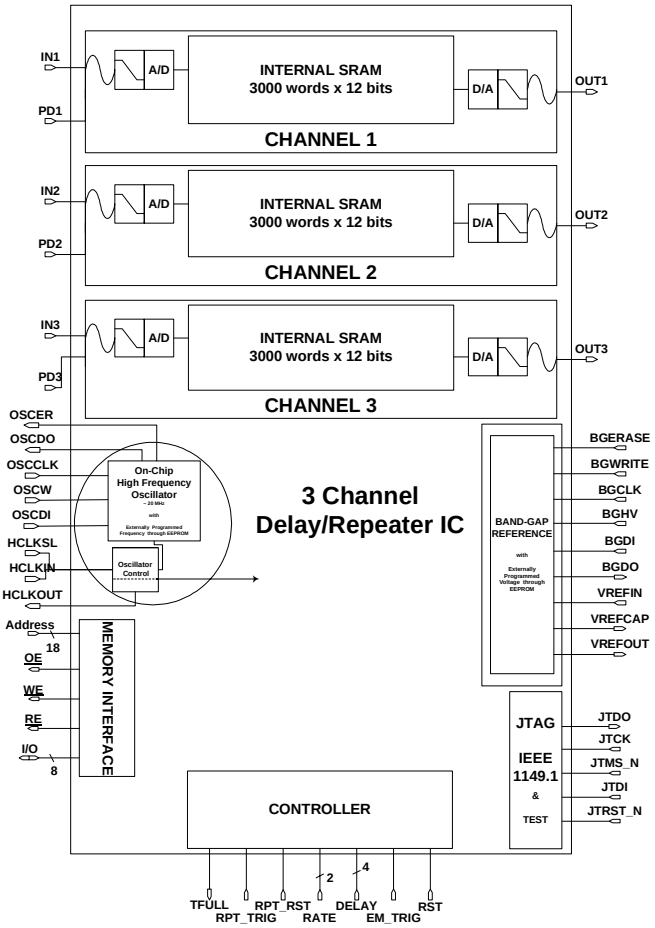

Figure 1: Functional Block Diagram

PROGRAMMING

The 3 Channel Delay/Repeater IC uses discrete signals that may be set using dip switches and/or jumpers to program the input control signals. The following Tables illustrate the D/R's programming functions.

Truth Tables

TRIG	RST	Function		Rate	Playback Rate
0	0	Power-up FIFO function		00	x1.0
1	0	Repeat function		01	x1.0
0	1	Return to FIFO function		10	x0.5
1	1	No Action		11	x0.1

Internal Memory

Delay	Time Delay (ms)
0001	5
0010	10
0011	15
0100	20

External Memory

Delay	Time Delay (ms)
1001	25
1010	50
1011	75
1100	100
1101	125
1110	150
1111	175

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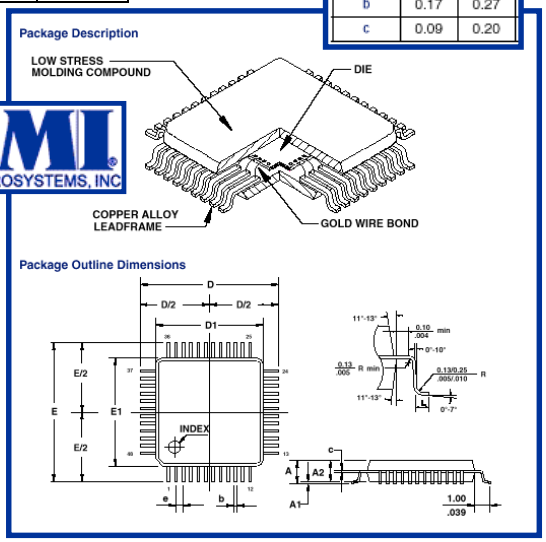
HARDENED SUBMINIATURE TELEMETRY AND SENSOR SYSTEM
DATA ACQUISITION CHIPSET

SPECIFICATIONS

Parameter		Symbol	Min	Typ	Max	Units
Power Requirements						
Supply Voltage	Digital	V_{DDD}	4.5	5.0	5.5	V
	Analog	V_{DDA}	4.5	5.0	5.5	V
Supply Current	Operating	I_{DD}		50		mA
	Low-Power	I_{PD}		TBD		µA
Power Consumption	Operating			250		mW
	Low-Power			TBD		µW
Dynamic Specifications						
Operating Ambient Temperature		T_A	-40	25	85	°C
External Voltage Reference		V_{EXT}	1.5	2.25	2.5	V
Internal Voltage Reference		V_{REF}	2.13	2.25	2.37	V
Resolution					12	Bits
Clock Frequency		F_C		19.2	20	MHz
Conversion Rate		F_S		150	156	KSPS
Input Frequency Response			DC		60K	Hz
Signal to Noise		S/N	68			dB
Total Harmonic Distortion		THD		0.4	1	%
Interchannel Crosstalk					1.25	mVrms
Interchannel Gain Mismatch					±0.5	dB
Absolute Gain Error				± 1	± 2	%
Gain Drift				100	200	ppm/°C
Analog Inputs						
Full Scale Input Voltage		IN1-IN3		$1.8*V_{REF}$	4.2	V
Input Capacitance		C_{INA}			15	pF
Input Resistance		R_{INA}	1M			Ω
Analog Outputs						
Full Scale Output Voltage		OUT1-OUT3		$1.8*V_{REF}$	4.2	V
Output Resistance		R_{OA}		600	1K	Ω
External Load Capacitance		C_{LA}			100	pF
External Load Resistance		R_{LA}	10K			Ω
Clock						
Duty Ratio		CLK	45	50	55	%
Clock High Voltage		V_{CLKH}	$0.7*V_{DDD}$		V_{DDD}	V
Clock Low Voltage		V_{CLKL}	0		$0.3*V_{DDD}$	V
Digital Inputs						
Input High Voltage		V_{INHD}	2.4		V_{DDD}	V
Input Low Voltage		V_{INLD}	0		0.8	V
Input Current		I_{IND}			± 1	µA
Input Capacitance		C_{IND}			10	pF
Digital Outputs						
Output High Voltage		V_{OHD}	4.0		V_{DDD}	V
Output Low Voltage		V_{OLD}	0		0.4	V

	100	
	14x14	
Symbol	MIN.	MAX.
A	-	1.60
A1	0.05	0.15
A2*	1.35	1.45
D	16.00 BSC	
D/2	8.00 BSC	
D1	14.00 BSC	
E	16.00 BSC	
E/2	8.00 BSC	
E1	14.00 BSC	
L	0.45	0.75
e	0.50 BSC	
b	0.17	0.27
c	0.09	0.20



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PACKAGING

The Thin Quad Flatpack (TQFP) plastic package family is a reduced thickness plastic surface mount package. The 100 lead TQFP packages are constructed using the latest wire bonding and molding technology to provide surface mount packages with a body thickness of 1.0 or 1.4mm. This package finds many applications where size and weight are a critical factor.

The 3 Channel D/R IC will be available in die form.

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