DPS8101 Highly Integrated ATU-R Analog Front End IC Digital Interface V0.1.0

DataPath Systems, Inc.

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1 General Description

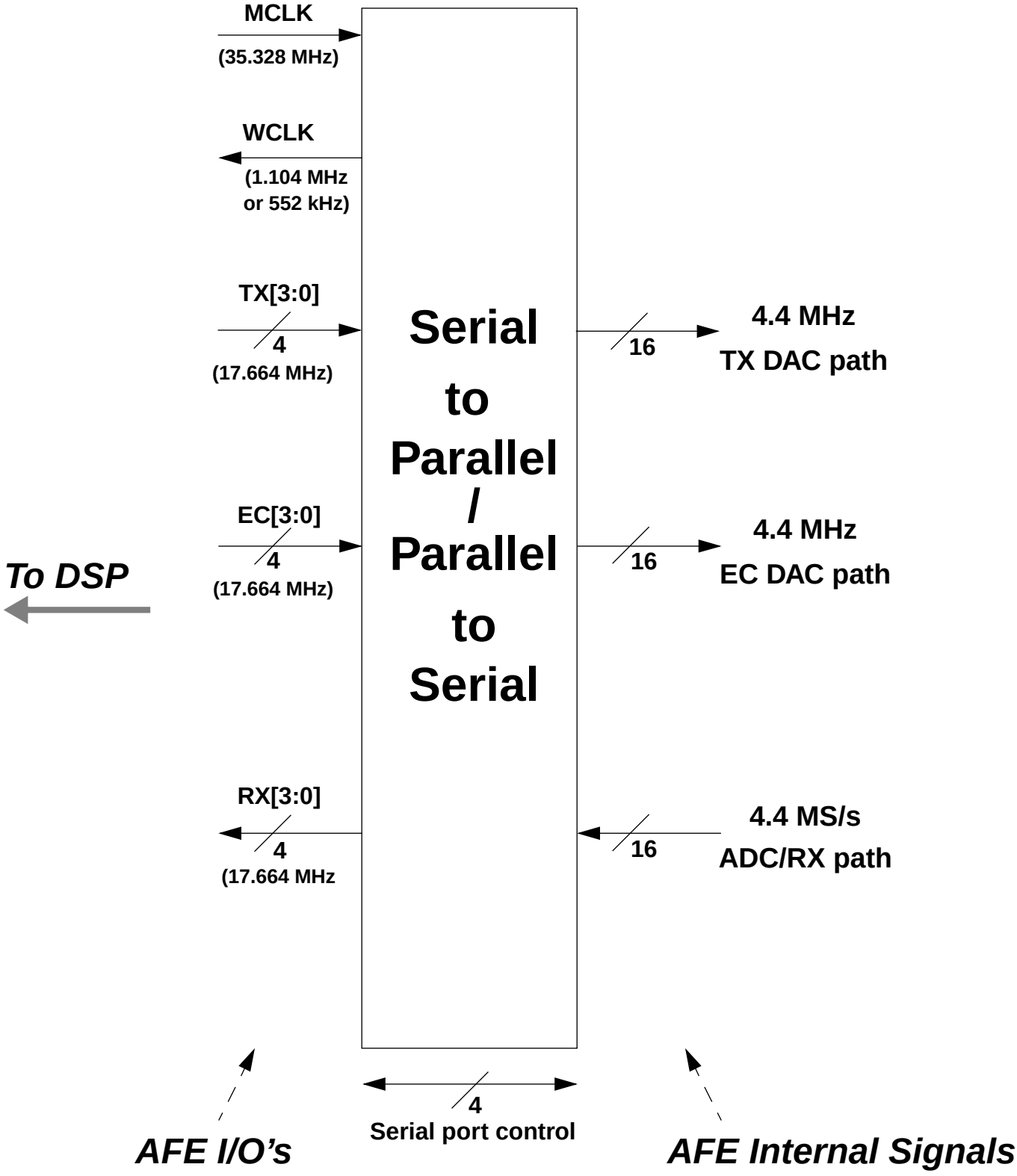
The DPS8101 is a highly integrated component containing a complete ADSL analog front end for the remote terminal side, with support for *G.dmt* and *G.lite*.

The primary digital data interface consists of three 4-bit ports: primary transmit (TX) signal; echo (EC) signal, for support of analog echo cancellation, if desired by the user; and receive (RX) signal. The primary TX data stream and the EC data stream each consist of a 4-bit word at 17.6 MHz, and thus support up to a 4.416 MHz incoming data rate, with a 16-bit DAC word. The RX data consists of a 4-bit stream at 17.6 MHz, to support up to 4.416 MHz outgoing data rate, with a 16-bit ADC word.

The interface is programmable, so that if a lower data rate is preferred on either TX or RX sides for a given transceiver scenario, few pins may be used. Specifically, the TX, EC, and RX data streams can be programmed to use 1-bit, 2-bit, or 4-bit data.

The chip requires a single low-jitter 35.328 MHz clock to be applied at the MCLK pin. All clock generation is performed internally and all converter and S/H clocks in both RX and TX paths are directly derived from MCLK. An independent asynchronous 4-wire serial port is used for control of gains, attenuations, modes etc.

2 Digital Interface Functionality



3 Digital Pin Function Description

In the following table: DI = digital input, DO = digital output, DIO = digital I/O.

Pin Name	Type	Pin Function Description
MCLK	DI	Master reference clock input: 35.328 MHz
WCLK	DO	Strobe / frame-sync digital output
TX3,...,TX0	DI	TX digital inputs
EC3,...,EC0	DI	EC digital inputs
RX_3,...,RX_0	DO	RX digital outputs
S_DOUT	DO	Serial port data output from IC
S_CLK	DI	Serial port clock input to IC
S_EN	DI	Serial port enable input to IC
S_DIN	DI	Serial port data input to IC
RESETB	DI	Resets internal state of chip (active low)
GP5, GP4, ..., GP0	DO	General purpose 5V digital outputs (available to the user for controlling other elements on the board)

4 Digital Interfaces

4.1 ADC and DAC Digital Interfaces

1 The interface runs at a a clock rate IFCLK = MCLK/2. This clock is generated on-chip by dividing down from a master clock MCLK. For ADSL, it is always generated by dividing down the 35.328 MHz MCLK clock, and so the interface always runs at 17.664 MHz.

2 To allow for asymmetrical data rates and to allow flexibility in the number of pins used, as well as to allow minimization of digital noise coupling, both TX and RX can be programmed as 4-bit, 2-bit, or 1-bit modes. This also allows for future bonding options using fewer pins. Since the interface runs at 17.664 MHz, and the digital data to/from the converters is 16-bit wide, this implies that data transfer rates of 4.416 MHz (using 4-bit mode), 2.208 MHz (using 2-bit mode), and 1.104 MHz (using 1-bit mode) can be supported. These modes are set under register control. **TX and RX sides may be programmed independently; TX and EC are identical.**

3 Below in Figs. 1–8 are diagrams showing explicitly the way DAC and ADC words are transmitted to the AFE during nibble-mode, 2-bit mode, and serial mode, for the TX and RX sides, respectively. In the DA[15:0], AD[15:0], words: bit 15 is the MSB and bit 0 is the LSB. *For simplicity, these diagrams only show the primary transmit digital data, TX[3:0]. The timing and behavior of the 4-bit bus for the echo data, EC[3:0], is identical.*

4 In nibble mode, TX[3:0], EC[3:0], and RX[3:0] are the signals that appear on the pins. DA[15:0], AD[15:0] are the internal 16-bit parallel words. In 2-bit mode, the interface uses 2 pins per channel and a similar protocol, as shown in Fig. 10 for the TX case. For example, pin TX[3] receives the high byte DA[15:8] serially at the same time that pin TX[1] receives the low byte DA[7:0] serially. So, during the entire frame, two 16-bit DAC words are received.

5 There a strobe or frame-sync signal called “WCLK” which is a start-of-word marker and is always at frequency IFCLK/16. WCLK is an *output* from the AFE, and may be considered a “start of words” signal. Its rising edge should be used by the DSP to align the outgoing transmit digital data and incoming receive data. WCLK transitions only on the rising edge of the IFCLK clock, and is therefore aligned also to the rising edge of the MCLK clock. WCLK is common to TX and RX data streams — i.e., the TX and RX data frames are exactly aligned.

6 WCLK is drawn as a 1/16 duty cycle clock for convenience in the following diagrams. However, it is implemented as a 50% duty cycle clock. So, the interpretation is that the *start* of the 16-bit frame is indicated by the simultaneous *rising edges* of IFCLK and WCLK. Thus, there is one WCLK rising edge for each 16-bit word in serial mode.

7 MCLK is the master clock *input* to the AFE. This clock is immediately divided down to IFCLK. The diagrams also show the internally generated IFCLK clock (not brought to a pin on the chip). *Data is transmitted from the AFE on the rising edge of the IFCLK and sampled by the AFE on the falling edge of the IFCLK clock.*

8 It is understood that the DSP samples the RX data on the falling edge of the IFCLK clock (generated presumably inside the DSP) or equivalently by counting edges of the 35.328 MHz MCLK. This allows the RX data from the AFE to have more delay than if they were sampled by the next falling edge of the MCLK clock.

9 The state of the interface after power-on is undefined: the interface resets itself on the next 16-bit frame (i.e., the first complete frame) following power-on.

10 There is no tristate control on the outputs.

11 In serial or 2-bit modes, or if the echo data stream is not used, the digital values on the unused pins do not matter — these values are ignored by the AFE, and so the interface and data transfer rates may be re-configured by programming registers, using the same PCB layout. However, note that the AFE does not have internal pull-downs on the digital inputs, so it is recommended that unused inputs should be pulled to GND on the board thru pullup or pulldown resistors. Similarly, if the echo path is not used, the EC[3:0] digital inputs should be pulled to GND.

12 With respect to electrical levels, the AFE digital inputs are both 3.3V CMOS and TTL compatible, and the *HIGH* level on the ADC outputs is set by the power supply voltage VDD_ADIO. It will always be possible to set the digital output HIGH level to a separate voltage. With respect to the threshold or trigger level for digital inputs to the AFE, DataPath guarantees that they operate correctly with a HIGH level of 2.5 V.

13 Note: in the DPS8101, as in the DPS8001, the DAC always runs at 4.416 MHz. If the incoming TX data rate is 2.208 MHz or 1.104 MHz, repeated samples are generated at the 4.416 MHz rate.

14 Both 2’s complement and offset binary formats are available for the RX data. The TX and EC data use offset binary format only.

15 All of the above modes (1-bit, 2-bit, 4-bit, EC on/off, sample rates etc.) are controlled by on-chip control registers, accessible thru the 4-wire serial control port. The details of these registers will be described in the DPS8101 Advance Data Sheet. The RX and TX/EC interfaces can be independently programmed to 1-bit, 2-bit, or 4-bit modes.

A timing diagram for the TX interface is shown below for 4-bit (nibble) mode.

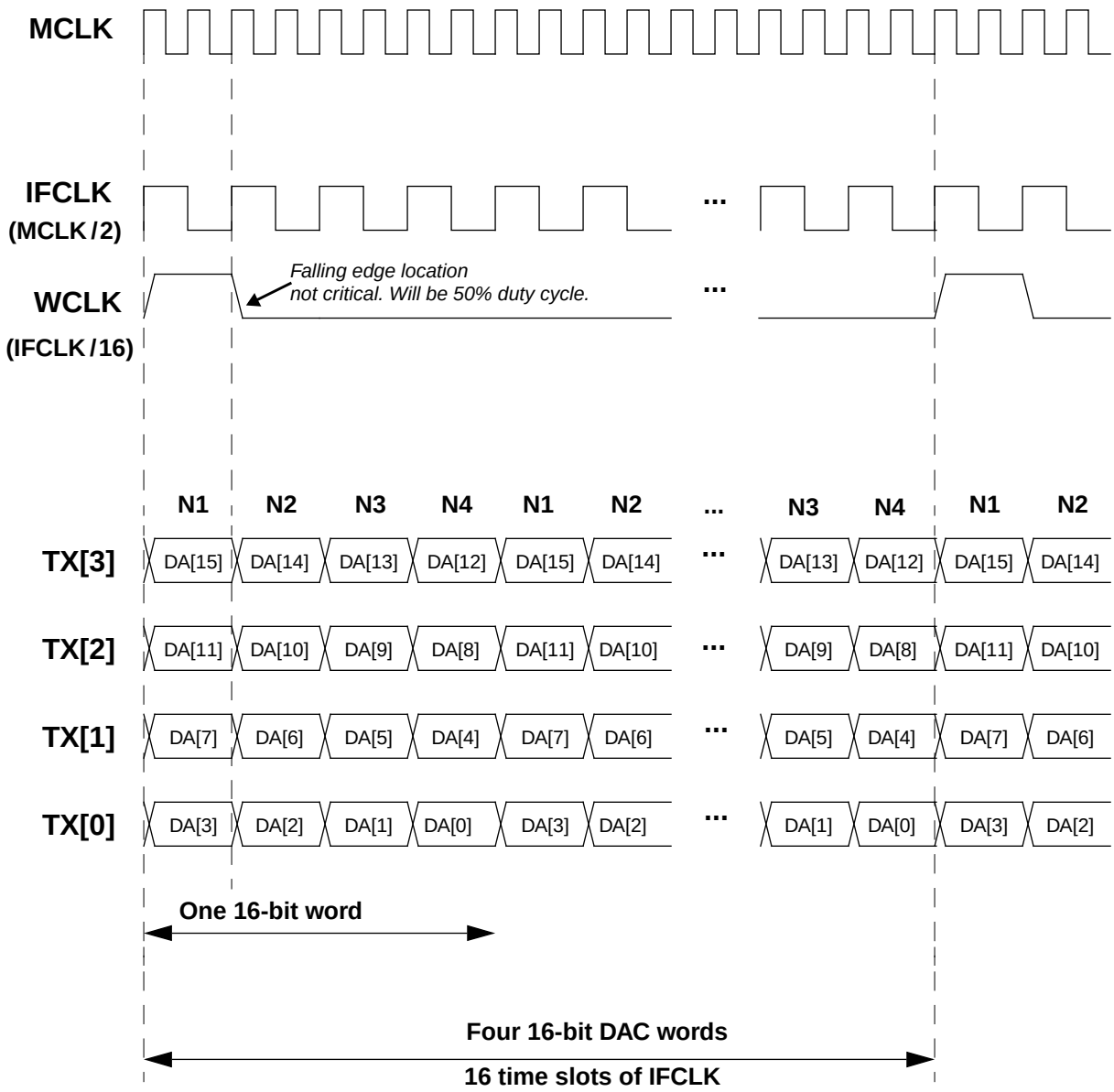


Fig. 1 Detailed data sequence for TX digital interface in nibble mode.

A timing diagram for the TX interface is shown below for 2-bit mode.

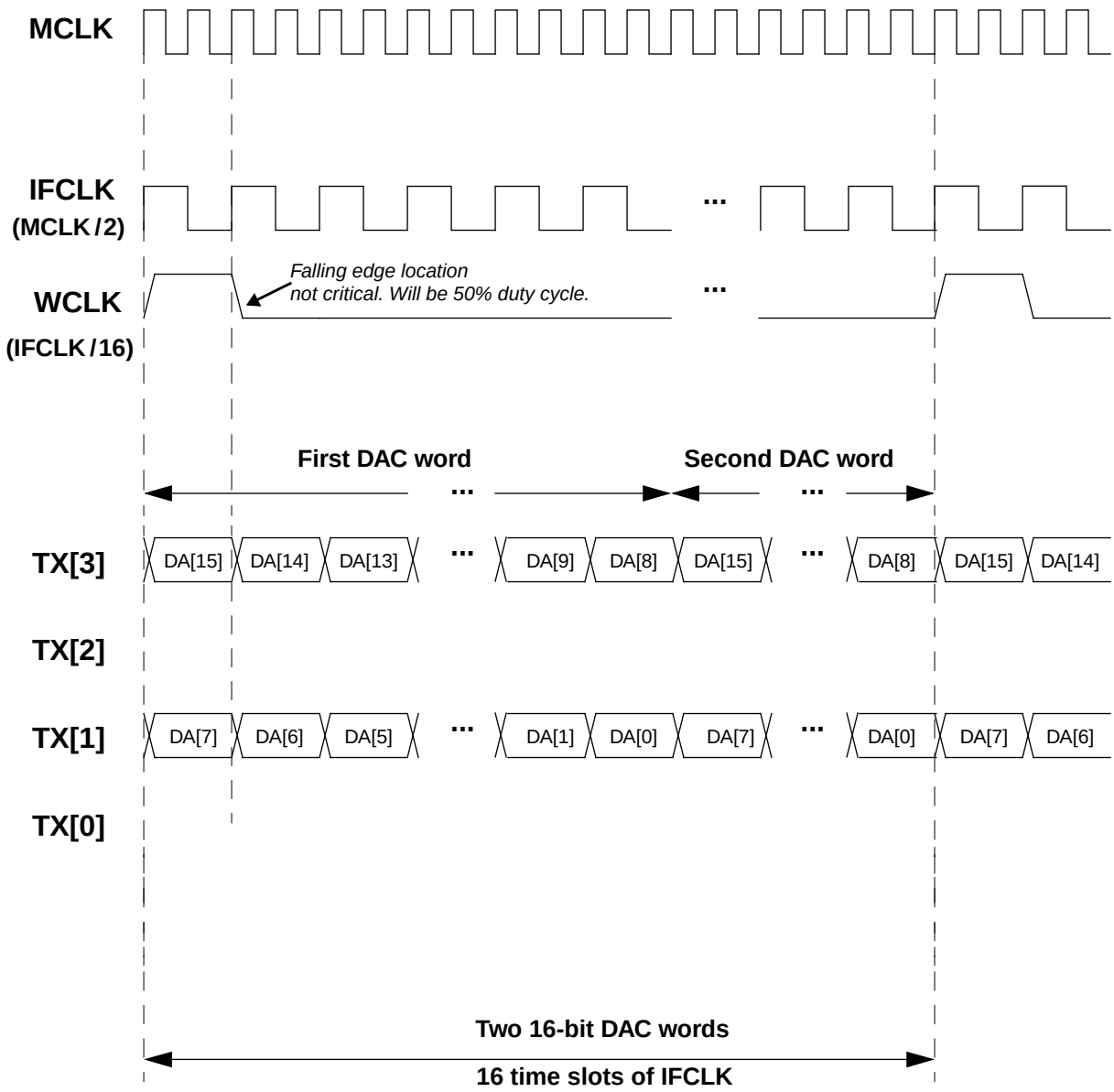


Fig. 2 Detailed data sequence for TX digital interface for 2-bit mode.

A timing diagram for the TX interface is shown below for 1-bit (serial) mode.

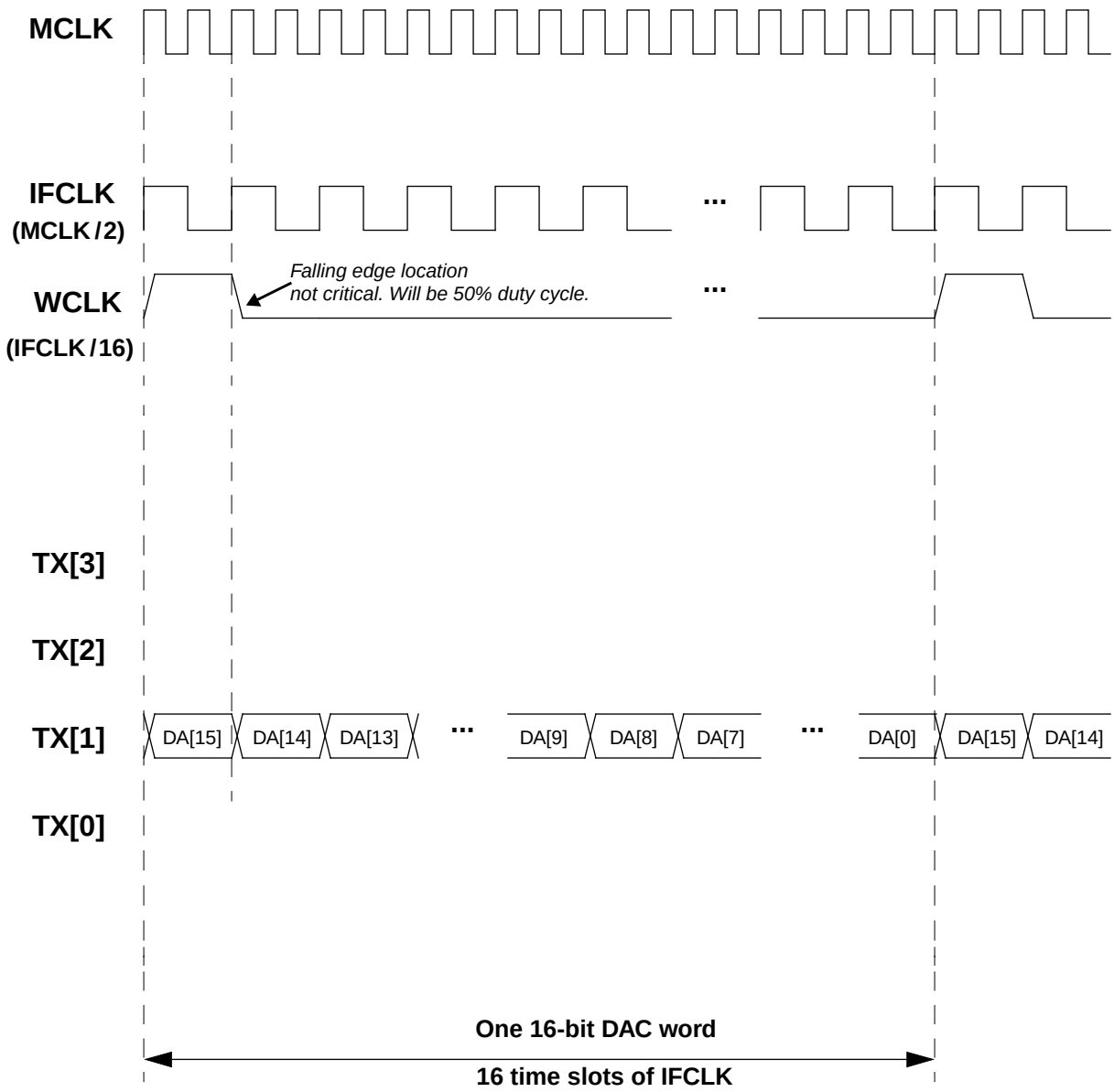


Fig. 3 Detailed data sequence for TX digital interface for 1-bit (serial) mode.

A timing diagram for the RX interface is shown below for 4-bit (nibble) mode.

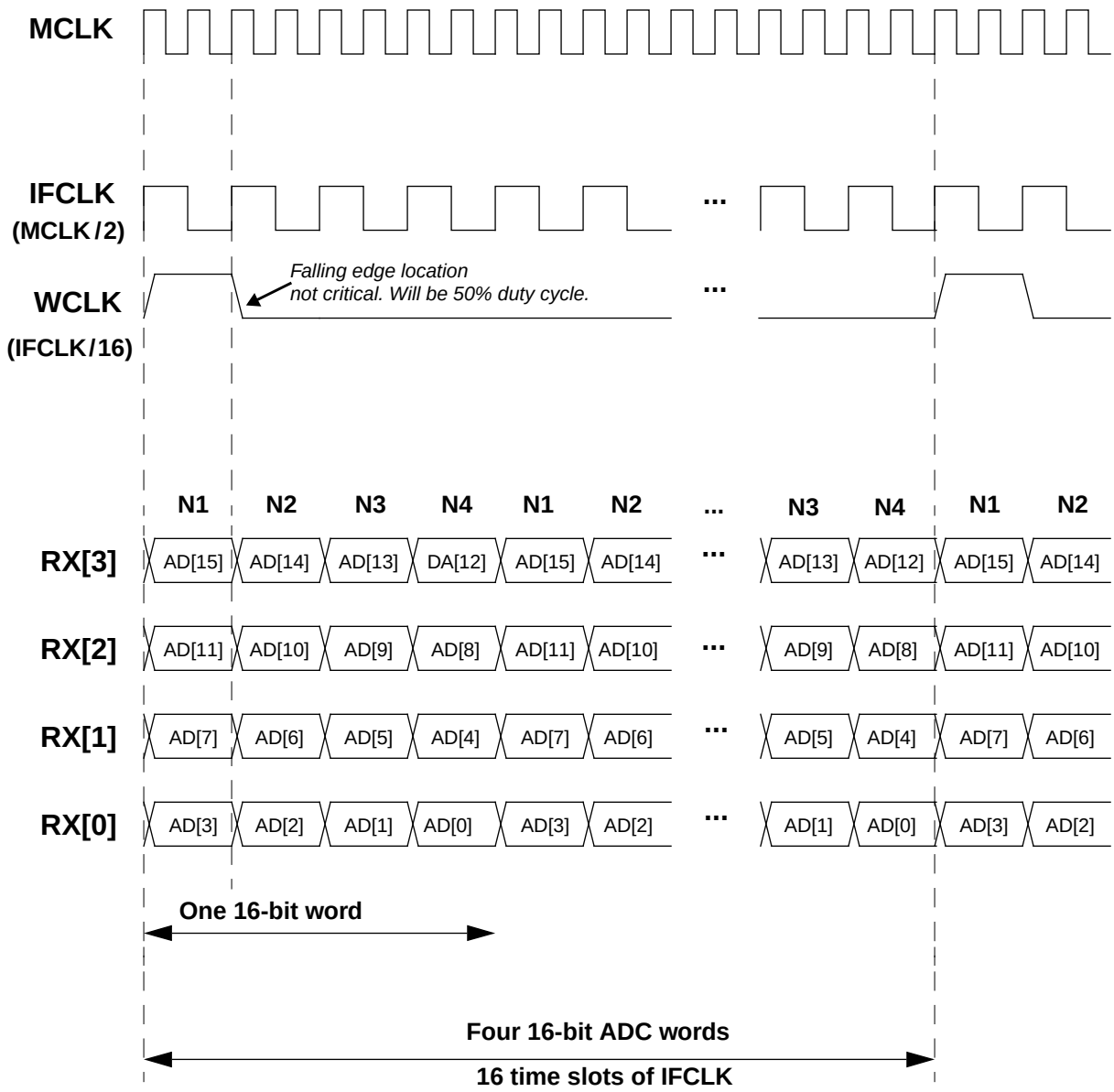


Fig. 4 Detailed data sequence for RX digital interface for nibble mode.

A timing diagram for the RX interface is shown below for 2-bit mode.

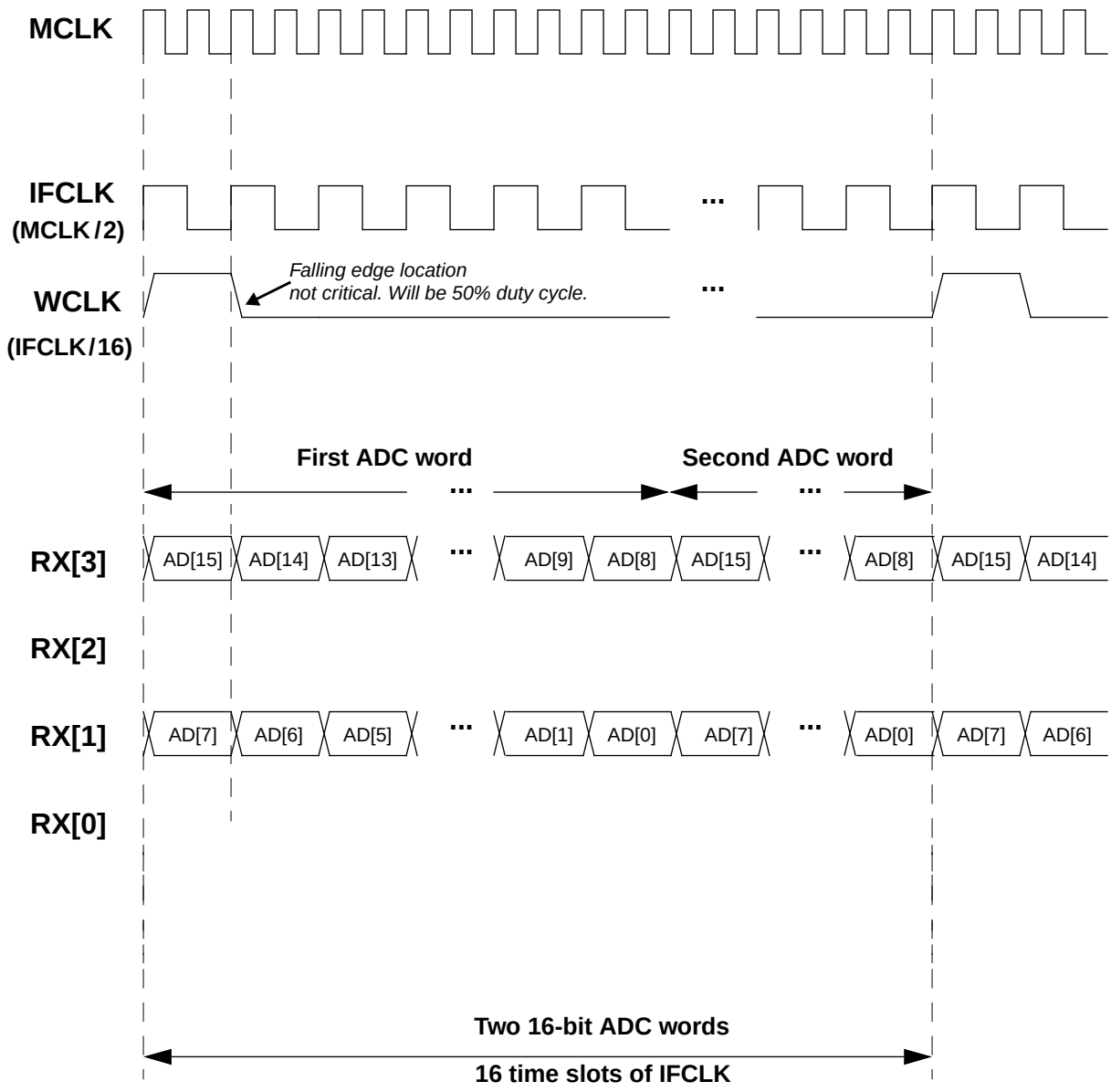


Fig. 5 Detailed data sequence for RX digital interface for 2-bit mode.

A timing diagram for the RX interface is shown below for 1-bit (serial) mode.

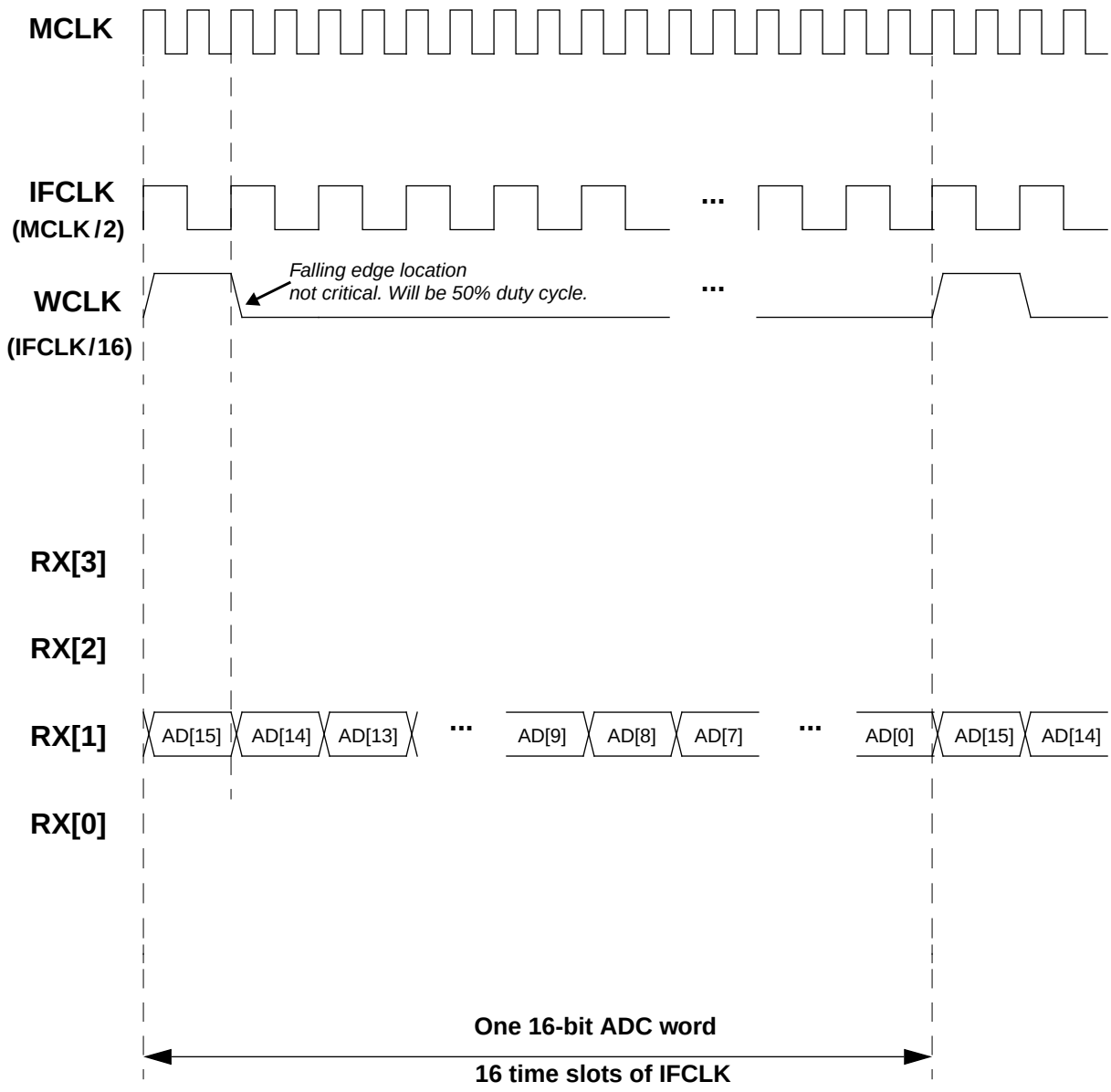


Fig. 6 Detailed data sequence for RX digital interface for 1-bit (serial) mode.

As an example, a timing diagram for a possible interface configuration is shown below for full-rate ADSL employing a 4.4 MHz rate in the RX path, and a 1.1 MHz rate in the TX path. The total number of data pins required is 5 (4 RX data and 1 TX data).

Full-rate ADSL: MCLK = 35.328 MHz, IFCLK = 17.664 MHz, WCLK = 1.104 MHz, outgoing RX data rate = 4.416 MHz, incoming TX data rate = 1.104 MHz

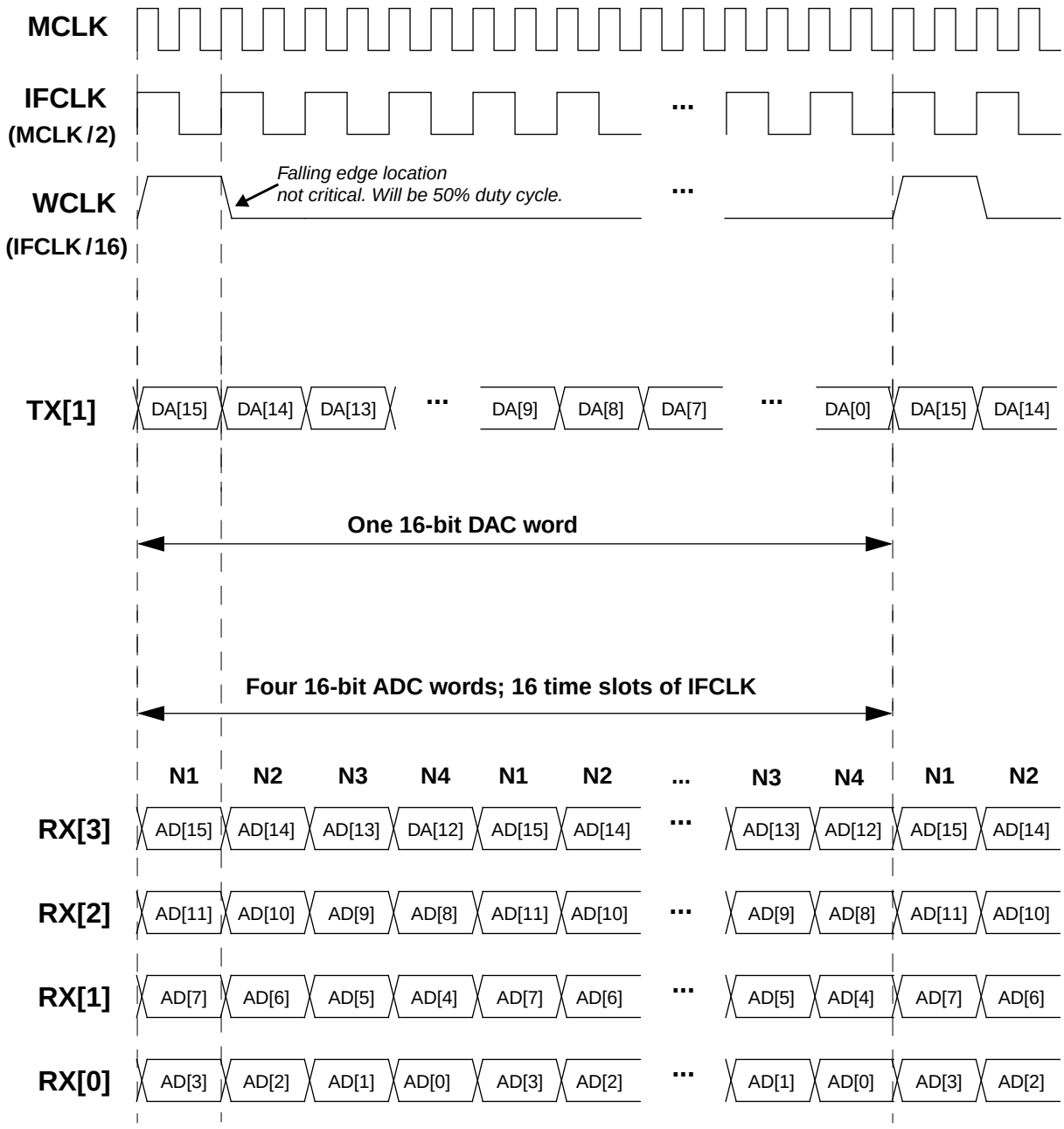


Fig. 7 Detailed data sequence for possible TX/RX digital interface for full-rate ADSL.

A timing diagram for a possible interface is shown below for *G.lite* ADSL. The total number of data pins required is 3 (2 RX data and 1 TX data).

***G.lite* ADSL: MCLK = 35.328 MHz, IFCLK = 17.664 MHz, WCLK = 1.104 MHz, outgoing RX data rate = 2.208 MHz, incoming TX data rate = 1.104 MHz**

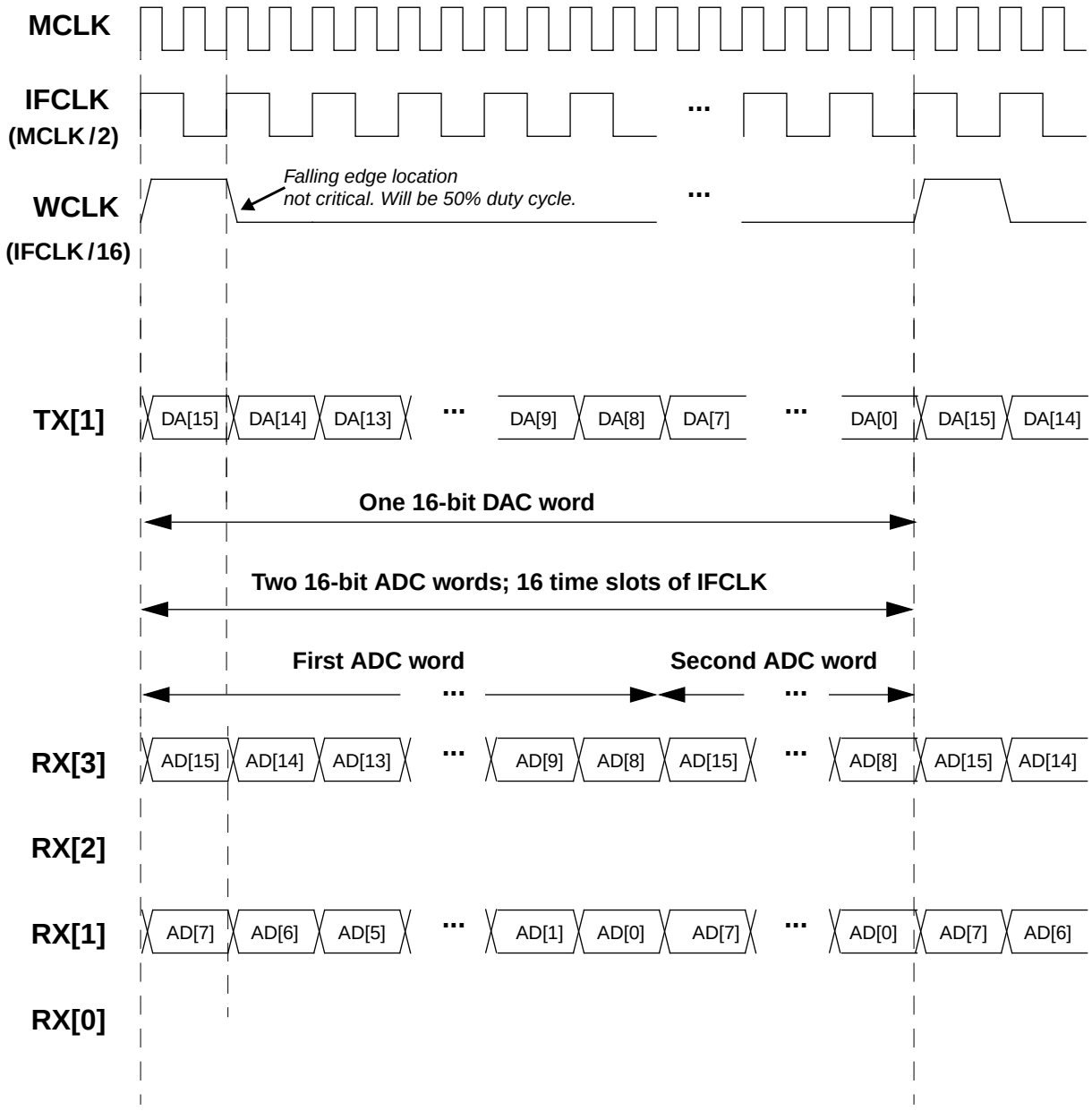
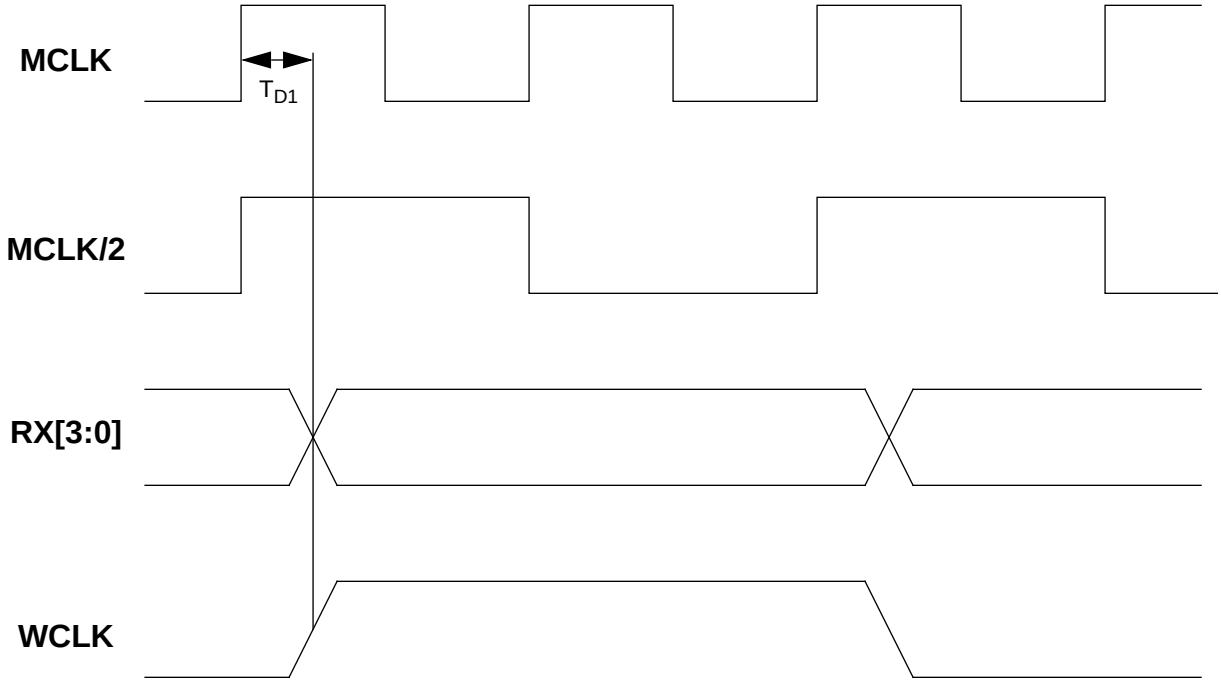


Fig. 8 Detailed data sequence for possible TX/RX digital interface for *G.lite.*

The following are the detailed timing specifications for the various digital interfaces.

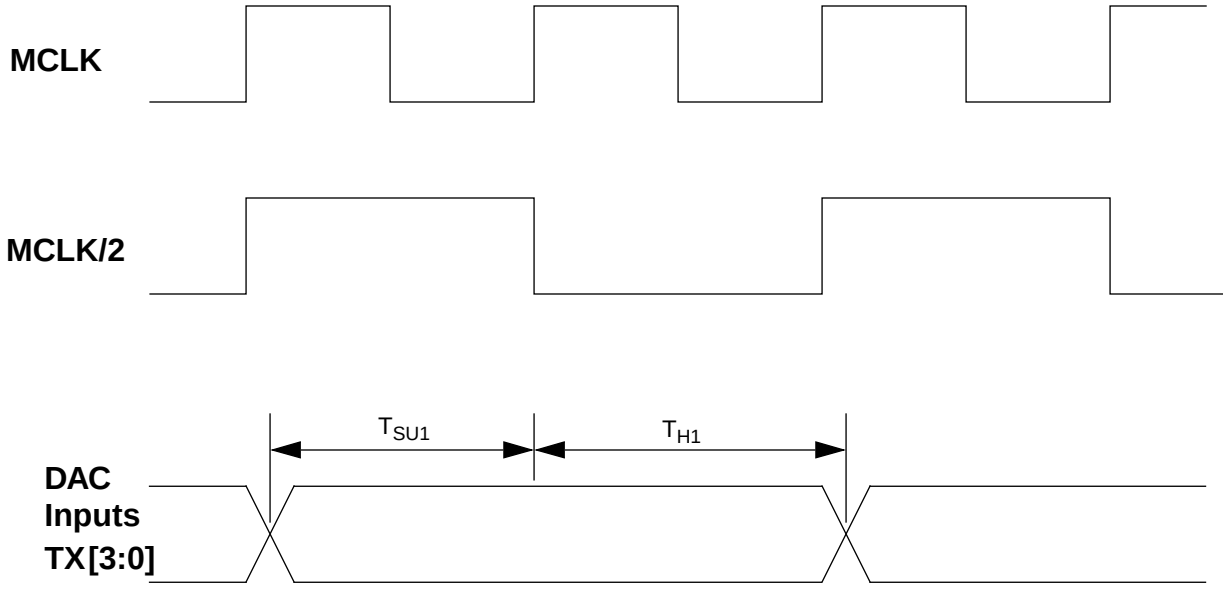
RX Output Timing



Parameter	Symbol	Min	Typ	Max	Units
MCLK high to Data Valid	T_{D1}			15	ns

Fig. 9 RX Output timing. Conditions: load capacitance = 20 pF, VOH = 3.3 V

TX Input Timing



Parameter	Symbol	Min	Typ	Max	Units
TX inputs setup time	T_{SU1}	7	10	14	ns
TX inputs hold time	T_{H1}	7	10	14	ns

Fig. 10 TX input timing. Conditions: load capacitance = 20 pF, VOH = 3.3 V

The EC[3:0] inputs have the same timing specifications.

4.2 Serial Port Interface

4.2.0 Introduction

The serial port interface controls the read/write to the registers on the chip. The interface consists of an active-low enable input pin (S_EN), a serial clock input pin (S_CLK), a data input pin (S_DIN) and a data output pin (S_DOUT). The timing diagram of the operation of the serial port is shown in Fig. 11. After S_EN is asserted, chip-selects (CS1, CS0), serial port register address (A4-A0) and read/write control bit ($\overline{R}$/W) are serially clocked in at the rising edge of S_CLK. For a write operation ($\overline{R}$/W=1), the addressed register is updated upon receiving the 16-bit write data (D15-D0). For a read operation ($\overline{R}$/W=0), the 16-bit contents of the addressed register is sequentially shifted out at the S_DOUT pin at the falling edge of S_CLK. As shown in Fig. 11, S_DOUT is driven only when data are being read; otherwise, it is tristated. **Note: in this implementation, chip selects (CS1, CS0) are tied to GND internally on chip, and so should always be LOW in real usage. Apart from the CS1, CS0 issue, this interface is identical to that present on the existing DPS8000 and DPS8001 family of products.**

4.2.1 Serial Port Timing

The timing diagram for the serial port is shown in Fig. 11.

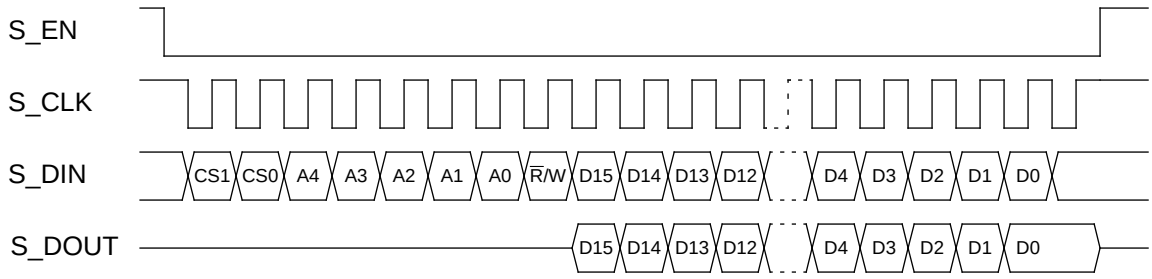
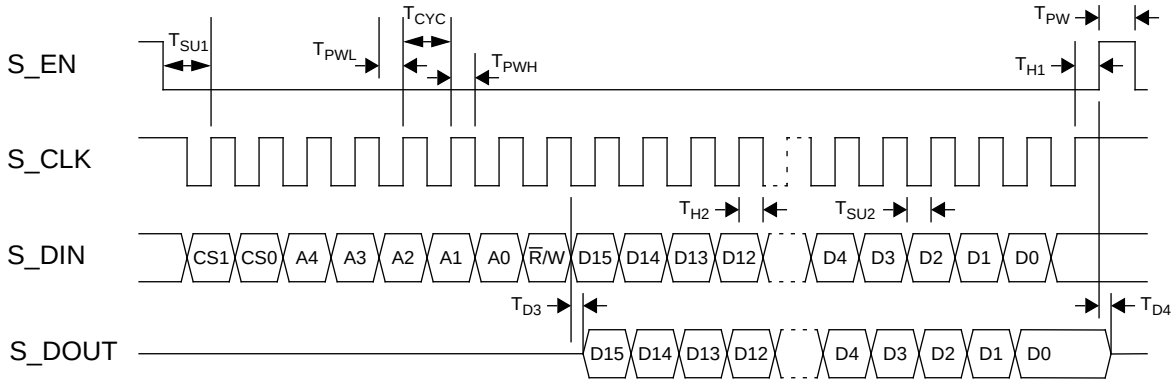


Fig. 11 Timing diagram for the serial port

Detailed information on setup/hold times is given below.

4.2.2 Serial Port



Parameter	Symbol	Min	Typ	Max	Units
S_CLK clock period	T_{CYC}	100	125		ns
S_CLK high time	T_{PWH}	50			ns
S_CLK low time	T_{PWL}	50			ns
S_EN low to S_CLK high	T_{SU1}	30			ns
S_CLK high to S_EN high	T_{H1}	15			ns
S_EN inactive pulse width	T_{PW}	100			ns
S_DIN setup time	T_{SU2}	15			ns
S_DIN hold time	T_{H2}	15			ns
S_CLK low to S_DOUT delay	T_{D3}			30[a]	ns
S_EN inactive to S_DOUT HiZ	T_{D4}			30	ns

a. Conditions: load capacitance = 30 pF, VOH = 5.0 V