DSTINI1
TINI Verification Module

PRELIMINARY

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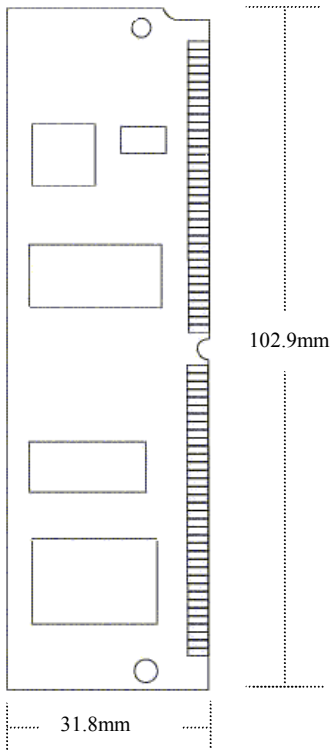
FEATURES

- TINI Chipset assembled on a standard 72 pin SIMM
- Hosts the TINI runtime environment in validated hardware design
- The extensive I/O capabilities of the DS80C390 microcontroller are exposed through Java™ APIs
  - Dual serial ports[1]
  - Dual 1-Wire net interfaces
  - Dual CAN (Controller Area Network) controllers
  - 2-wire synchronous serial bus
  - General-purpose digital I/O
  - Easy system expansion using a parallel bus interface
- Direct connection to the 10 or 10/100Base-T Ethernet network
- Real Time clock for time stamping
- Flash ROM for storage and execution of runtime environment
- 512K/1MByte nonvolatile SRAM provides fast, unlimited write operations and persistent data storage
- Level translator provides RS232 voltages
- Wide operating temperature range, -20°C to +70°C
- Requires only a single +5V power supply

PIN ASSIGNMENT



72 pin SIMM

[1] The runtime environment supports up to 4 serial ports using an external UART.

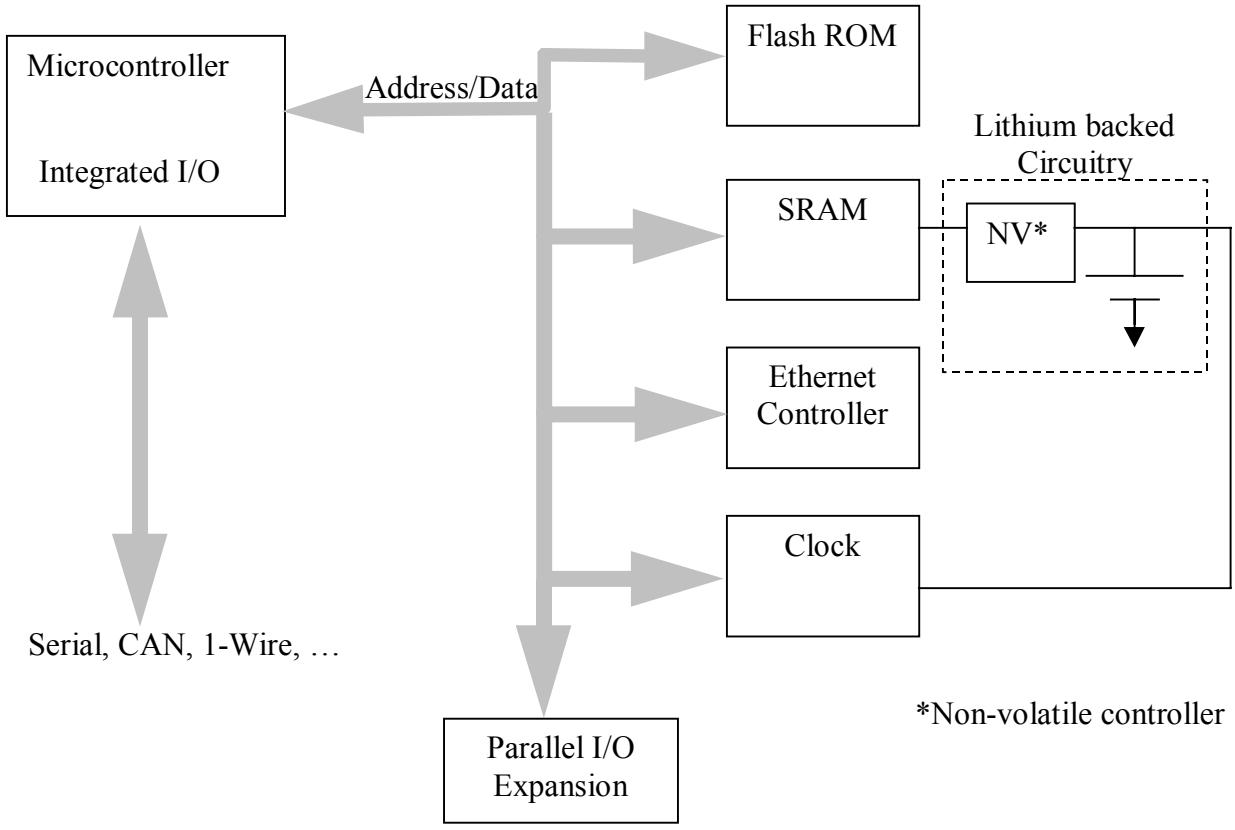
DSTINI1 Description

The DSTINI1 module is designed for use in intelligent networked devices including IP sensors, industrial control, home automation, and remote metering. It provides a proven and commercially available reference implementation for the TINI chipset. The DSTINI1 serves the following purposes:

- **Reference implementation** - The details of the verification module design are available at http://www.ibutton.com/TINI. Hardware developers are free to use information gleaned from the DSTINI1 when designing the chipset into their own TINI-based systems.
- **Development tool** – The DSTINI1 provides easy access to much of the platform's I/O capability allowing designers to quickly interface custom external hardware and develop their applications.
- **System Component** – For embedded network devices where the SIMM form factor is desirable, the DSTINI1 is available to meet high volume production requirements.

The TINI model 390 chipset is defined as the chips on the DSTINI1. All the chips are standard catalog items so that targeted designs can be built up from the core microcontroller, flash ROM and static RAM. The DSTINI1 provides a 10BASE-T Ethernet controller, Real Time clock and a RAM non-volatizer. The Ethernet controller and Real Time clock are interfaced to the microcontroller's parallel bus as shown in the following block diagram.

DSTINI1 Block Diagram Figure 1

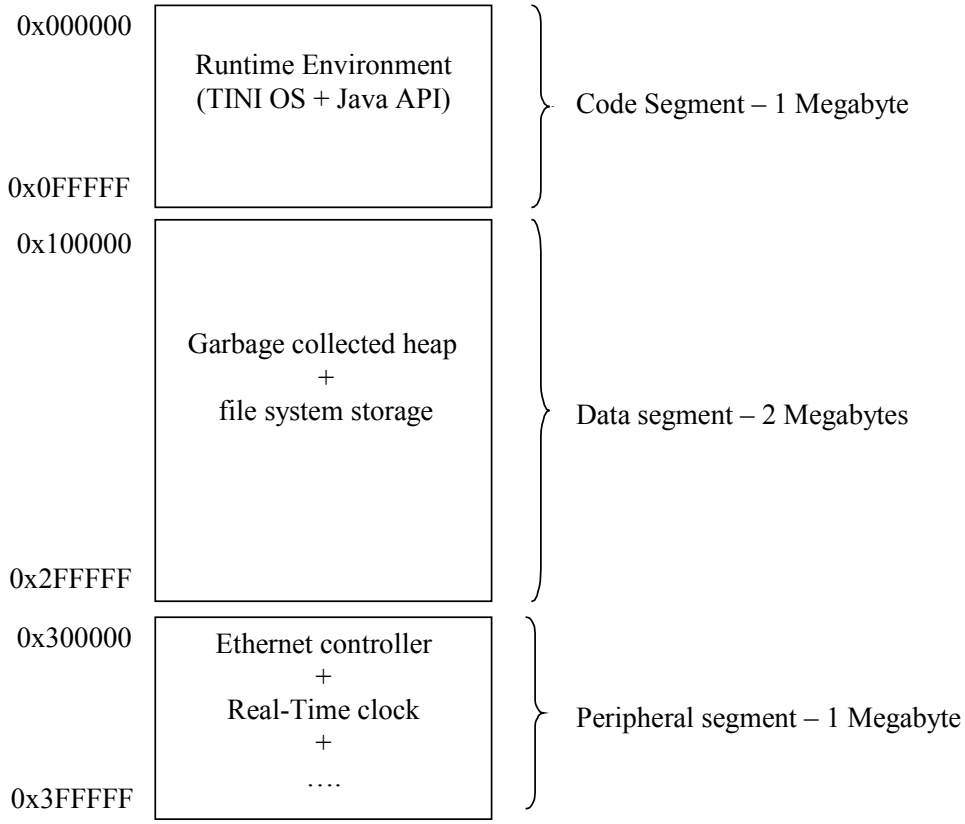


Peripheral devices, other than memory, can also be interfaced directly to the microcontroller's address and data buses (labeled Parallel I/O expansion in figure 1). The DSTINI1 maps the Ethernet controller in the memory range of [0x300000 –0x37FFFF] and it maps the Real Time clock at address 0x310000. Additional devices added to the system must avoid these address ranges.

MEMORY DESCRIPTION

Figure 2 illustrates the memory map of the DSTINI1. There are three memory segments, code, data and peripheral. Figure 2 illustrates the maximum segment sizes supported by the DSTINI1. So, for example, even though the DSTINI1 contains only 512 kilobytes of flash ROM, the starting address of the data segment remains 0x100000. The starting address of the segments is always constant, while the ending addresses may vary according to memory size. The TINI platform's minimum memory requirement for both the code and data segments is 512 kilobytes. The code and data segments are occupied exclusively by memory chips and the peripheral segment is occupied by other types of hardware components such as the Ethernet controller and real time clock.

MEMORY MAP Figure 2



The DSTINI1 consumes the following address ranges:

1. TINI OS and API - [0x000000 – 0x07FFFF]
2. Heap and file system storage – [0x180000 – 0x280000]
3. Ethernet controller – [0x300000 – 0x37FFFF]
4. Real Time clock – 0x310000

System designers must avoid the Ethernet controller and Real Time clock when interfacing with other devices. The rest of this address range is available for adding other peripheral devices.

There is also a separate 4 megabyte peripheral area, known as peripheral chip enable (PCE) space, that can be used to interface large (up to four 1 megabyte) external memory chips or other hardware devices

directly to the microcontroller's address and data buses. However most hardware is mapped in the peripheral segment because the microcontroller can access it more efficiently. The microcontroller uses 4 pins to enable access to the PCE address space ($\overline{PCE0} - \overline{PCE3}$). If no devices are mapped into this space the microcontroller pins can be used as general-purpose port pins. The system designer is free to use the peripheral area either for interfacing hardware directly to the microcontroller's address and data buses or general purpose TTL I/O, but not both.

STRETCH MEMORY CYCLES

The DSTINI1 allows user application software to select the number of machine cycles it takes to execute a bus read or write (MOVX) instruction, allowing access to both fast and slow off-chip data memory and/or peripherals without glue logic. High-speed systems often include memory-mapped peripherals such as LCDs or UARTs with slow access times, so it may not be necessary or desirable to access external devices at full speed.

External MOVX timing is governed by the selection of 0 to 7 Stretch cycles, controlled by the MD2-MD0 SFR bits in the Clock Control Register (CKCON.2-0). A Stretch of zero will result in a 2 machine cycle MOVX instruction. A Stretch of seven will result in a MOVX of twelve machine cycles. Software can dynamically change the stretch value depending on the particular memory or peripheral being accessed[2].

Stretch cycle settings affect external MOVX timing in three gradations. Changing the Stretch value from 0 to 1 adds an additional clock cycle each to the data setup and hold times. When a Stretch value of 4 or above is selected, the interface timing changes dramatically to allow for very slow peripherals. The address is held on the bus for one additional machine cycle increasing the address hold time by this amount. Next, The $\overline{WR}$ and $\overline{RD}$ signals are then lengthened by a machine cycle. Finally, during a MOVX write the data is held on the bus for one additional machine cycle, thereby increasing the data hold time by this amount. For every Stretch value greater than 4, the setup and hold times remain constant, and only the width of the read or write signal is increased. These three gradations are reflected in the AC Electrical characteristics, where only three timing diagrams represent the eight MOVX timing specifications.

The specific timing of MOVX instructions as a function of stretch settings is provided in the Electrical Specifications section of this data sheet, also refer to the DS80C390 datasheet. As an example, Table 1 shows the read and write strobe widths corresponding to each stretch value.

DATA MEMORY CYCLE STRETCH VALUES Table 1

MD2	MD1	MD0	Stretch Cycle Count	MOVX Machine Cycles	$\overline{RD}$ and $\overline{WR}$, Pulse Width (in oscillator clocks)
0	0	0	0*	2	1 t_{CLCL}
0	0	1	1*	3	2 t_{CLCL}
0	1	0	2	4	4 t_{CLCL}
0	1	1	3	5	6 t_{CLCL}
1	0	0	4	9	8 t_{CLCL}
1	0	1	5	10	10 t_{CLCL}
1	1	0	6	11	12 t_{CLCL}
1	1	1	7	12	14 t_{CLCL}

[2] See the runtime environment documentation of the DataPort class for details.

SERIAL BOOTSTRAP LOADER

The serial loader is the easiest and most reliable way to load the DSTINI1 runtime environment into the flash ROM. Communication can be performed over a standard asynchronous serial communications port. A typical application would use a simple RS232C serial interface on a host PC or workstation to program the DSTINI1 as a final production procedure. The loader will autobaud to any of the following bit rates: 12800, 14400, 16457, 19200, 23040, 28800, 38400, 57600, and 115200 bps.

Following is a partial list of the command set supported by the serial bootstrap loader.

Command	Function
B	Selects a memory bank.
C	Calculates the CRC-16 of the specified range.
D	Dumps a specified bank of memory.
E	Exit to bank 1 and begin execution.
F	Fill memory in the selected bank.
H	Prints help.
L	Load into the selected bank.
M	Copies the loader to the selected bank.
S	Sets comm. Speed to ½ of present.
T	Invoke tests.
V	Verify hex against memory.
Z	Erases a sector of flash.

PIN DESCRIPTION

PIN	SIGNAL NAME	DESCRIPTION
67, 68, 69, 70	Vcc	+5V DC +/- 5% @ 250mA max[3]
3 - 7	GND	Digital Circuit Ground.
2	IN1	TTL input– dual-purpose input pin. Can be used as CTS for RTS/CTS flow control or as a general-purpose data input pin.
59	IN2	TTL input – Can be used as general-purpose input port pin.
1	IN3	TTL input – dual-purpose input pin. Can be used as DCD for RTS/CTS flow control or as a general-purpose data input pin.
8	OWIO	1-Wire Input/Output Pin: 1-Wire bus with slew-rate-controlled pull-down, active pull-up, ability to switch in V_{PP} to program EPROM, and ability to switch in V_{DD} through a low-impedance path to program EEPROM or to perform a temperature conversion.
9	V_{PP}	+12V supply input for EPROM programming[1].
10	CTX	CAN bus TX line or bi-directional port pin
11	CRX	CAN bus RX line or bi-directional port pin
12	$\overline{CE0}$	CPU chip enable 0[2]
14	TX1	Serial Port 1 output TTL
15	XRX1	Serial Port 1 input TTL
16	$\overline{RD}$	CPU read strobe[7]

17	INTOW	Internal 1-Wire bus[4]
18	SMCRST	Peripheral reset from CPU
19	TX232	Serial Port 0 output
20	RX232	Serial Port 0 input
21	TX	Serial Port 0 output TTL
22	XRX0	Serial Port 0 input TTL
23	$\overline{\text{EXTINT}}$	CPU interrupt input
24	CPURST	CPU reset input[5]
25	DTR232	RS232 CPU reset input[6]
26	EN2480	On-board DS2480 enable
27 28 29 30	$\overline{\text{PCE3}}$ $\overline{\text{PCE2}}$ $\overline{\text{PCE1}}$ $\overline{\text{PCE0}}$	Peripheral chip enables from CPU[7]
31	$\overline{\text{CE3}}$	Chip Enable 3 from CPU[7]
32	$\overline{\text{PSEN}}$	Program Store enable from CPU[7]
45	$\overline{\text{RCE0}}$	CE0 return to on-board Flash ROM[2]
58	$\overline{\text{WR}}$	CPU Write Strobe[7]
63 64	ETH3 ETH6	10Base-T differential inputs.
65 66	ETH2 ETH1	10Base-T differential outputs.
71	OUT1	TTL output – dual-purpose output pin. Can be used as RTS for RTS/CTS flow control or as a general-purpose data output pin.
72	OUT2	TTL output – dual-purpose output pin. Can be used as DTR for RTS/CTS flow control or as a general-purpose data output pin.
33 - 36 37 – 44 54 - 57 60 - 62 13	A7 – A4 A8 – A15 A0 – A3 A16 - A18 A19	Address lines[7].
46 - 53	D7 - D0	Data lines[7]

NOTES FOR PIN DESCRIPTION:

1. Pin 9 (V_{PP}) may be connected to +12V DC to allow EPROM programming with the on-board DS2480. If pin 9 (V_{PP}) is not used in this manner, it must be connected to V_{CC}.
2. To execute from the on-board Flash ROM, connect $\overline{\text{CE0}}$ (Pin 12) to $\overline{\text{RCE0}}$ (Pin 45). If an external boot-up memory is provided, $\overline{\text{RCE0}}$ must be pulled high (V_{CC}) to disable the on-board Flash ROM or data bus interference could occur. Logic in the $\overline{\text{CE0}}$ to $\overline{\text{RCE0}}$ path must take care to present minimal delay (<6 ns) to the $\overline{\text{CE0}}$ signal.
3. TINI board power consumption is rated at no more than 250 mA.
4. The internal 1-Wire bus (INTOW) is a micro-controller port pin that drives the CPU status LED and links to the board's 1-Wire EPROM memory chip that contains the DSTINI1's Ethernet MAC address. Other 1-Wire devices may be connected to this bus in the future to convey configuration

data to the DSTINI. If this bus is shorted to ground (low) during system boot-up, a Master Clear will be invoked. This forces the contents of the SRAM to be reinitialized.

5. CPURST must be taken high (V_{CC}) and then released to cause a reset of the DSTINI1. An active state on the DTR232 (pin 25) will also take this line high. This line is pulled down through a 22kΩ pull-down on-board.
6. The RS232 level DTR control line is used to invoke a DSTINI1 reset when asserted. This is to facilitate loaders and diagnostic equipment that must invoke a reset of the board to gain control of the system. This line is pulled to –8 V via 22K ohms and has a .01 µF capacitor filter to prevent cross talk on an open DTR conductor from causing spurious resets of the DSTINI if this function is not used.
7. Address bus, data bus and strobe lines are subject to strict loading limitations. Exceeding these limits can cause erratic system operation with on-board as well as off-board resources. Be sure to buffer any signals that will be heavily loaded off-board. Always adhere to the design specifications to assure reliable system operation.

ABSOLUTE MAXIMUM RATINGS[1]

Voltage on Any Pin Relative to Ground	-0.3V to V_{CC}+0.3V
Except for the following pins:	
RX232	±30 V
ETH3, ETH6	+125 V
ETH2, ETH1	+125 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +85°C
Soldering Temperature	260°C for 10 seconds

[1] This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-20°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	

DC ELECTRICAL CHARACTERISTICS

(-20°C to 70°C; V_{CC} = 4.75 to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.75		5.25	V	
Output Low Voltage @I_{OL}=1.7mA	V_{OL}			0.4	V	
Output High Voltage @-680µA	V_{OH}	2.4			V	

Input Leakage Current $0.45 < V_{IN} < V_{CC}$	I_{IL}			320	µA	
Reset Trip Point	V_{RST}	4.50		<4.75	V	
Supply Current Active Mode	I_{CC}		250		mA	
Output Low Voltage for Port 3, 5 @I_{OL} = 1.6mA	V_{OL1}			0.45	V	
Output Low Voltage for Port 3, 5 @I_{OL} = 3.2mA	V_{OL2}			0.45	V	
Output High Voltage for Port 3, 5 @ I_{OH}=-50µA	V_{OH1}	2.4			V	
Output High Voltage for Port 3, 5 @ I_{OH}=-1.5mA	V_{OH2}	2.4			V	
Logic 1 to 0 Transition Current for Port 3,5	I_L	-300		300	µA	
Input Current for IN1, IN2, IN3	I_{IH}		+75	+150	µA	
Output Low Voltage for OUT1, OUT2 @ I_{OL}=4mA	V_{OL3}			0.4	V	
Output High Voltage for OUT1, OUT2 @I_{OH}=-2mA	V_{OH3}	2.4			V	
Output Leakage Current for OUT1, OUT2 $0 < V_{IN} < V_{CC}$	I_{OL3}	-10		10	µA	

AC ELECTRICAL CHARACTERISTICS

(-20°C to 70°C; V_{CC} = 4.75 to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
External Oscillator Frequency	$1/t_{CLCL}$		18.432		MHz
$\overline{\text{PSEN}}$ Pulse Width	t_{PLPH}	0.5 t_{MCS} - 5			ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In	t_{PLIV}			0.5 t_{MCS} - 20	ns
Input Instruction Hold after $\overline{\text{PSEN}}$	t_{PXIX}	0			ns
Input Instruction Float after $\overline{\text{PSEN}}$	t_{PXIZ}			See MOVX Characteristics	ns
Capacitive load presented to external devices	C_L			90	pF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			Years	5

NOTES FOR AC ELECTRICAL CHARACTERISTICS

1. The value t_{MCS} is a function of the machine cycle clock in terms of the processor's input clock frequency. These relationships are described in the "Stretch Value Timing" table.
2. All signals characterized with load capacitance of 80 pF except $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ with 100 pF.
3. Specifications assume a 50% duty cycle for the oscillator.
4. t_{MCS} is defined as $2*t_{CLCL}$
5. The minimum expected data retention time in the absence of V_{CC} is 10 years at 25°C.

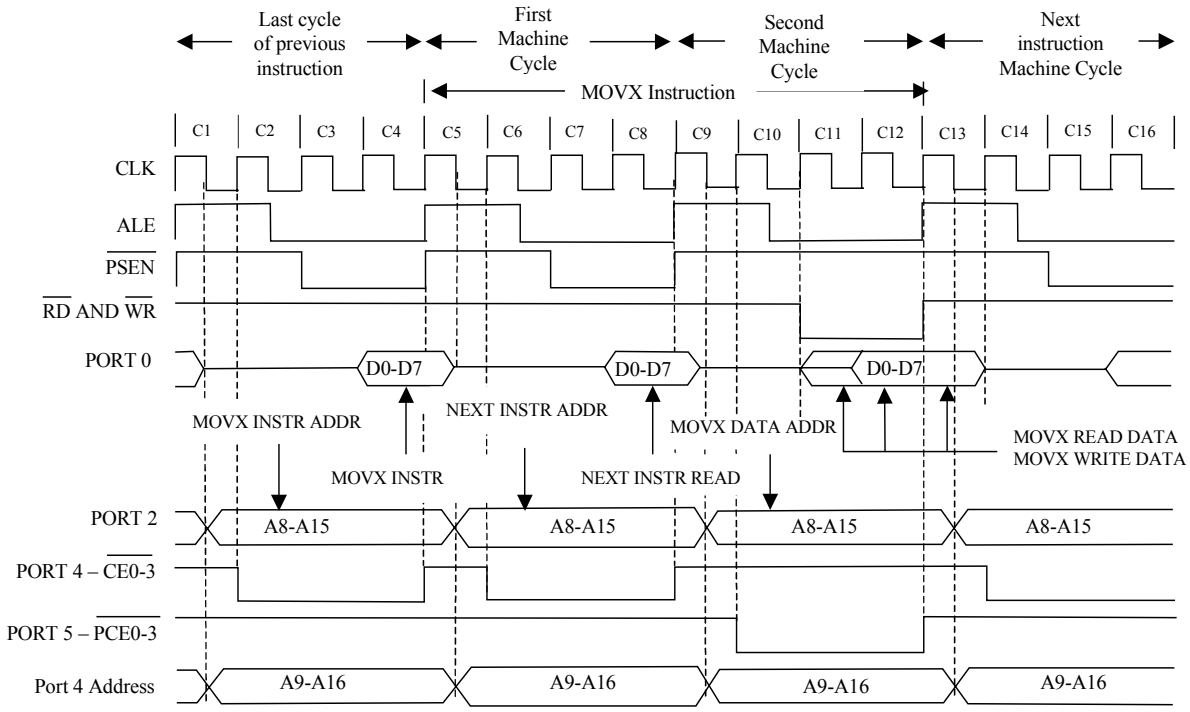
MOVX CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNITS	STRETCH VALUES C_{ST} (MD2:0)
Input Instruction Float after $\overline{PSEN}$	t_{PXIZ}	$0.5\ t_{MCS} - 5$ $0.75\ t_{MCS} - 5$ $2.75\ t_{MCS} - 10$		ns	$C_{ST} = 0$ $1 \le C_{ST} \le 3$ $4 \le C_{ST} \le 7$
$\overline{RD}$ Pulse Width	t_{RLRH}	$0.5\ t_{MCS} - 5$ $C_{ST}*t_{MCS}-10$		ns	$C_{ST} = 0$ $1 \le C_{ST} \le 7$
$\overline{WR}$ Pulse Width	t_{WLWH}	$0.5\ t_{MCS} - 5$ $C_{ST}*t_{MCS}-10$		ns	$C_{ST} = 0$ $1 \le C_{ST} \le 7$
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		0.5tMCS – 20 CST*tMCS-20	ns	$C_{ST} = 0$ $1 \le C_{ST} \le 7$
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		$0.5\ t_{MCS} - 5$ $0.75\ t_{MCS} - 5$ $1.75\ t_{MCS} - 5$	ns	$C_{ST} = 0$ $1 \le C_{ST} \le 3$ $4 \le C_{ST} \le 7$
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-5		ns	$C_{ST} = 0$ $1 \le C_{ST} \le 3$ $4 \le C_{ST} \le 7$
Data hold after $\overline{WR}$ high	t_{WHZX}	$0.25\ t_{MCS} - 5$ $0.5\ t_{MCS} - 5$ $1.5\ t_{MCS} - 10$		ns	$C_{ST} = 0$ $1 \le C_{ST} \le 3$ $4 \le C_{ST} \le 7$

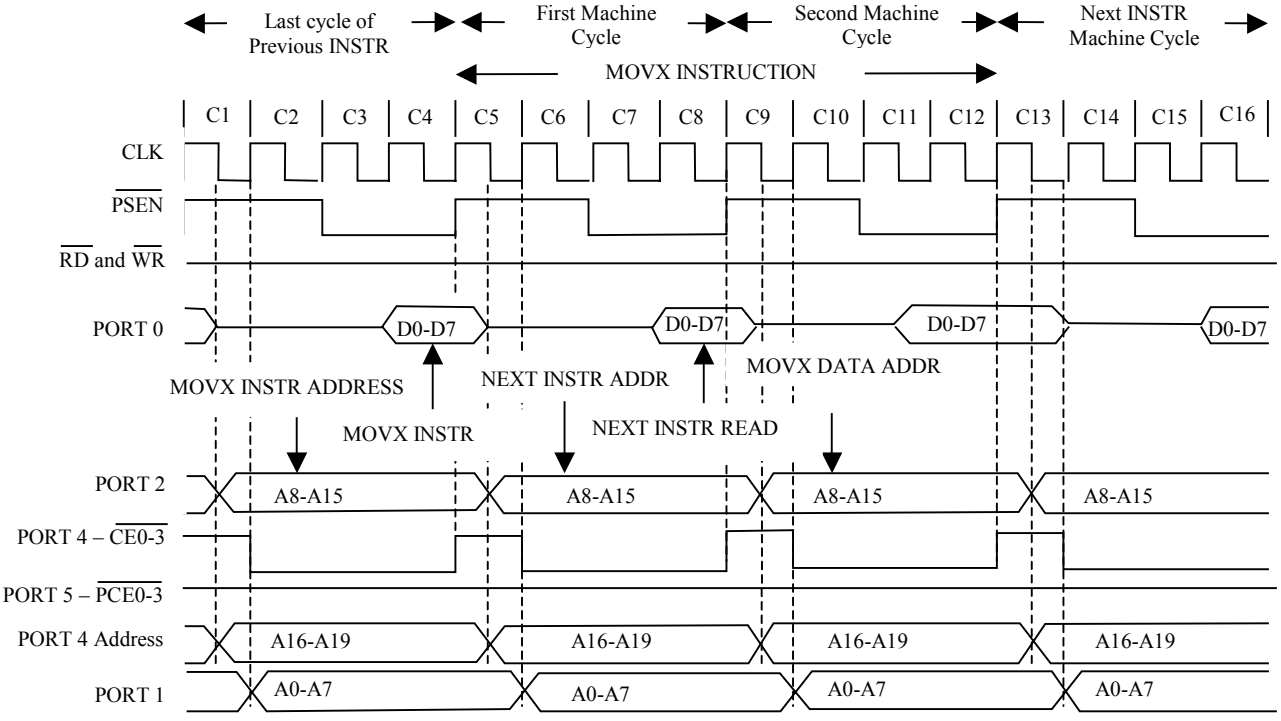
NOTES FOR MOVX CHARACTERISTICS

1. t_{MCS} is defined as $2*t_{CLCL}$

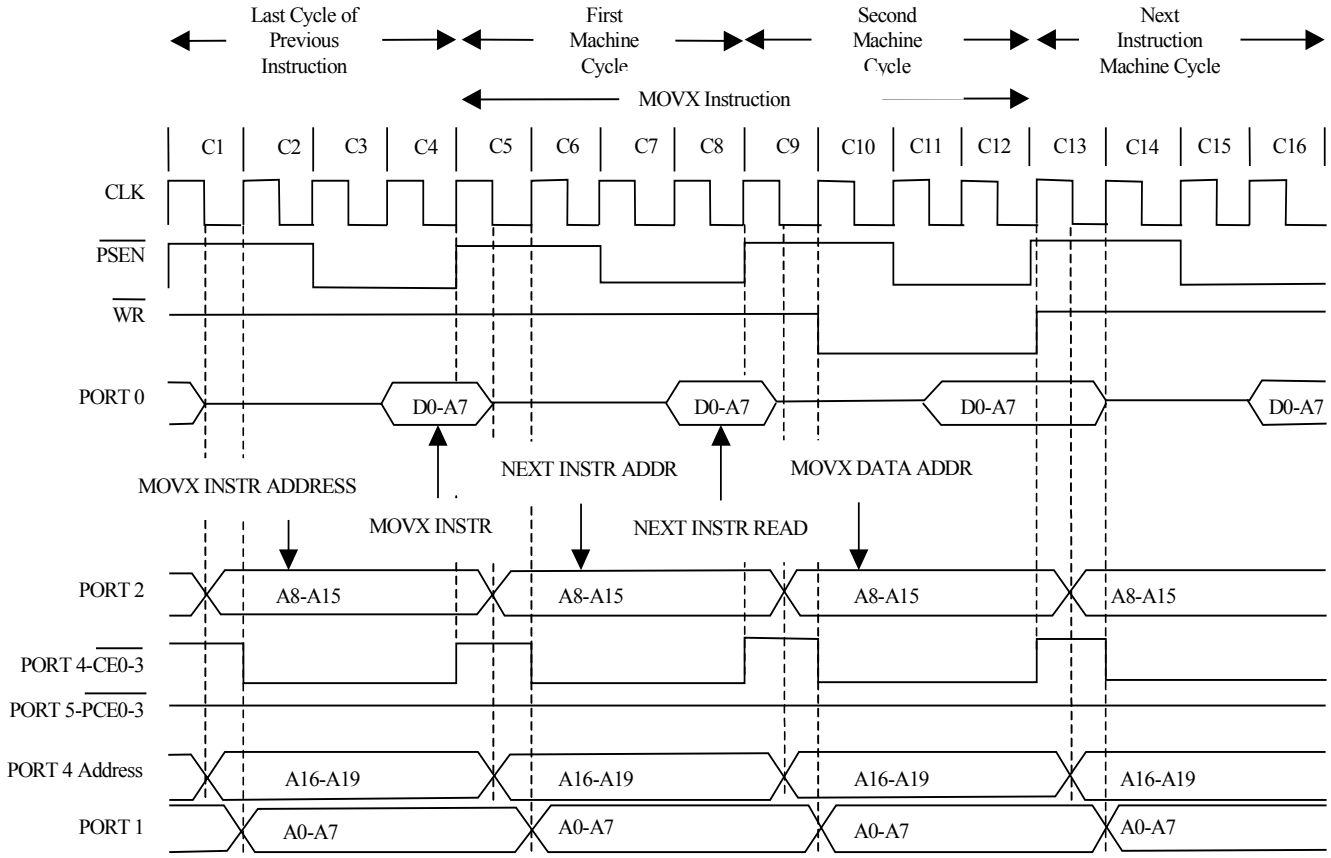
2 CYCLE DATA MEMORY $\overline{\text{PCE0-3}}$ READ OR WRITE



2 CYCLE DATA MEMORY $\overline{\text{CE0-3}}$ READ



2 CYCLE DATA MEMORY $\overline{\text{CE0-3}}$ WRITE



TYPICAL TEMPERATURE VERSUS LOAD CHARACTERISTICS

Number of Loads[1]	Minimum Temperature (ºC)	Maximum Temperature (ºC)
0	-20	70
1	-20	70
2	-20	70
3	-20	60
4	-20	55
5	-20	50

[1] A load is characterized as 7pF applied to the address, control and data lines of a DSTINI1-512.

HANDLING INSTRUCTIONS

Handle the DSTINI1 as if it were a PC style memory module. The DSTINI1 is designed to be robust, however Electrostatic Discharge (ESD) precautions should be observed when handling this module. As with any other electronic device with exposed circuitry, the DSTINI1 should be stored in an anti-static box. When inserting the DSTINI1 into a socket, verify that power is not present. VCC and GND connections should be checked before applying power. Also, verify that the input power is between 4.75 and 5.25 volts.

ORDERING INFORMATION

PART NUMBER	FLASH SIZE	RAM SIZE	CRYSTAL SPEED
DSTINI1-512	512 kbytes	512 kbytes	36.864 MHz[1]
DSTINI1-1MG	512 kbytes	1024 kbytes	36.864 MHz[1]

[1] The external crystal frequency is 18.432MHz, which is doubled on chip to 36.864MHz.