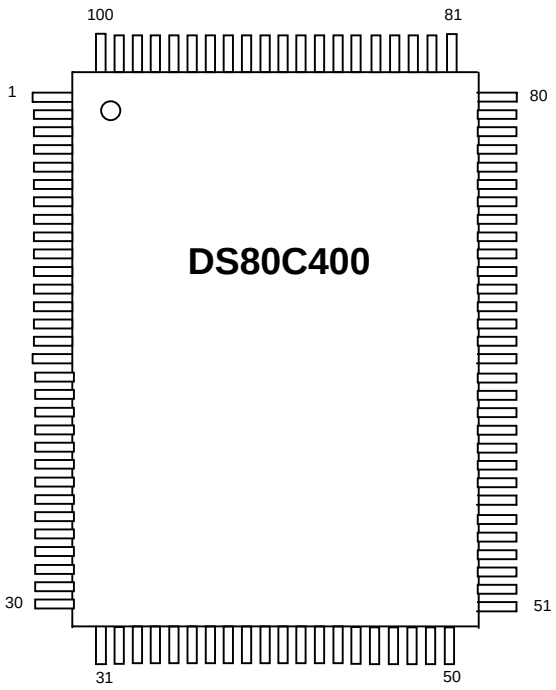
DALLAS SEMICONDUCTOR

DS80C400
Network Microcontroller

FEATURES

- **High-Performance Architecture**
  - Single 8051 instruction cycle in 80 ns
  - DC to 50 MHz clock rate
  - Flat 16 MB address space for high level language support
  - Four data pointers with auto-inc/dec accelerate data movement
  - 16/32-bit math accelerator
- **Multitiered Networking and I/O**
  - 10/100 Ethernet Media Access Controller
  - CAN 2.0B controller
  - 1-Wire net controller
  - Three full-duplex hardware serial ports
  - Up to eight bi-directional 8-bit ports (64 digital I/O pins)
- **Robust ROM Firmware**
  - Bootstrap loader supports cold start over serial or Ethernet using Magic Packet, BOOTP, and TFTP
  - Full, application-accessible TCP/IP network stack
  - Supports IPv4 and IPv6
  - Implements UDP, TCP, DHCP, ICMP, IGMP, and PPP
  - MAC address acquisition from IEEE-registered DS2502-E48
- **10/100 Ethernet MAC**
  - Flexible IEEE 802.3 MII (10/100 Mbps) and ENDEC (10 Mbps) interfaces allow selection of PHY
  - Low-power operation
  - Ultra low-power sleep mode with Magic Packet and wake-up frame detection
  - 8kB on-chip TX/RX packet data memory with Buffer Control Unit offloads CPU
  - Full- or half-duplex operation
  - Multicast/Broadcast address filtering with VLAN support

PIN ASSIGNMENT



100-PIN LQFP

- **Full-Function CAN 2.0B Controller**
  - 15 message centers
  - Supports standard (11-bit) and extended (29-bit) identifiers and global masks
  - Media byte filtering to support DeviceNet™, SDS, and higher layer CAN protocols
  - Auto-baud mode and SIESTA low power mode
- **Integrated Primary System Logic**
  - 16 total interrupt sources with 6 external
  - Four 16-bit timer/counters
  - 2X/4X Clock Multiplier reduces EMI
  - Programmable watchdog timer
  - Oscillator fail detection
  - Programmable IrDA clock

- **Advanced Power Management**
  - Energy saving 1.8V Core
  - 3.3V I/O Operation, 5V tolerant
  - Power Management, idle and stop mode operation with switchback feature
  - Ethernet and CAN shutdown control for power conservation
  - Early warning power-fail interrupt
  - Power-fail reset
- **Enhanced Memory Architecture**
  - Selectable 8/10-bit stack pointer for high-level language support
  - 1kB additional on-chip SRAM usable as data/stack memory
  - 16-bit / 24-bit paged / 24-bit contiguous modes
  - Selectable multiplexed / non-multiplexed external memory interface
  - Merged program/data memory space allows in-system programming
  - Defaults to true 8051 memory compatibility

DESCRIPTION

The DS80C400 is a fast 8051-compatible microcontroller. The redesigned core executes 8051 instructions up to 3 times faster than the original for the same crystal speed. The DS80C400 supports a maximum crystal speed of 50 MHz, resulting in a minimum instruction cycle time of 80 ns. The DS80C400 utilizes an internal 24-bit program counter to achieve a flat 16MB address space, alleviating the bank switching methods often required to support code generated by high-level languages. To accelerate data transfer between the microcontroller and the 16MB memory map, the DS80C400 provides four data pointers, each of which can be configured to automatically increment or decrement upon execution of certain data pointer related instructions. The DS80C400's hardware math accelerator further increases the speed of 32 and 16 bit multiply and divide operations, as well as high-speed shift, normalization and accumulate functions.

With extensive network and I/O capabilities, the DS80C400 is equipped to serve as a central controller in a multitiered network. The 10/100 Ethernet Media Access Controller enables the DS80C400 to access and communicate over the Internet. While maintaining a presence on the Internet, the DS80C400 can actively control lower tier networks with dedicated on-chip hardware. These hardware resources include a full CAN 2.0B controller, a 1-Wire net controller, three full-duplex serial ports, and eight 8-bit ports (up to 64 digital I/O pins).

The DS80C400 Network Microcontroller provides instant connectivity and networking support via an embedded 64kB ROM. This ROM contains firmware to perform cold starts over an Ethernet or serial connection using Magic Packet, BOOTP or TFTP. The ROM firmware realizes a full, application accessible, TCP/IP stack, supporting both IPv4 and IPv6, and implements UDP, TCP, DHCP, ICMP, IGMP, and PPP. Additionally, the firmware has been structured so that a MAC address can be acquired from an IEEE registered DS2502-E48.

The 10/100 Ethernet Media Access Controller (MAC) featured on the DS80C400 complies with both the IEEE 802.3 MII and ENDEC PHY interface standards. The MII interface supports 10/100 Mbps bus operation, while the ENDEC interface supports 10Mbps operation. The MAC has been designed for low power standard operation and can optionally be placed into an ultra low-power sleep mode, to be awakened manually or by detection of a Magic Packet or wake-up frame. The DS80C400 minimizes the burden of Ethernet traffic on the CPU by incorporating a Buffer Control Unit. This Unit, after initial configuration through an SFR interface, manages all TX/RX packet activity and status reporting through an on-chip 8kB SRAM. To further reduce host (DS80C400) software intervention, the MAC can be setup to generate a hardware interrupt following each transmit or receive status report. The DS80C400 MAC can be operated in half-duplex or full-duplex mode and provides Multicast/Broadcast address filtering modes as well as VLAN tag recognition capability.

The DS80C400 features a full-function Controller Area Network (CAN) 2.0B controller. This controller provides 15 total message centers, 14 of which can be configured as either transmit or receive buffers and 1 which can serve as a receive double buffer. The device supports standard 11-bit or 29-extended message identifiers, and offers two separate 8-bit media masks and media arbitration fields to support the use of higher-level CAN protocols such as DeviceNet™ and SDS. A special auto-baud mode allows the CAN controller to quickly determine required bus timing when inserted into a new network. A SIESTA sleep mode has been made available for times when the CAN controller can be placed into a power saving mode.

The DS80C400 resources far exceed those normally provided on a standard 8-bit microcontroller. Many functions that might exist as peripheral circuits to a microcontroller have been integrated into the DS80C400 device. Some of the integrated functions of the DS80C400 include: 16 interrupt sources (6 external), four timer/counters, a programmable watchdog timer, a programmable IrDA output clock, an oscillator fail detection circuit, and an internal 2X/4X clock multiplier. This frequency multiplier allows the microcontroller to operate at full speed with a reduced crystal frequency, reducing EMI.

The DS80C400, with an advanced power management scheme, is well positioned for portable and power conscious applications. The microcontroller core operates on a 1.8V supply and the I/O, while 5V tolerant, operates on a 3.3V supply. A Power Management Mode (PMM) allows software to switch from the standard machine cycle rate of 4 clocks per cycle to 1024 clocks per cycle. For example, 50 MHz standard operation has a machine cycle rate of 12.5 MHz. In Power Management Mode, at the same external clock speed, software can select a 12.2 kHz

machine cycle rate. There is a corresponding reduction in power consumption when the processor runs slower. The microcontroller can be configured to automatically switch back from PMM to the faster mode in response to external interrupts or serial port activity. The DS80C400 provides the ability to place the CPU into an idle state or an ultra low power stop mode state. As protection against brown-out and power-fail conditions, the DS80C400 is capable of issuing an early warning power-fail interrupt and can generate a power-fail reset.

While the DS80C400 defaults to the true 8051 memory compatibility, the microcontroller is most powerful when taking advantage of its enhanced memory architecture. The DS80C400 has a selectable 10-bit stack pointer that can address up to 1kB of on-chip SRAM stack space for increased code efficiency. The DS80C400 can be operated in a 24-bit paged or 24-bit contiguous address mode, giving access to a much larger address range than the standard 16-bit address mode. The DS80C400 allows merged program and data memory access to support in-system programming and can be configured to internally demultiplex data and the lowest address byte, thereby eliminating the need for an external latch and potentially allowing the use of slower memory devices.

ORDERING INFORMATION

Part Number	Package	Max. Clock Speed	Temperature Range
DS80C400-FCS	100-pin LQFP	50 MHz	0°C to +70°C
DS80C400-FNS	100-pin LQFP	50 MHz	-40°C to +85°C