Enhanced Memory Systems Inc.

DM4M32SJ
4Mb x 32 Enhanced DRAM SIMM

Product Specification

Features

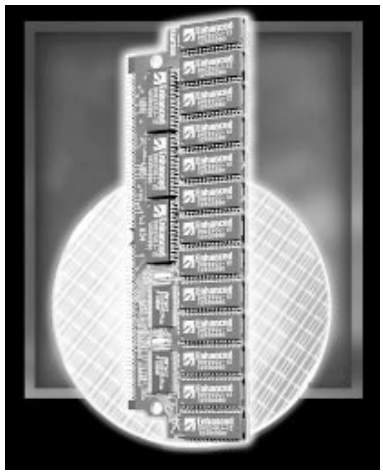
- Integrated 2,048 x 32 SRAM Cache Row Register Allows 12ns Access Random Reads Within the Page
- Interleaved SRAM Cache for 8ns Burst Reads
- 30ns DRAM Array for Fast Random Access to Any Page
- Ultra-Fast Integrated 8Kbyte-Wide DRAM to Cache Bus for 454-Gbyte/sec Cache Fill Bandwidth
- On-Chip Write Posting and Fast Page Mode Operation Allows 12ns Writes and Burst Writes
- On-Board Address and Control Buffering
- Low Power Self Refresh Mode Option

Description

The Enhanced Memory Systems 16MB EDRAM SIMM module provides a single memory module solution for the main memory or local memory of fast PCs, workstations, servers, and other high performance systems. Due to its fast 12ns cache row register, the EDRAM memory module supports zero-wait-state burst read operations at up to 66MHz bus rates in a non-interleave configuration and >100MHz bus rates with a two-way interleave configuration.

On-chip write posting and fast page mode operation supports 12ns write and burst write operations. On a cache miss, the fast DRAM array reloads the entire 8Kbyte cache over an 8Kbyte-wide bus in 18ns for an effective bandwidth of 454 Gbytes/sec. This means very low latency and fewer wait states on a cache miss than a non-integrated cache/DRAM solution. The JEDEC compatible SIMM configuration allows a single memory controller to be designed to support either JEDEC slow DRAMs or high speed EDRAMs to provide a simple upgrade path to higher system performance.

Architecture



The DM4M32SJ achieves 4Mb x 32 density by mounting 32 4M x 1 EDRAMs, packaged in 28-pin plastic SOJ packages on both sides of the multi-layer substrate. Four buffers have been added to reduce the loading on the address and control lines. The buffers have balanced output current levels and current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled fall times.

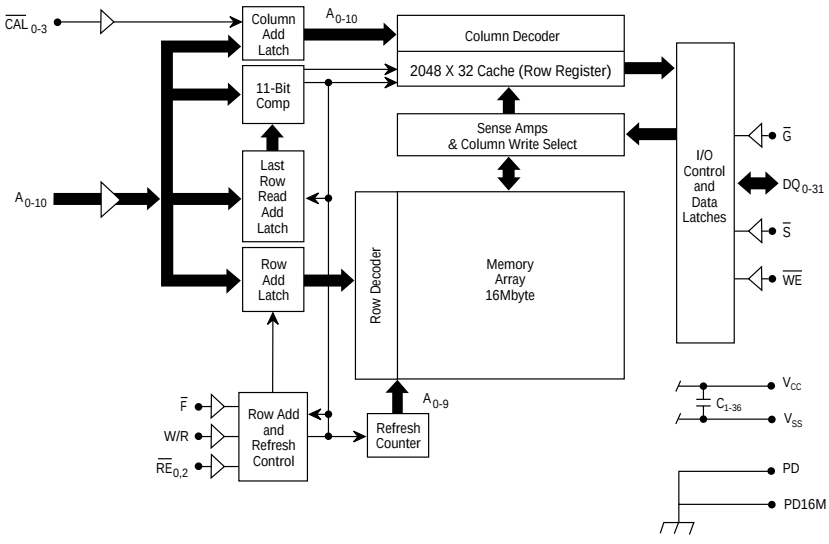
The EDRAM memory module architecture is very similar to a standard 16MB DRAM module with the addition of an integrated cache and on-chip control which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the on-chip comparator detects a page hit, only the SRAM is accessed and data is available in 12ns from column address. When a page read miss is detected, the entire new DRAM row is updated into the cache and data is available at the output all within a single 30ns access. Subsequent reads within the page (burst reads, local instructions, or data) will continue at 12ns cycle time. Since reads occur from the SRAM cache, DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

Memory writes are internally posted in 12ns and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 12ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance over standard slow DRAMs.

DM4M32SJ Functional Diagram



Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times t_{AC} or t_{GQV}. Since no DRAM activity is initiated, /RE can be brought high after time t_{RE1}, and a shorter precharge time, t_{RP1}, is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} or t_{CQV}.

DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times t_{RAC}, t_{AC}, and t_{GQV}. It is possible to bring /RE high after time t_{RE} since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time t_{AC} after each column address change in static column mode. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address. In page mode, data valid time is determined by either t_{AC} or t_{CQV}.

DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 12ns cycle times (the first read cannot complete until after time t_{RAC2}). At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to

EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	/CAL	/WE	A_{0-10}	Comment
Read Hit	L	↓	L	H	H	X	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	H	X	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	X	X	Cache Reads Enabled
Low Power Standby	H	H	X	X	H	H	X	Standby Current
Unallowed Mode	H	L	X	H	X	X	X	Unallowed Mode (Except -L Option)
Low Power Self Refresh Option	H	↓	X	H	L	H	X	Standby Current, Internal Refresh Clock

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE (t_{RAH} + t_{ASC} for the column address and t_{DS} for the data). During a write burst sequence, the second write data can be posted at time t_{RSW} after /RE. Subsequent writes within a page can occur with write cycle time t_{PC}. During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time t_{WRR} after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and t_{RE} is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

/RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time t_{AC} after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time t_{AC} after the column address is setup to /CAL.

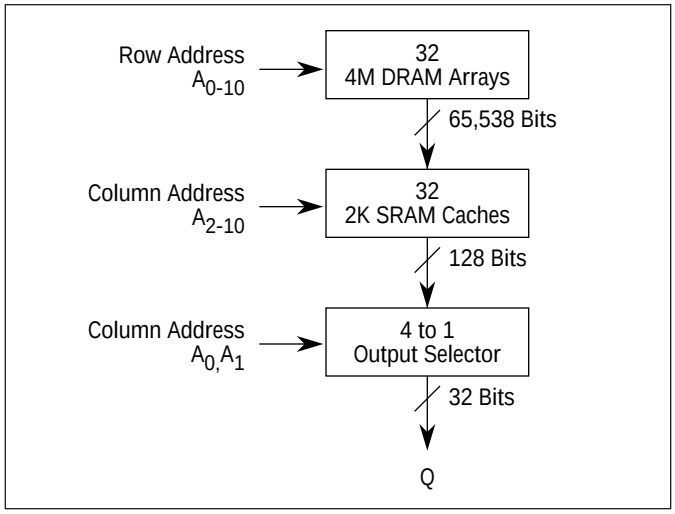
Function	/S	/G	/CAL	A_{0-10}
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

On-Chip SRAM Interleave

The DM4M32 has an on-chip interleave of its SRAM cache which allows 8ns random accesses (t_{AC1}) for up to three data words (burst reads) following an initial read access (hit or miss). The SRAM cache is integrated into the DRAM arrays in a 512 x 128 organization. It is converted into a 2K x 32 page organization by using an on-chip address multiplexer to select one of four 32-bit words to the output pins DQ_{0-31} (as shown below). The specific word selected to the output is determined by column addresses A_0 and A_1. System operation is consistent with the standard "Functional Description" and timing diagrams shown in this specification. See the note in the read timing diagrams and "Switching Characteristics" chart for the faster access and data hold times.

DM4M32 Datapath Architecture



Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F refresh cycle. At least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled.

/CAL Before /RE Refresh ("/CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

/RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses A_0, A_2 - A_{10} must be sequenced every 64ms refresh period. A_1 does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

Low Power Self Refresh

When the low power, self-refresh option is specified when ordering the EDRAM, the EDRAM enters this mode when /RE is clocked while /S, W/R, /F, and /WE are high; and /CAL is low. In this mode, the power is turned off to all I/O pins except /RE to minimize chip power and an on-board refresh clock is enabled to perform self-refresh cycles using the on-board refresh counter. The EDRAM remains in this low power mode until /RE is brought high again to terminate the mode. The EDRAM /RE input must remain high for t_{RP2} following exit from self-refresh mode to allow any on-going internal refresh to terminate prior to the next memory operation.

Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 34mA.

Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization. /RE must be high for 300ns prior to initialization.

Unallowed Mode

Read, write, or /RE only refresh operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

Reduced Pin Count Operation

It is possible to simplify the interface to the 16 MByte SIMM to reduce the number of control lines. /REO and /RE2 could be tied together externally to provide a single row enable. W/R and /G can be tied together if reads are not performed during write hit cycles. This external wiring simplifies the interface without any performance impact.

Pin Descriptions

/$RE_{0,2}$ — Row Enable

These inputs are used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /F. It is not necessary to clock /$RE_{0,1}$ to read data from the EDRAM SRAM row registers. On read operations, /$RE_{0,1}$ can be brought high as soon as data is loaded into cache to allow early precharge. /REO controls Bytes 1 and 2. /RE2 controls Bytes 3 and 4.

/CAL_{0-3} — Column Address Latch

These inputs are used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles. /CAL_{0-3} controls Bytes 1-4 respectively.

W/R — Write/Read

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

/F — Refresh

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

/WE — Write Enable

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

/G — Output Enable

This input controls the gating of read data to the output data pins during read operations.

/S — Chip Select

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in its low power mode. /S must remain active throughout any read or write operation. With the exception of /F refresh cycles, /$RE_{0,2}$ should never be clocked when /S is inactive.

DQ_{0-31} — Data Input/Output

These bidirectional pins are used to read and write data to the EDRAM.

PD — Presence Detect

This signal is grounded to indicate the presence of SIMM module in the socket.

PD16M — 16M Presence Detect

This signal is grounded to indicate the presence of a 16M SIMM. A 4 or 8 MB SIMM has this pin open.

A_{0-10} — Multiplex Address

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 11-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles. $A_{0,1}$ are used to select one of four interleaved data words during read operations.

V_{CC} Power Supply

These inputs are connected to the +5 volt power supply.

V_{SS} Ground

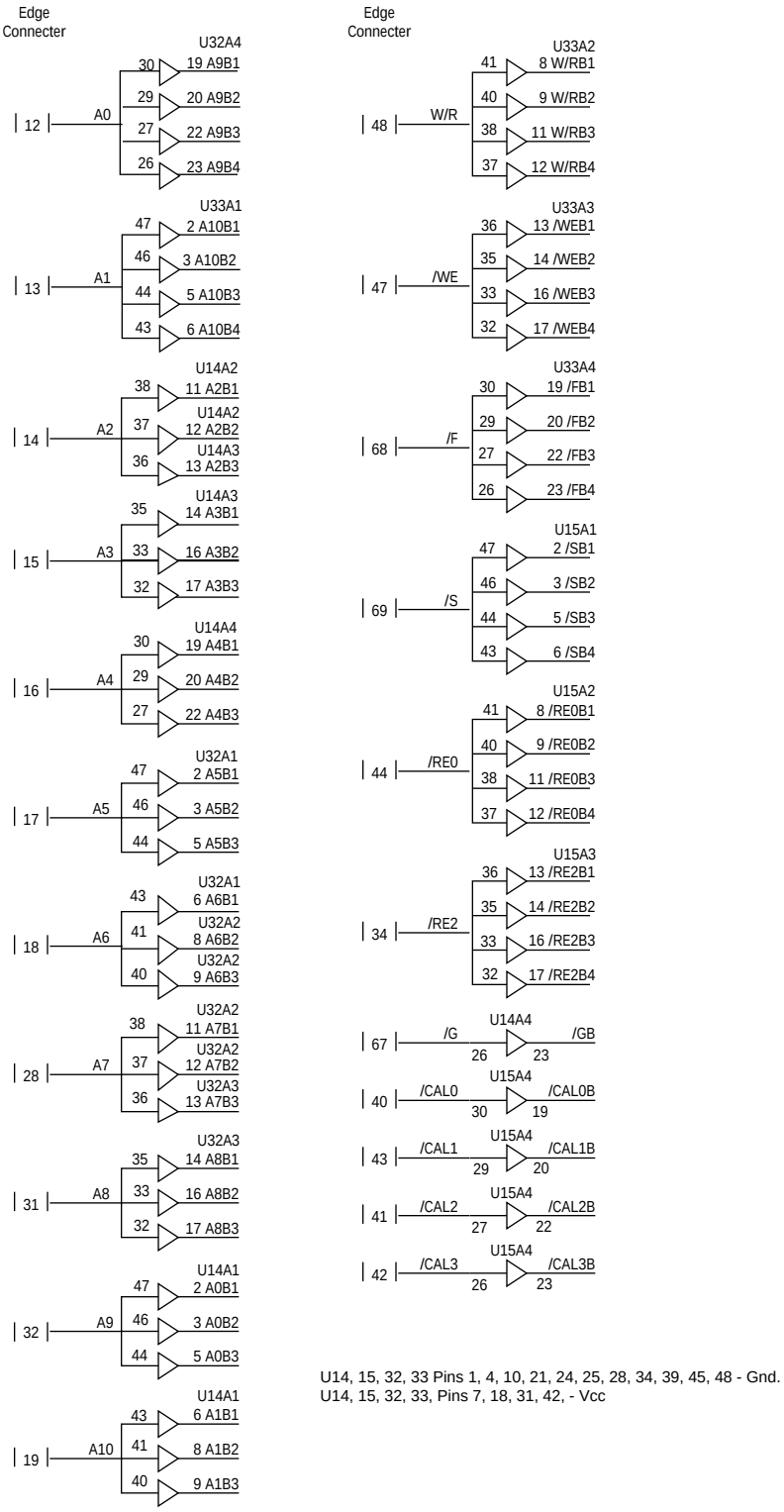
These inputs are connected to the power supply ground connection.

Pinout

Pin No.	*Function*		*Organization*
1	GND		Ground
2	DQ_0		Byte 1 I/O 1
3	DQ_{18}		Byte 3 I/O 1
4	DQ_1		Byte 1 I/O 2
5	DQ_{19}		Byte 3 I/O 2
6	DQ_2		Byte 1 I/O 3
7	DQ_{20}		Byte 3 I/O 3
8	DQ_3		Byte 1 I/O 4
9	DQ_{21}		Byte 3 I/O 4
10	+5 Volts		V_{CC}
11	+5 Volts		V_{CC}
12	A_0		Address
13	A_1		Address
14	A_2		Address
15	A_3		Address
16	A_4		Address
17	A_5		Address
18	A_6		Address
19	A_{10}		Address
20	DQ_4		Byte 1 I/O 5
21	DQ_{22}		Byte 3 I/O 5
22	DQ_5		Byte 1 I/O 6
23	DQ_{23}		Byte 3 I/O 6
24	DQ_6		Byte 1 I/O 7
25	DQ_{24}		Byte 3 I/O 7
26	DQ_7		Byte 1 I/O 8
27	DQ_{25}		Byte 3 I/O 8
28	A_7		Address
29	GND		Ground
30	+5 Volts		V_{CC}
31	A_8		Address
32	A_9		Address
33	NC		Not Connected
34	$\overline{RE}_2$		Row Enable (Bytes 3, 4)
35	GND		Ground
36	GND		Ground

Pin No.	*Function*		*Organization*
37	+5 Volts		V_{CC}
38	GND		Ground
39	GND		Ground
40	$\overline{CAL}_0$		Byte 1 Column Address Latch
41	$\overline{CAL}_2$		Byte 3 Column Address Latch
42	$\overline{CAL}_3$		Byte 4 Column Address Latch
43	$\overline{CAL}_1$		Byte 2 Column Address Latch
44	$\overline{RE}_0$		Row Enable (Bytes 1, 2)
45	NC		Not Connected
46	PD16M	Signal GND	Ground
47	$\overline{WE}$		Write Enable
48	W/R		W/R Mode Control
49	DQ_9		Byte 2 I/O 1
50	DQ_{27}		Byte 4 I/O 1
51	DQ_{10}		Byte 2 I/O 2
52	DQ_{28}		Byte 4 I/O 2
53	DQ_{11}		Byte 2 I/O 3
54	DQ_{29}		Byte 4 I/O 3
55	DQ_{12}		Byte 2 I/O 4
56	DQ_{30}		Byte 4 I/O 4
57	DQ_{13}		Byte 2 I/O 5
58	DQ_{31}		Byte 4 I/O 5
59	+5 Volts		V_{CC}
60	DQ_{32}		Byte 4 I/O 6
61	DQ_{14}		Byte 2 I/O 6
62	DQ_{33}		Byte 4 I/O 7
63	DQ_{15}		Byte 2 I/O 7
64	DQ_{34}		Byte 4 I/O 8
65	DQ_{16}		Byte 2 I/O 8
66	+5 Volts		V_{CC}
67	$\overline{G}$		Output Enable
68	$\overline{F}$		Refresh Mode Control
69	$\overline{S}$		Chip Select
70	PD	Signal GND	Presence Detect
71	GND		Ground
72	GND		Ground

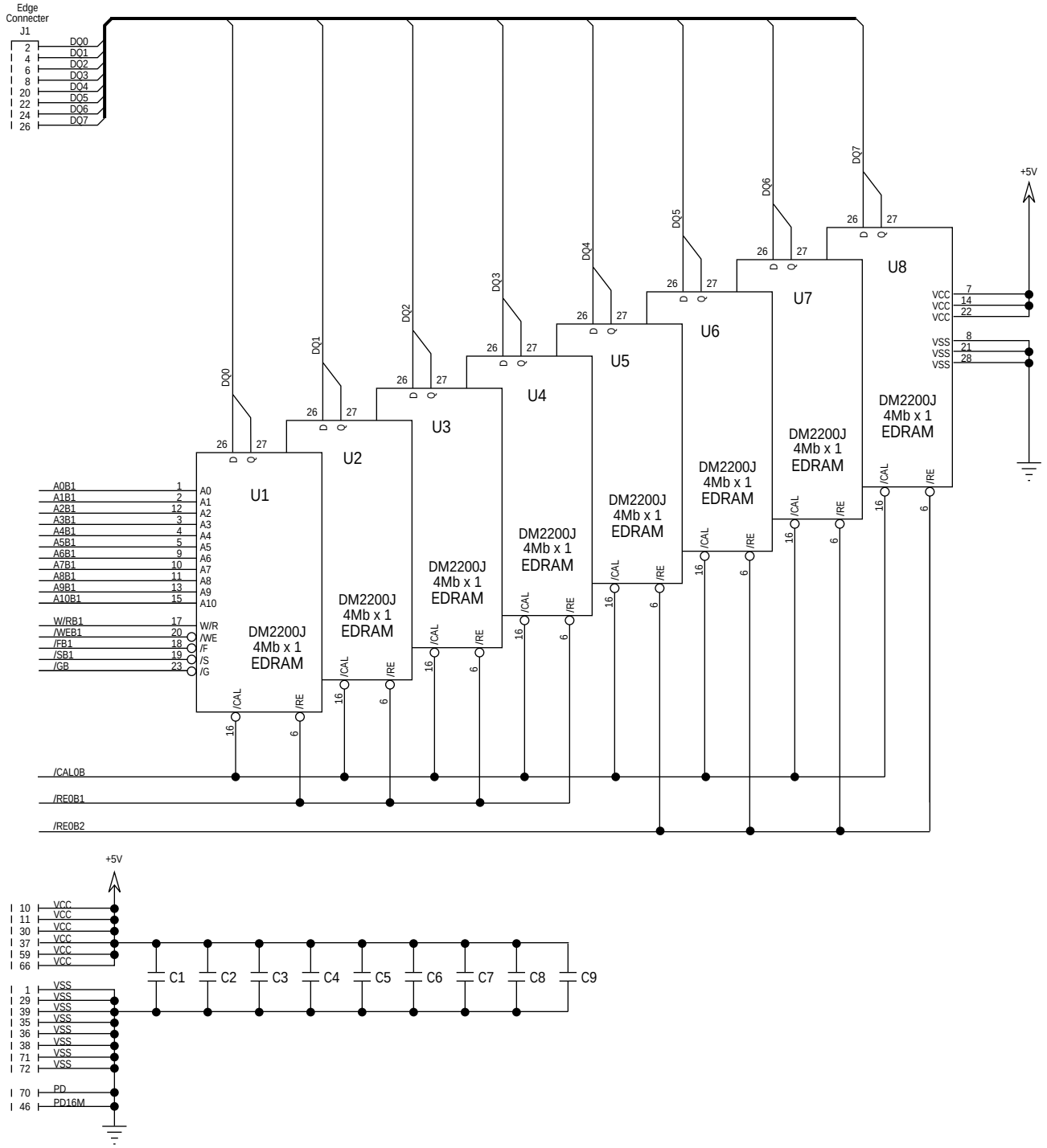
Buffer Diagram



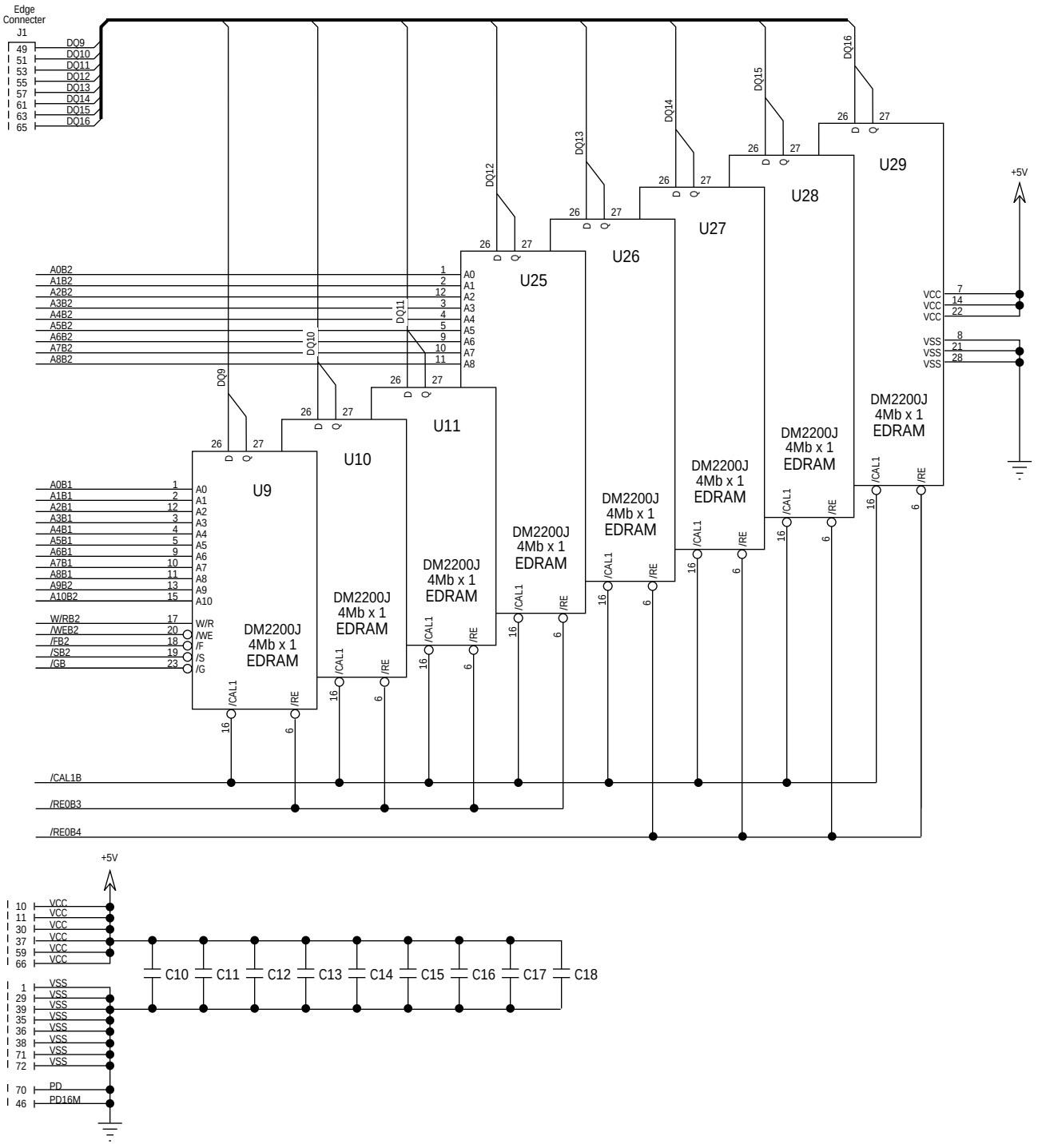
U14, 15, 32, 33 Pins 1, 4, 10, 21, 24, 25, 28, 34, 39, 45, 48 - Gnd.
U14, 15, 32, 33, Pins 7, 18, 31, 42, - Vcc

Note: Address and control buffers add minimum of 1.7ns to maximum of 4.5ns to each signal path.

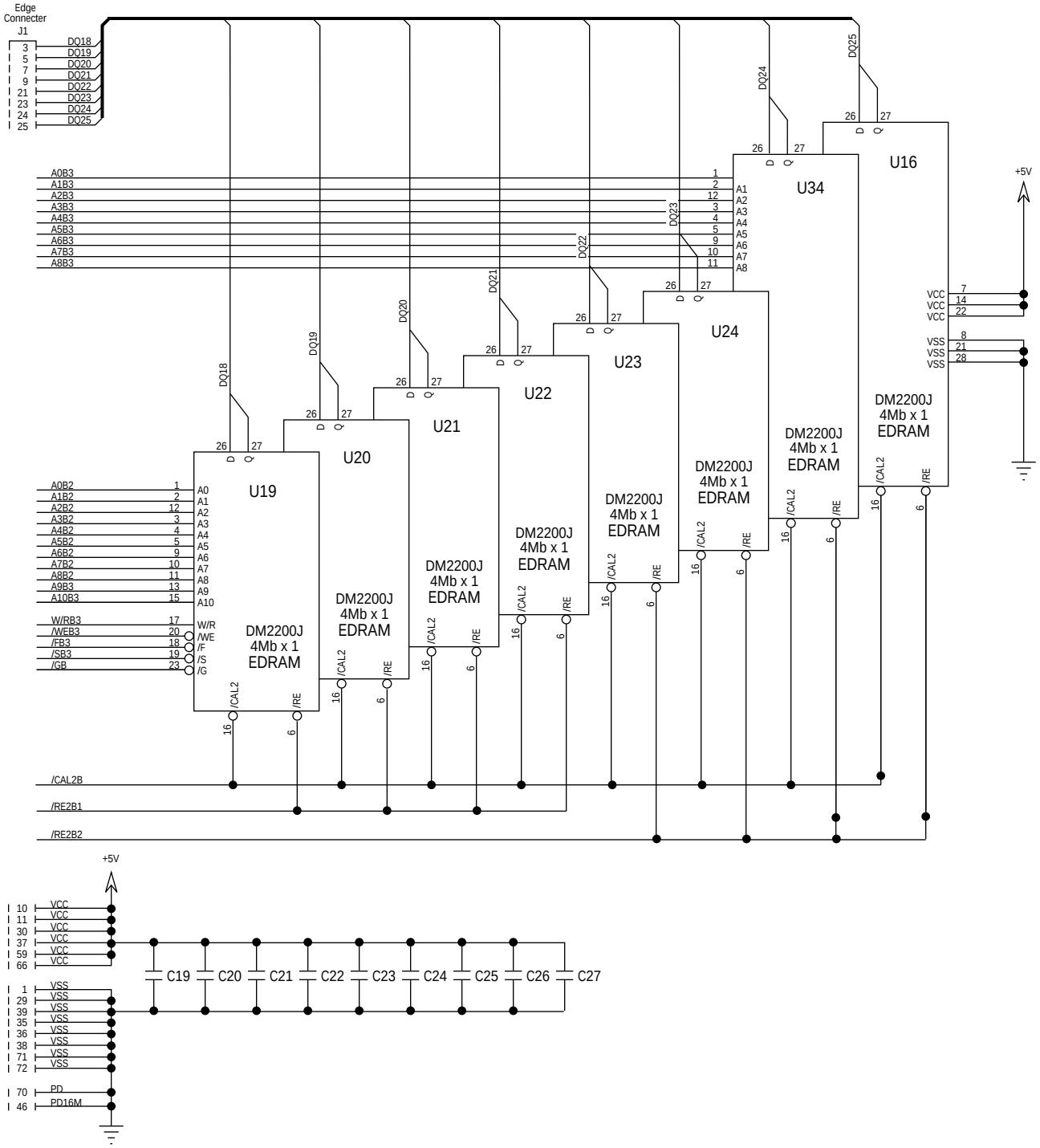
Interconnect Diagram — Byte 1



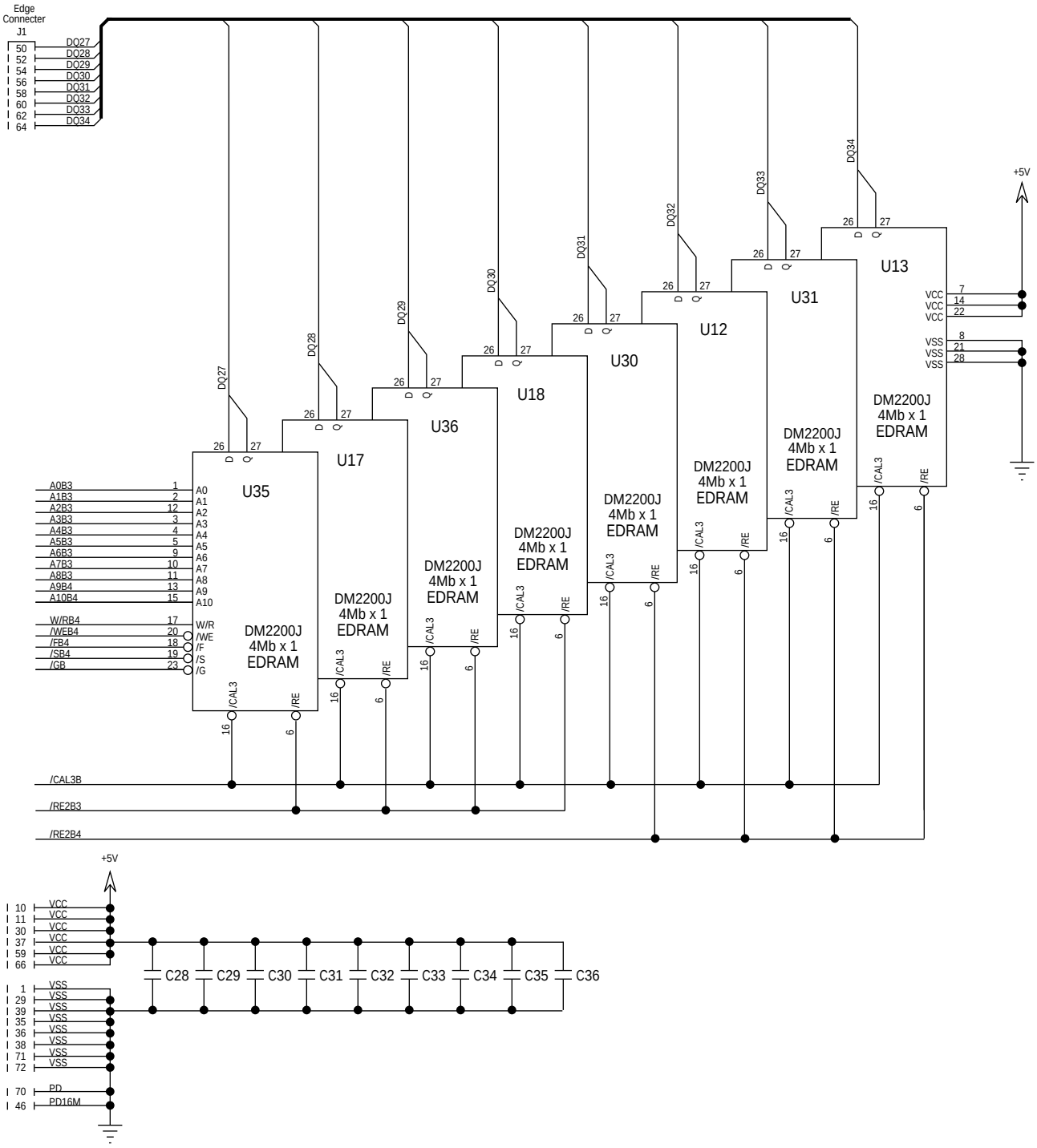
Interconnect Diagram — Byte 2



Interconnect Diagram — Byte 3

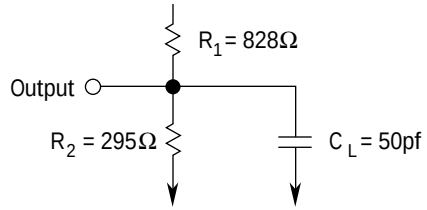


Interconnect Diagram — Byte 4

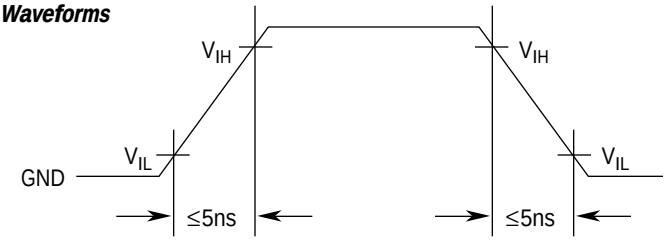


AC Test Load and Waveforms

Load Circuit



Input Waveforms



Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage (V_{IN})	- 1 ~ 7v
Output Voltage (V_{OUT})	- 1 ~ 7v
Power Supply Voltage (V_{CC})	- 1 ~ 7v
Ambient Operating Temperature (T_A)	0 ~ 70°C
Storage Temperature (T_S)	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	Class 1
Short Circuit O/P Current (I_{OUT})	50mA*

Capacitance

Description	Max	Pins
Input Capacitance	29pf	A_{0-10}
Input Capacitance	39pf	$/RE_0$, $/RE_2$, W/R, /WE, /F, /S
Input Capacitance	19pf	/G, $/CAL_{0-3}$
Input/Output Capacitance	18pf	DQ_{0-31}

Electrical Characteristics

Symbol	Parameters	Min	Max	Test Conditions
V_{CC}	Supply Voltage	4.75V	5.25V	All Voltages Referenced to V_{SS}
V_{IH}	Input High Voltage	2.4V	6.5V	
V_{IL}	Input Low Voltage	-1.0V	0.8V	
V_{OH}	Output High Level	2.4V	—	I_{OUT} = - 5mA
V_{OL}	Output Low Level	—	0.4V	I_{OUT} = 4.2mA
$I_{i(L)}$	Input Leakage Current	40µA	40µA	$OV \le V_{IN} \le 6.5V$, All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	20µA	20µA	$OV \le V_{IN}$, $OV \le V_{OUT} \le 5.5V$

Symbol	Operating Current	33MHz Typ(1)	-12 Max	-15 Max	Test Condition	Notes
I_{CC1}	Random Read	3840mA	7520mA	7520mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC2}	Fast Page Mode Read	2400mA	4960mA	4960mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC3}	Static Column Read	2080mA	3840mA	3840mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
I_{CC4}	Random Write	4640mA	6400mA	6400mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
I_{CC5}	Fast Page Mode Write	1920mA	4640mA	4640mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
I_{CC6}	Standby	36mA	36mA	36mA	All Control Inputs Stable $\ge V_{CC}$ - 0.2V, Outputs Driven	
I_{CC7}	Self-Refresh (-L Option)	6.4mA	6.4mA	6.4mA	/S, /F, W/R, /WE and A_{0-10} at $\ge V_{CC}$ - 0.2V, /RE and /CAL at $< V_{SS}$ + 0.2V, I/O Option	
I_{CCT}	Average Typical Operating Current	1280mA	1280mA	1280mA	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case I_{CC} expected in a system operating with a 33MHz memory bus. In this typical example, page mode and random reads refers to page burst hits and misses. Writes are two clock cycle random and page mode writes. See power applications note for further details. This parameter is not 100% tested or guaranteed.
(2) I_{CC} is dependent on cycle rates and is measured with CMOS levels and the outputs open.
(3) I_{CC} is measured with a maximum of one address change while /RE = V_{IL}.
(4) I_{CC} is measured with a maximum of one address change while /CAL = V_{IH}.

Switching Characteristics

V_{CC} = 5V ± 5%, T_A = 0 - 70°C, C_L = 50pf Note: These parameters do not include address and control buffer delays. See page 1-110 for derating factor.

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{AC}(1)	Column Address Access Time for Addresses A_{2-10}		12		15	ns
t_{AC1}(1)	Column Address Access Time for Addresses A_0 and A_1		8		8	ns
t_{ACH}	Column Address Valid to /CAL Inactive (Write Cycle)	12		15		ns
t_{AQX}	Column Address Change to Output Data Invalid for Addresses A_{0-8}	5		5		ns
t_{AQX1}	Column Address Change to Output Data Invalid for Addresses $A_{9 \text{ and } A_{10}}$	1		1		ns
t_{ASC}	Column Address Setup Time	5		5		ns
t_{ASR}	Row Address Setup Time	5		5		ns
t_C	Row Enable Cycle Time	55		65		ns
t_{C1}	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	20		25		ns
t_{CA}	Address Cycle Time (Cache Hits)	12		15		ns
t_{CAE}	Column Address Latch Active Time	5		6		ns
t_{CAH}	Column Address Hold Time	0		0		ns
t_{CH}	Column Address Latch High Time (Latch Transparent)	5		5		ns
t_{CHR}	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-2		-2		ns
t_{CHW}	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
t_{CQV}	Column Address Latch High to Data Valid		15		17	ns
t_{CQX}	Column Address Latch Inactive to Data Invalid for Addresses A_{0-8}	5		5		ns
t_{CQX1}	Column Address Latch Inactive to Data Invalid for Addresses A_9 and A_{10}	1		1		ns
t_{CRP}	Column Address Latch Setup Time to Row Enable	5		5		ns
t_{CWL}	/WE Low to /CAL Inactive	5		5		ns
t_{DH}	Data Input Hold Time	0		0		ns
t_{DS}	Data Input Setup Time	5		5		ns
t_{GQV}(1)	Output Enable Access Time		5		5	ns
t_{GQX}(2,3)	Output Enable to Output Drive Time	0	5	0	5	ns
t_{GQZ}(4,5)	Output Turn-Off Delay From Output Disabled (/G↑)	0	5	0	5	ns
t_{MH}	/F and W/R Mode Select Hold Time	0		0		ns
t_{MSU}	/F and W/R Mode Select Setup Time	5		5		ns
t_{NRH}	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
t_{NRS}	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		5		ns
t_{PC}	Column Address Latch Cycle Time	12		15		ns
t_{RAC}(1)	Row Enable Access Time, On a Cache Miss		30		35	ns
t_{RAC1}(1)	Row Enable Access Time, On a Cache Hit (Limit Becomes t_{AC})		15		17	ns
t_{RAC2}(1,6)	Row Enable Access Time for a Cache Write Hit		30		35	ns
t_{RAH}	Row Address Hold Time	1		1.5		ns

Switching Characteristics (continued)

V_{CC} = 5V ± 5%, T_A = 0 - 70°C, C_L = 50pf Note: These parameters do not include address and control buffer delays. See page 1-110 for derating factor.

Symbol	Description	-12		-15		Units
		Min	Max	Min	Max	
t_{RE}	Row Enable Active Time	30	100000	35	100000	ns
t_{RE1}	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{REF}	Refresh Period		64		64	ms
t_{RGX}	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	9		10		ns
t_{RQX1}	Row Enable High to Output Turn-On After Write Miss		12		15	ns
t_{RP}(7)	Row Precharge Time	20		25		ns
t_{RP1}	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	8		10		ns
t_{RP2}	Row Precharge Time, Self-Refresh Mode	100		100		ns
t_{RRH}	Read Hold Time From Row Enable (Write Only)	0		0		ns
t_{RSH}	Last Write Address Latch to End of Write	12		15		ns
t_{RSW}	Row Enable to Column Address Latch Low For Second Write	35		40		ns
t_{RWL}	Last Write Enable to End of Write	12		15		ns
t_{SC}	Column Address Cycle Time	12		15		ns
t_{SHR}	Select Hold From Row Enable	0		0		ns
t_{SQV}(1)	Chip Select Access Time		12		15	ns
t_{SQX}(2,3)	Output Turn-On From Select Low	0	12	0	15	ns
t_{SQZ}(4,5)	Output Turn-Off From Chip Select	0	8	0	10	ns
t_{SSR}	Select Setup Time to Row Enable	5		5		ns
t_T	Transition Time (Rise and Fall)	1	10	1	10	ns
t_{WC}	Write Enable Cycle Time	12		15		ns
t_{WCH}	Column Address Latch Low to Write Enable Inactive Time	5		5		ns
t_{WHR}	Write Enable Hold After /RE	0		0		ns
t_{WI}	Write Enable Inactive Time	5		5		ns
t_{WP}	Write Enable Active Time	5		5		ns
t_{WQV}(1)	Data Valid From Write Enable High		12		15	ns
t_{WQX}(2,5)	Data Output Turn-On From Write Enable High	0	12	0	15	ns
t_{WQZ}(3,4)	Data Turn-Off From Write Enable Low	0	12	0	15	ns
t_{WRP}	Write Enable Setup Time to Row Enable	5		5		ns
t_{WRR}	Write to Read Recovery (Cache Miss)		16		18	ns

(1) V_{OUT} Timing Reference Point at 1.5V

(2) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to V_{OH} or V_{OL}

(3) Minimum Specification is Referenced from V_{IH} and Maximum Specification is Referenced from V_{IL} on Input Control Signal

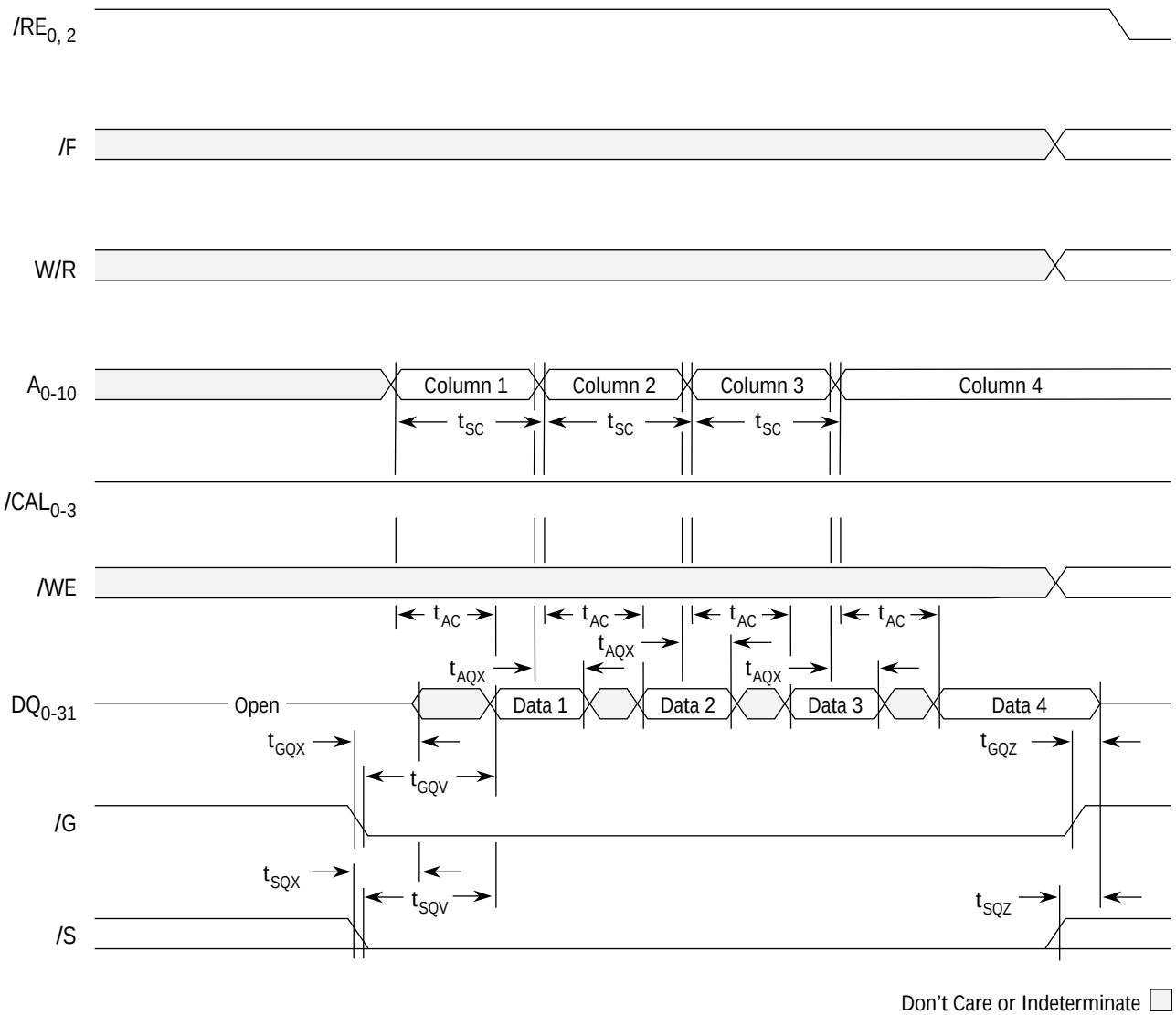
(4) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to V_{OH} or V_{OL}

(5) Minimum Specification is Referenced from V_{IL} and Maximum Specification is Referenced from V_{IH} on Input Control Signal

(6) Access Parameter Applies When /CAL Has Not Been Asserted Prior to t_{RAC2}

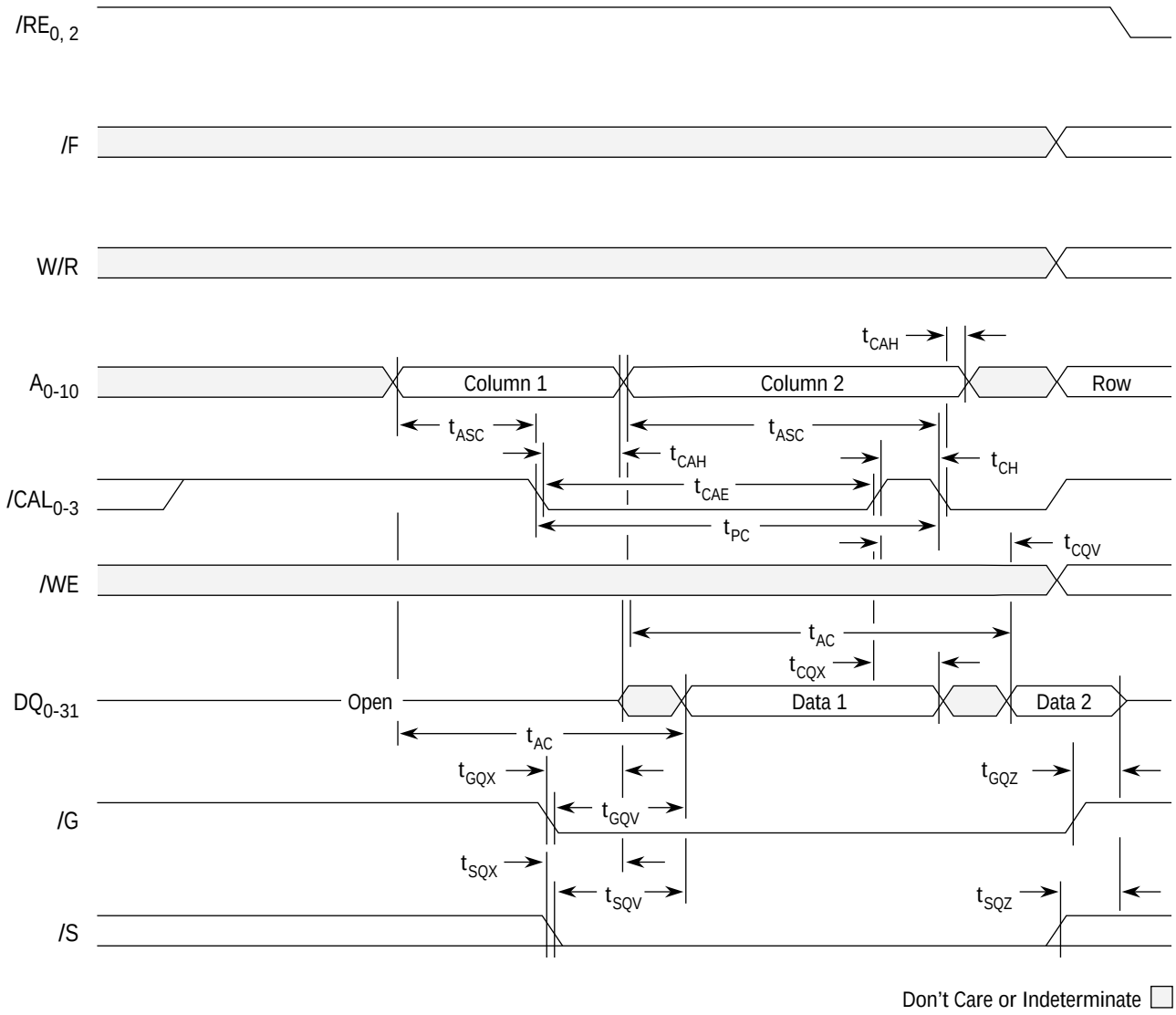
(7) For Back-to-Back /F Refreshes, t_{RP} = 40ns. For Non-Consecutive /F Refreshes, t_{RP} = 25ns and 32ns respectively.

/RE Inactive Cache Read Hit (Static Column Mode)



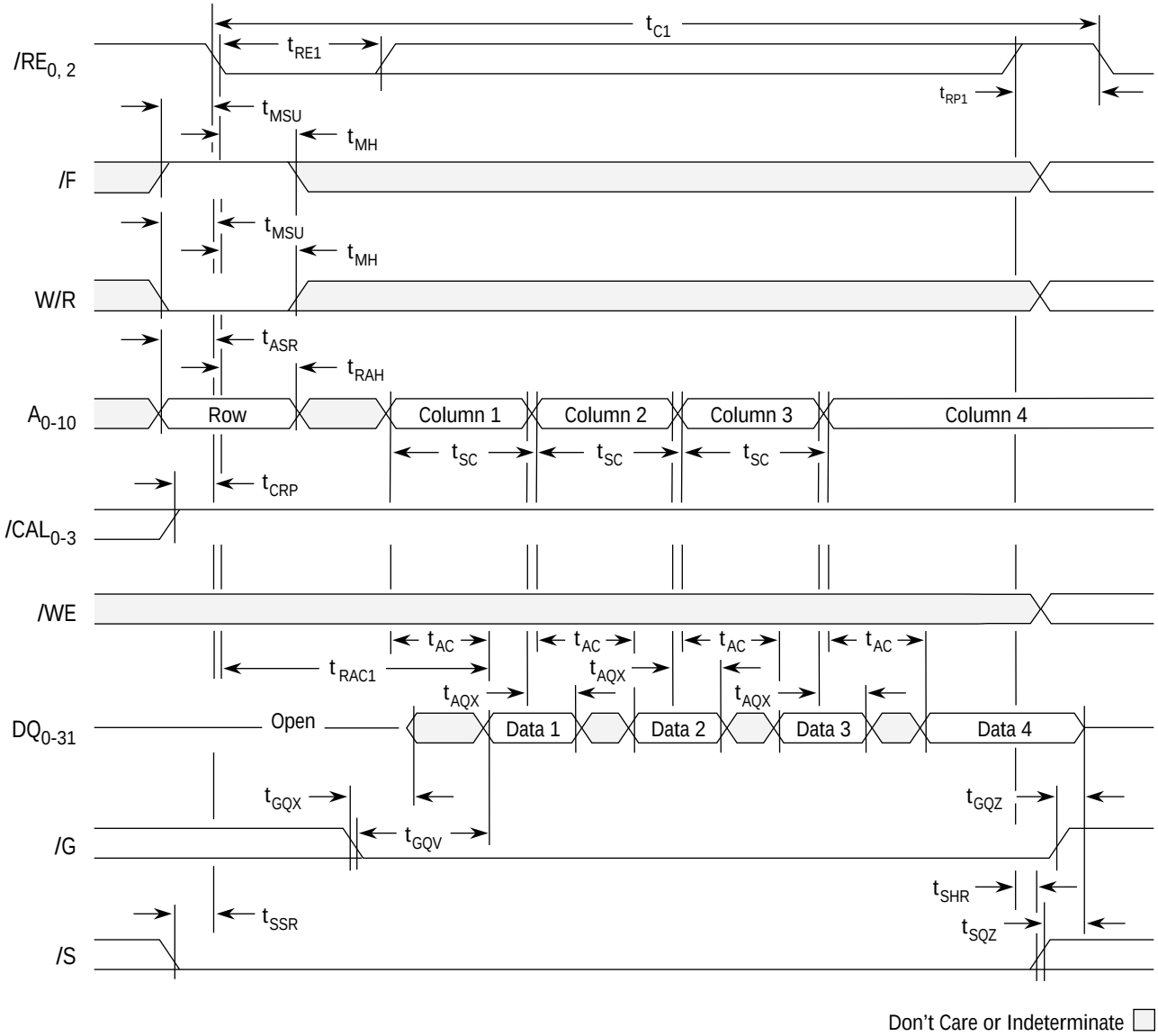
NOTES: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.
2. If column address 2, 3, or 4 modifies only address pin A_0 or A_1, then t_{AC} becomes t_{AC1} for data 2, 3, and 4, and t_{AQX} becomes t_{AQX1} for data 1, 2, and 3.

/RE Inactive Cache Read Hit (Page Mode)



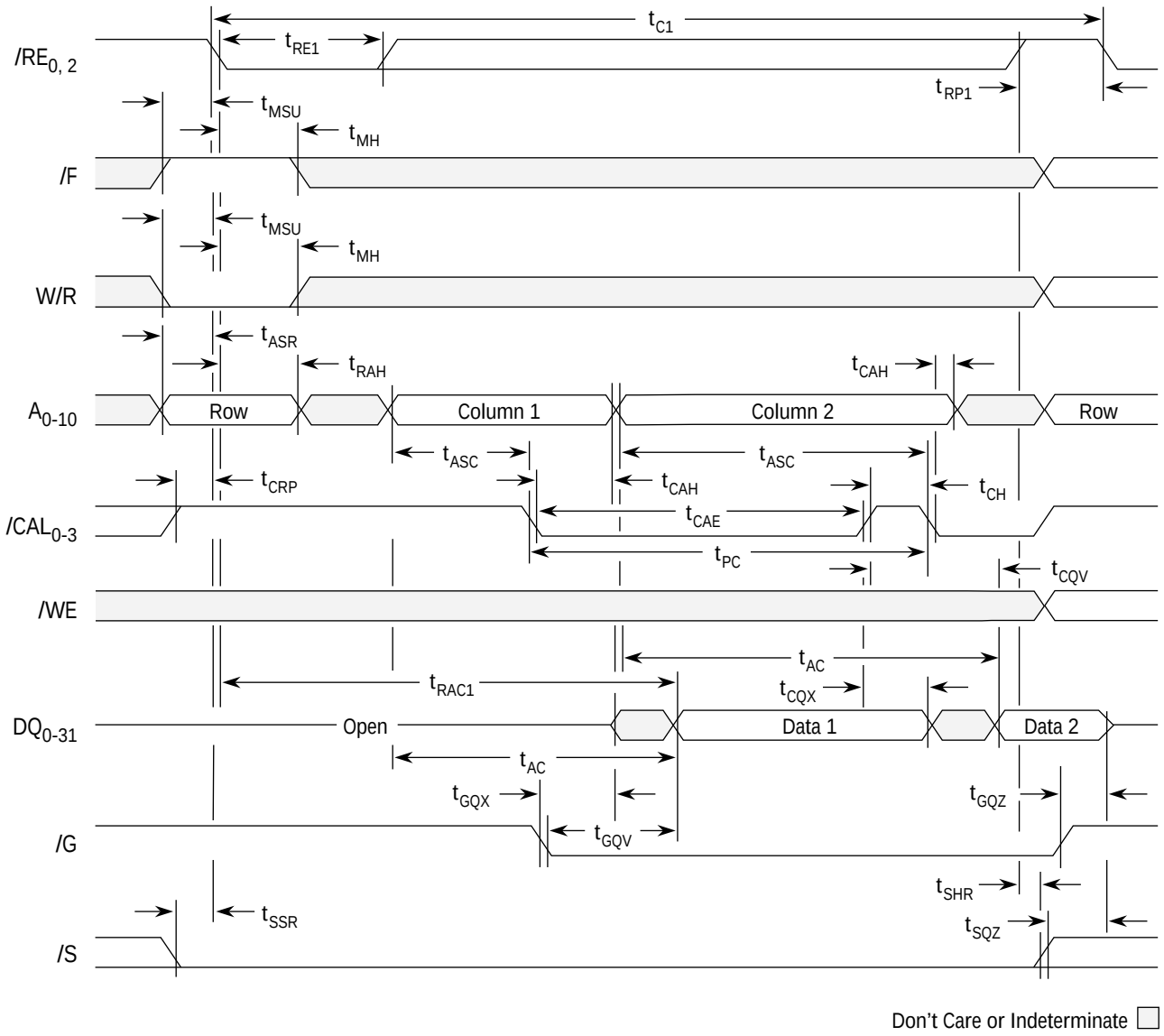
NOTES: 1. Data accessed during /RE inactive read is from the row address specified during the last /RE active read cycle.
2. If column address 2 modifies only address pin A_0 or A_1, then t_{AC} becomes t_{AC1} for data 2 and t_{CQX} becomes t_{CQX1} for data 1.

/RE Active Cache Read Hit (Static Column Mode)



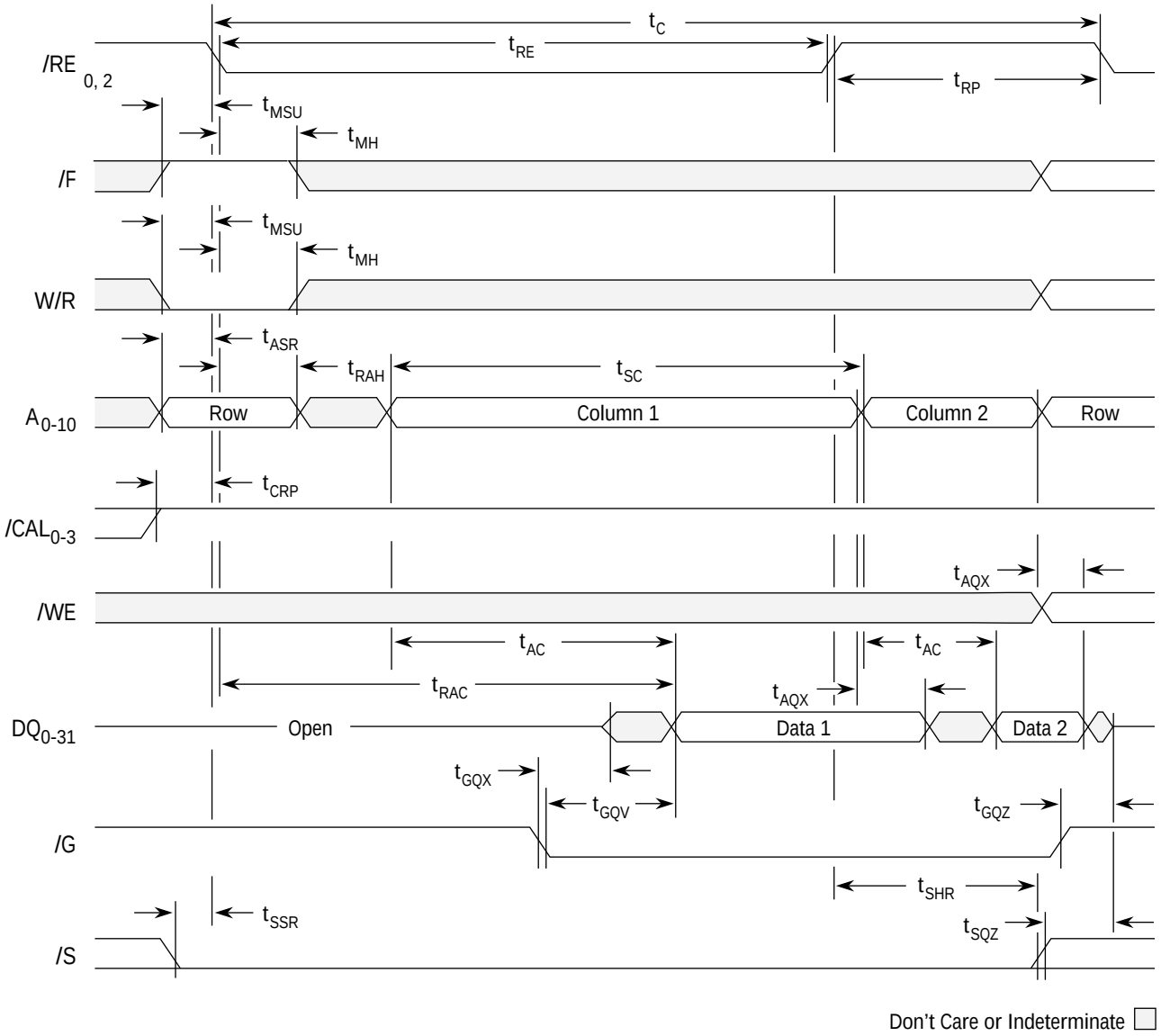
NOTES: 1. If column address 2, 3, or 4 modifies only address pin A_0 or A_1, then t_{AC} becomes t_{AC1} for data 2, 3, and 4, and t_{AQX} becomes t_{AQX1} for data 1, 2, and 3.

/RE Active Cache Read Hit (Page Mode)



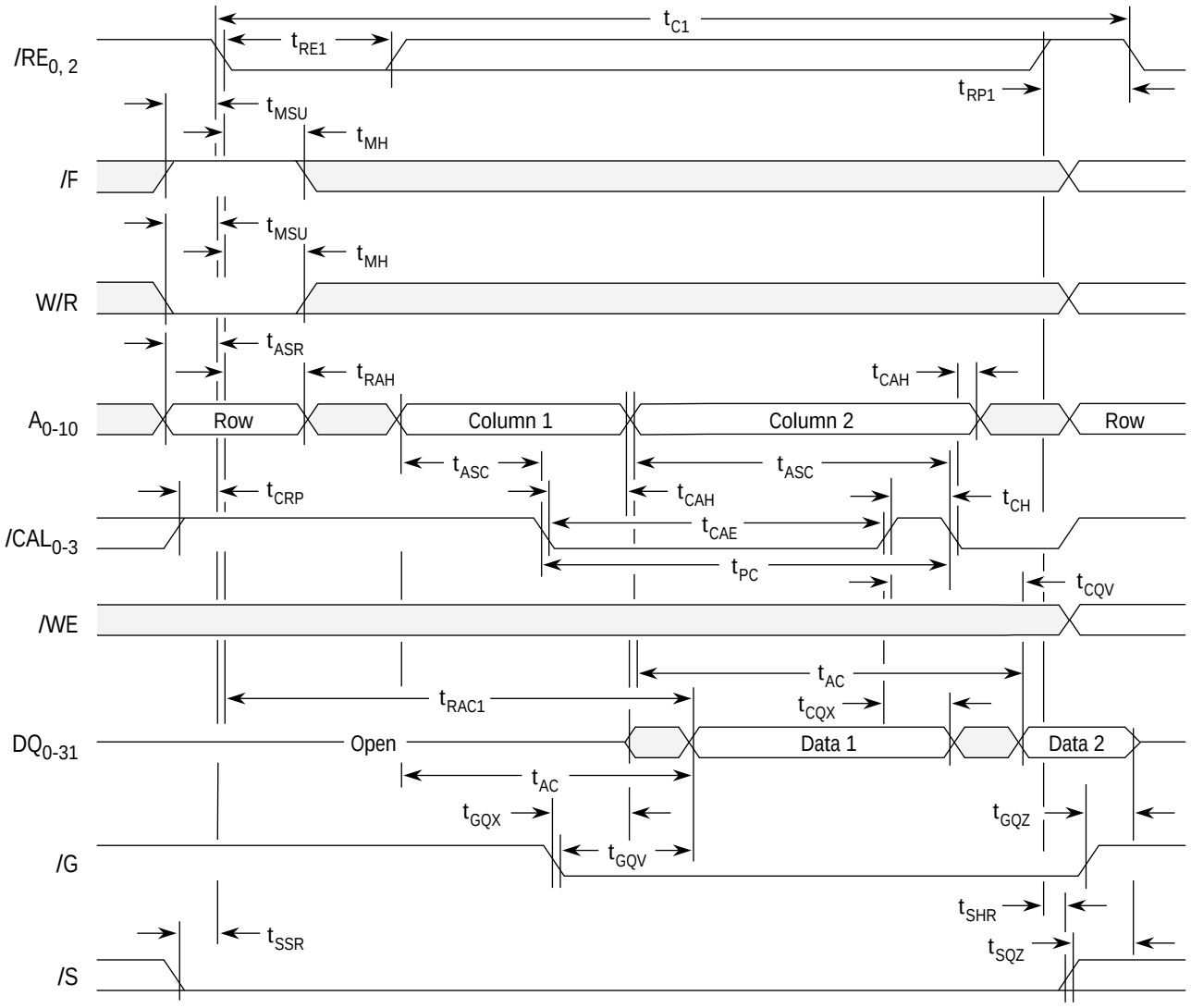
NOTES: 1. If column address 2 modifies only address pin A_0 or A_1, then t_{AC} becomes t_{AC1} for data 2 and t_{CQX} becomes t_{CQX1} for data 1.

/RE Active Cache Read Miss (Static Column Mode)



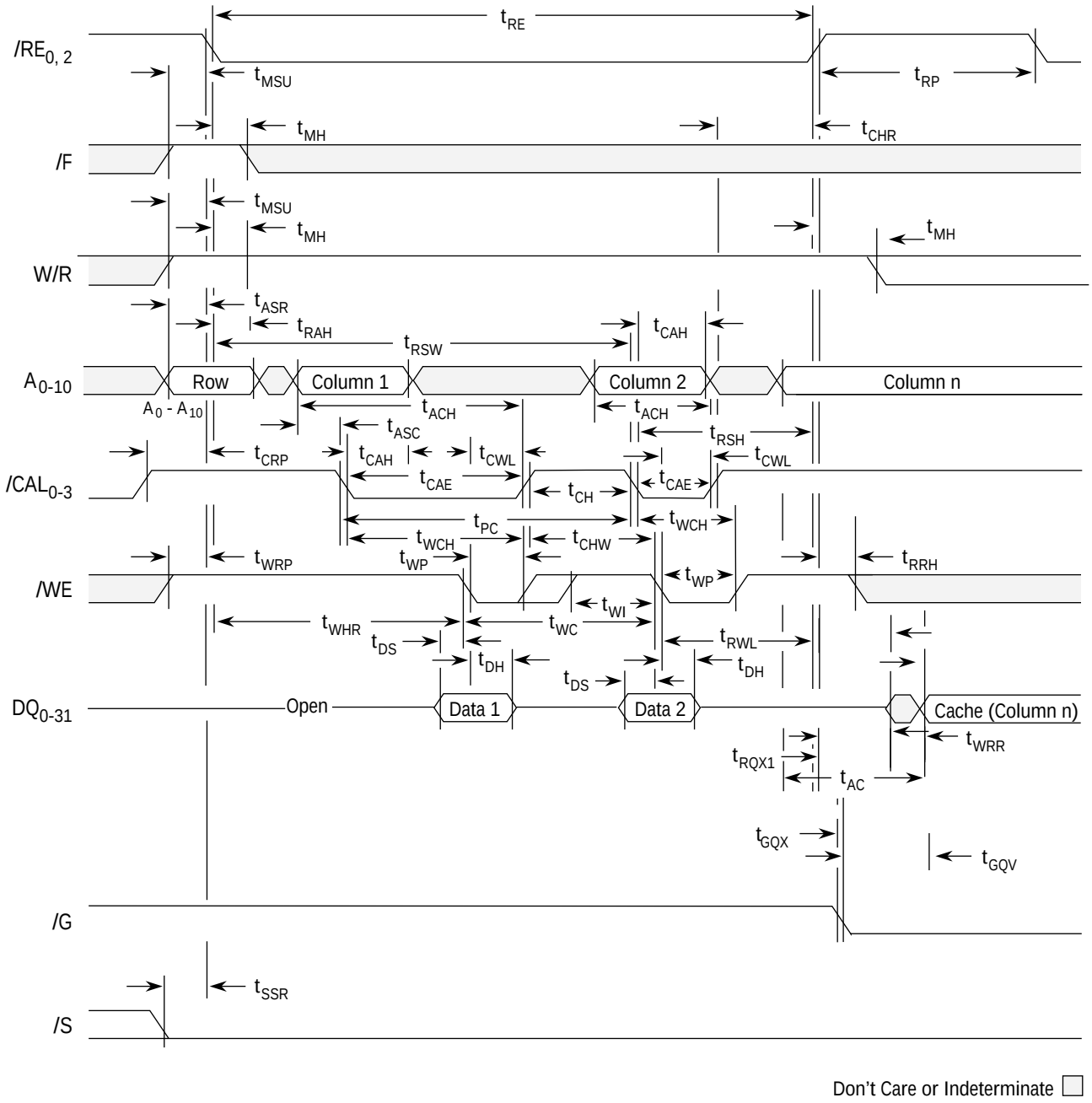
NOTES: 1. If column address 2 modifies only address pin A_0 or A_1, then t_{AC} becomes t_{AC1} for data 2, and t_{AQX} becomes t_{AQX1} for data 1.

/RE Active Cache Read Miss (Page Mode)



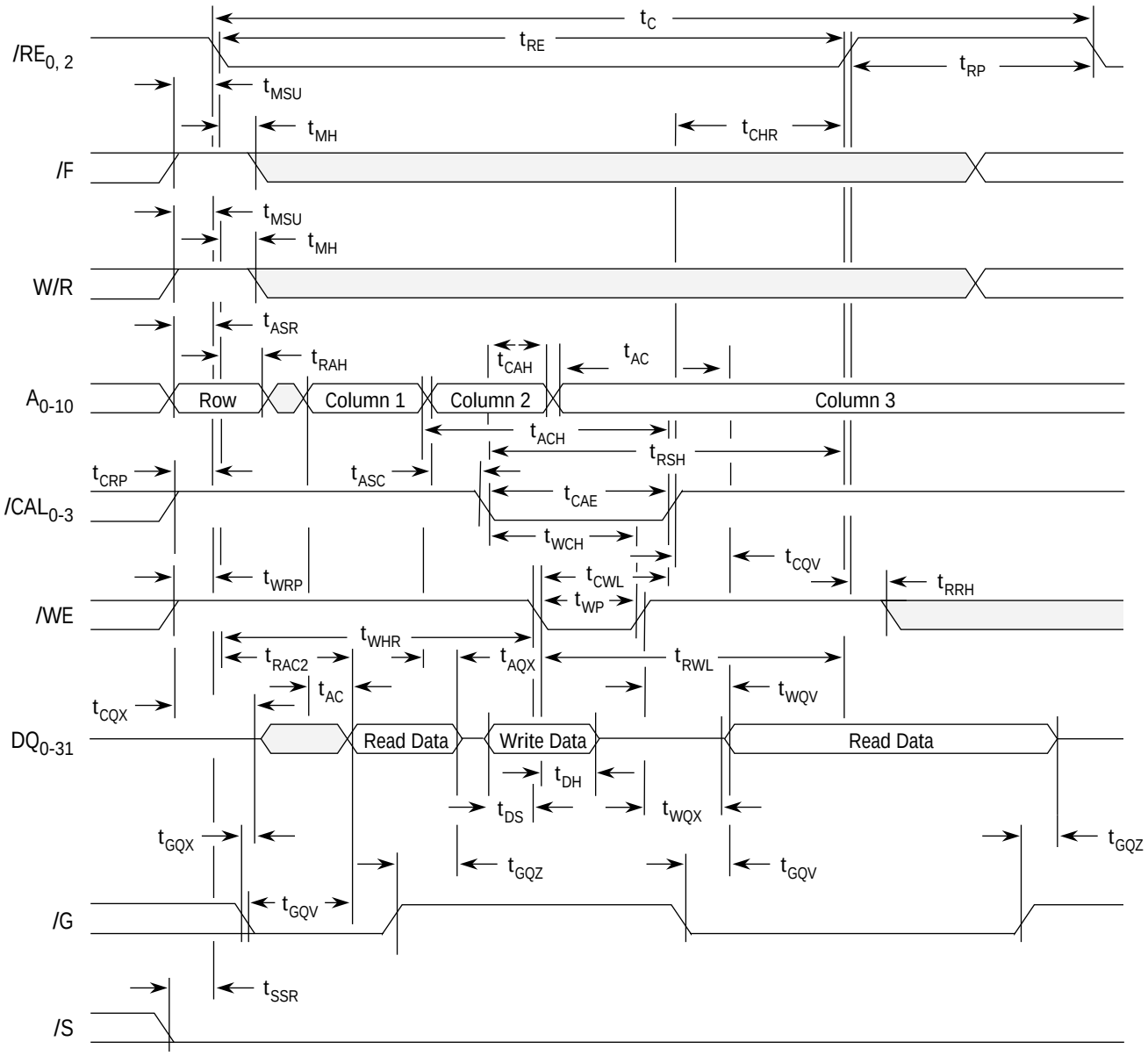
NOTES: 1. If column address 2 modifies only address pin A_0 or A_1, then t_{AC} becomes t_{AC1} for data 2 and t_{CQX} becomes t_{CQX1} for data 1.

Burst Write (Hit or Miss) Followed By /RE Inactive Cache Reads



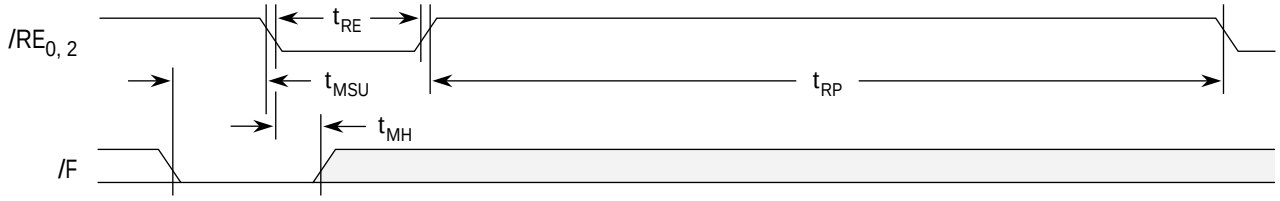
NOTES: 1. /G becomes a don't care after t_{RGX} during a write miss.

Page Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)



NOTES: 1. If column address 2 modifies only address pin A_0 or A_1, then t_{AQX} becomes t_{AQX1}.

/F Refresh Cycle

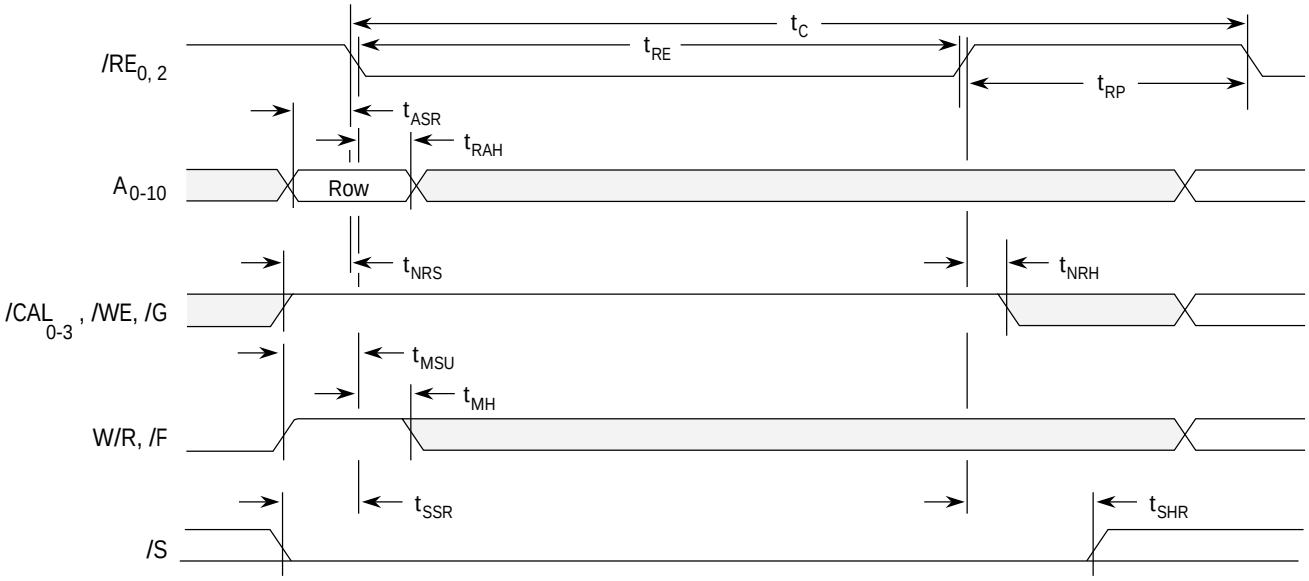


Don't Care or Indeterminate □

NOTES: 1. During /F refresh cycles, the status of W/R, /WE, $A_{0\text{-}10}$, /CAL, /S, and /G is a don't care.

2. /RE inactive cache reads may be performed in parallel with /F refresh cycles.

/RE-Only Refresh

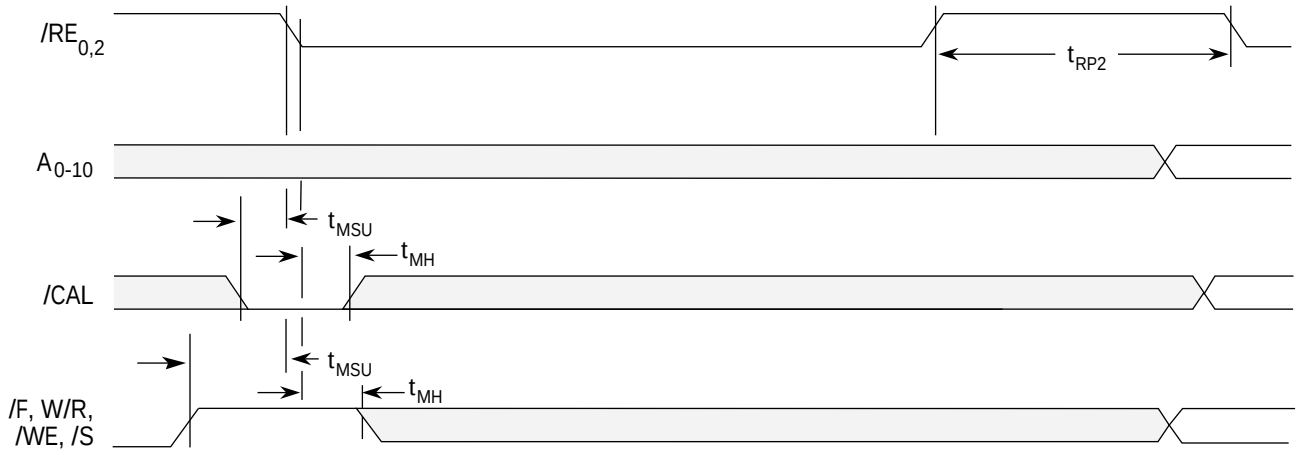


Don't Care or Indeterminate □

NOTES: 1. All binary combinations of A_0, $A_{2\text{-}10}$ must be refreshed every 64ms interval. A_1 does not have to be cycled, but must remain valid during row address setup and hold times.

2. /RE refresh is write cycle with no /CAL active cycle.

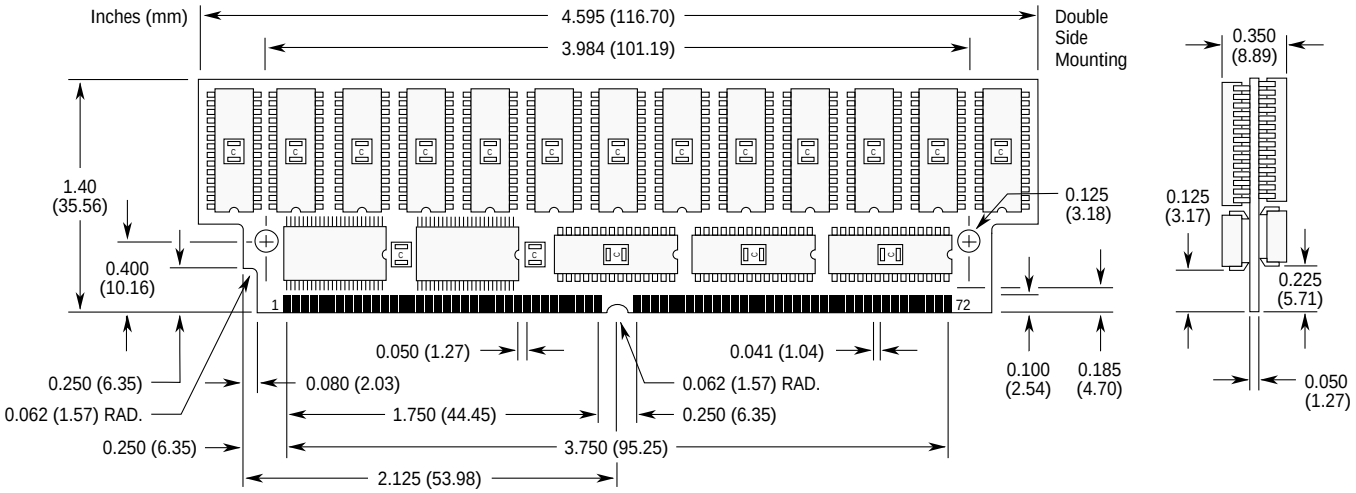
Low Power Self-Refresh Mode Option



Don't Care or Indeterminate ☐

NOTES: 1. EDRAM self refreshes as long as /RE remains low. (Low Power Self Refresh part only).
2. When using the Low Power Self Refresh mode the following operations must be performed:
If row addresses are being refreshed in an *evenly distributed* manner over the refresh interval using /F refresh cycles, then at least one /F refresh cycle must be performed immediately after exit from the Low Power Self Refesh Mode.
If row addresses are being refreshed in any other manner (/F burst or /RE distributed or burst), then all rows must be refreshed immediately befor entry to and immediately after exit from the Low Power Self Refresh.

Mechanical Data
DM4M32SJ 72 Pin Simm Module Configuration



U1-13, U16-31, U34-36 — Enhanced DM2200J-XX, 4M x 1 EDRAMs, 300 Mil SOJ
U14-15, U32-33 — IDT 74 FCT 162244CT PA 16-bit Buffer/Line Driver or Equivalent
C1-13, C16-31, C34-36 — 0.22µF Chip Capacitor
C14-15, C32-33 — 4.7µF Chip Capacitor
Socket — Amp 822030-3 or Equivalent

Part Numbering System

DM4M32SJ -12L

Lower Power, Self Refresh Option
No Designator = 0 to 70°C (Commercial)
L= 0 to 70°C, Low Power Self Refresh Option

Access Time from Cache in Nanoseconds
12ns
15ns

Packaging System
J = 300 Mil, Plastic SOJ

Memory Module Configuration
S = SIMM

I/O Width (Including Parity)
32 = 32 Bits

Memory Depth (Megabits)
4M

Dynamic Memory