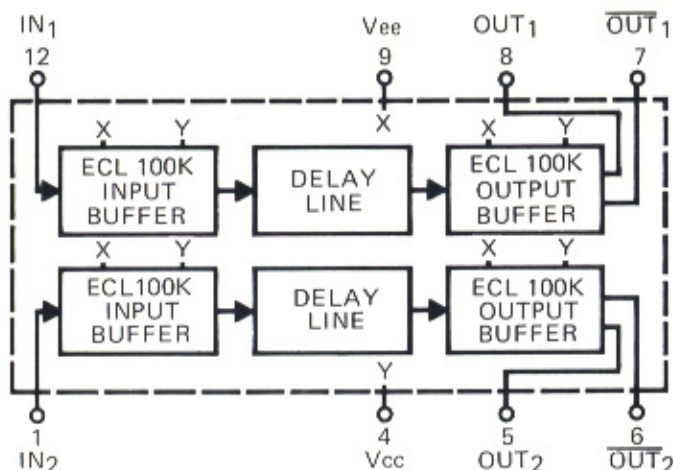
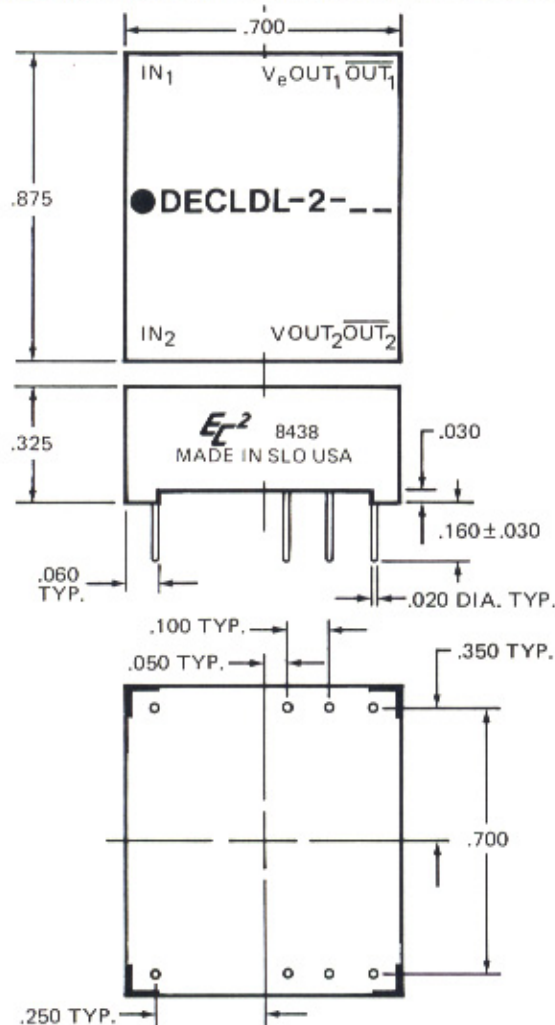


BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITONS

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at -4.5V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 100K gate. The input and output utilizes a 50 ohm pull-down resistor to -2V; the output is also loaded with one ECL 100K gate.
4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

- * Supply voltage: -4.5V $\pm$ 5% to Vee
- Supply current: 155ma typical
- Logic 1 Input at 25°C:
 - Voltage -1.165 min.
 - Current 350ua max.
- Logic 0 Input at 25°C:
 - Voltage -1.475V max.
 - Current5ua min.
- Logic 1 Output at 25°C: -1.025 min.
- Logic 0 Output at 25°C: -1.620 max.
- Operating temperature range: 0 to +85°C
- Storage temperature: -55 to +125°C
- * Delays increase or decrease less than .5% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
DECLDL-2-2	2 $\pm$.2	DECLDL-2-10	10 $\pm$ 1
DECLDL-2-2.5	2.5 $\pm$.2	DECLDL-2-10.5	10.5 $\pm$ 1
DECLDL-2-3	3 $\pm$.3	DECLDL-2-11	11 $\pm$ 1
DECLDL-2-3.5	3.5 $\pm$.3	DECLDL-2-11.5	11.5 $\pm$ 1
DECLDL-2-4	4 $\pm$.4	DECLDL-2-12	12 $\pm$ 1
DECLDL-2-4.5	4.5 $\pm$.4	DECLDL-2-12.5	12.5 $\pm$ 1
DECLDL-2-5	5 $\pm$.5	DECLDL-2-13	13 $\pm$ 1
DECLDL-2-5.5	5.5 $\pm$.5	DECLDL-2-13.5	13.5 $\pm$ 1
DECLDL-2-6	6 $\pm$.6	DECLDL-2-14	14 $\pm$ 1
DECLDL-2-6.5	6.5 $\pm$.6	DECLDL-2-14.5	14.5 $\pm$ 1
DECLDL-2-7	7 $\pm$.7	DECLDL-2-15	15 $\pm$ 1
DECLDL-2-7.5	7.5 $\pm$.7	DECLDL-2-16	16 $\pm$ 1
DECLDL-2-8	8 $\pm$.8	DECLDL-2-17	17 $\pm$ 1
DECLDL-2-8.5	8.5 $\pm$.8	DECLDL-2-18	18 $\pm$ 1
DECLDL-2-9	9 $\pm$.9	DECLDL-2-19	19 $\pm$ 1
DECLDL-2-9.5	9.5 $\pm$.9	DECLDL-2-20	20 $\pm$ 1

- ϕ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. [Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.](#)