Data Sheet

C-5e Network Processor

SILICON REVISION A0

C5ENPDATA-DS/D
Rev 01 PRELIMINARY

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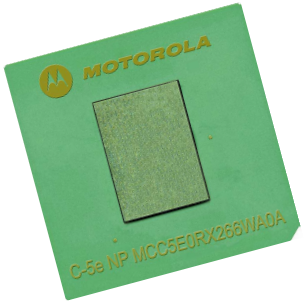

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Data Sheet

C-5e NETWORK PROCESSOR
SILICON REVISION A0

C5ENPDATA-DS/D
Rev 01

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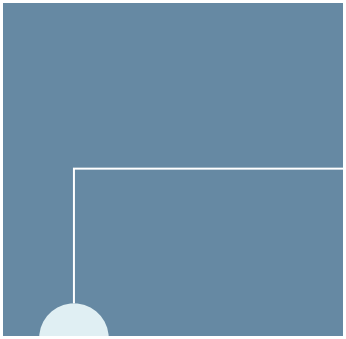

ABOUT THIS GUIDE

Guide Overview

The C-5e Network Processor Data Sheet describes hardware layout specifications including pinouts, memory configuration guidelines, timing diagrams, power and power sequencing guidelines, thermal design guidelines, and mechanical specifications.

This guide assumes a good understanding of the C-5e™ Network Processor (NP) architecture. See the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D)* for more detail about the hardware.

This guide also assumes good working knowledge of the C-Ware Software Toolset.

This guide covers the following topics:

- Functional Description
- Signal Descriptions
- Electrical Specifications
- Mechanical Specifications

Using PDF Documents

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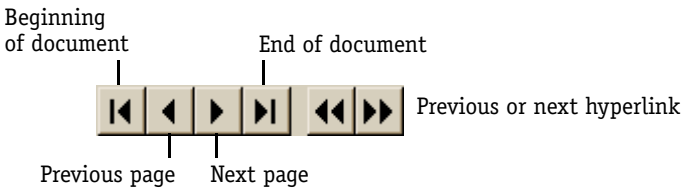

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Guide Conventions

The following visual elements are used throughout this guide, where applicable:

This icon and text designates information of special note.

Warning: *This icon and text indicate a potentially dangerous procedure. Instructions contained in the warnings must be followed.*

Warning: *This icon and text indicate a procedure where the reader must take precautions regarding laser light.*

This icon and text indicate the possibility of electrostatic discharge (ESD) in a procedure that requires the reader to take the proper ESD precautions.

Revision History

Table 2 provides details about changes made for each revision of this guide.

Table 2 *C-5e Network Processor Data Sheet* Revision History

REVISION DATE	CST REVISION	CDS REVISION	CHANGES
June 12, 2002	2.1	2.0	New document.

Related Product Documentation

Table 3 lists the user and reference documentation for Motorola's C-Port silicon documentation set.

Table 3 C-Port Silicon Documentation Set

DOCUMENT SUBJECT	DOCUMENT NAME	PURPOSE	DOCUMENT ID
Processor Information	*C-5 Network Processor Architecture Guide*	Describes the full architecture of the C-5 network processor.	C5NPARCH-RM/D
	C-5 Network Processor Data Sheet	Describes hardware design specifications for the C-5 network processor.	C5NPDATA-DS/D
	C-5e/C-3e Network Processor Architecture Guide	Describes the full architecture of the C-5e and C-3e network processors.	C5EC3EARCH-RM/D
	C-5e Network Processor Data Sheet	Describes hardware design specifications for the C-5e network processor.	C5ENPDATA-DS/D
	C-3e Network Processor Data Sheet	Describes hardware design specifications for the C-3e network processor.	C3ENPDATA-DS/D
	M-5 Channel Adapter Architecture Guide	Describes the full architecture of the M-5 channel adapter.	M5CAARCH-RM/D
	Q-5/Q-3 Traffic Management Coprocessor Architecture Guide	Describes the full architecture of the Q-5 and Q-3 traffic management coprocessor.	Q5Q3ARCH-RM/D

Chapter 1

FUNCTIONAL DESCRIPTION

Features

Key features of the C-5e™ Network Processor (NP) are its massive processing capabilities and its high level of functional integration on one chip.

Massive Processing Power

- Operating frequencies: up to 266MHz
- 5Gbps of bandwidth (for non-blocking throughput)
- More than 4,500MIPS of computing power (for adding services throughout the protocol stack)
- Up to 15 million packets per second transmitted at wire speed
- 17 programmable RISC Cores (for cell/packet forwarding)
- 32 programmable Serial Data Processors (for processing bit streams)
- Up to 133 million table lookups per second
- Three internal buses for 68Gbs of aggregate bandwidth

High Functional Integration

- 840 pin Ball Grid Array (BGA) package
- 16 Channel Processors including:
  - Embedded OC-3c, OC-12, OC-12c SONET framers
  - Programmable MAC interface
  - RISC Cores
  - Programmable pin PHY interfaces
- Embedded coprocessors for table lookup (classification), buffer management (payload control), and queue management (CoS/QoS implementation)
- Dedicated Fabric Processor and port

- Embedded RISC Executive Processor
- Integrated 32bit/66MHz PCI bus interface

Block Diagram

The C-5e™ NP, has an architecture specifically designed for networking applications. The following sections describe each component of the C-5e NP.

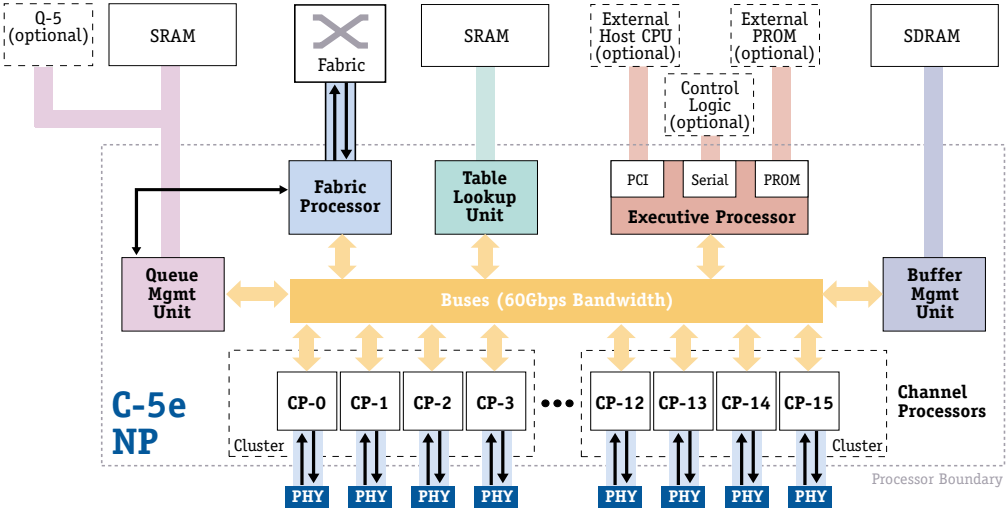
The main components of the C-5e NP are:

- Channel Processors
- Executive Processor
- Fabric Processor
- Buffer Management Unit
- Table Lookup Unit
- Queue Management Unit

Figure 1 shows a block diagram of the C-5e NP, including its potential external interfaces.

For more information about the architecture of the C-5e NP, see the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D)*.

Figure 1 C-5e Network Processor Block Diagram



PHY Interface Examples:

10/100 Ethernet

Gigabit Ethernet - Aggregated

OC-3

OC-12

1xOC-48c or 48x STS-1 with M-5 Companion Device

Channel Processors

The C-5e NP contains sixteen programmable Channel Processors (CPs) that receive, process, and transmit network data. The number of CPs per port is configurable, depending on the line interface. Typically one CP is assigned to each port for medium bandwidth applications (Fast Ethernet to OC-3). Multiple CPs can be assigned to a port in a configuration called *channel aggregation* in high bandwidth applications (greater than OC-3). Multiple logical ports can be assigned to a single CP, with the addition of an external multiplexor, for low bandwidth applications, such as DS1 to DS3.

The C-5e NP's architecture supports a variety of industry-standard serial and parallel protocols and individual port data rates including:

- 10/100Mb Ethernet (RMII)
- 1Gb Ethernet (GMII and TBI)
- OC-3c
- OC-12
- OC-48c (using various configurations with M-5 Channel Adapter)
- OC-48 (using various configurations with M-5 Channel Adapter)
- 100Mbit FibreChannel
- DS1/DS3, supported through the use of external framers/multiplexors

The C-5e NP's programmability can also support a variety of special interfaces, such as various xDSL encapsulations and proprietary protocols.

Key components of each CP are a RISC Core (CPRC) that orchestrates cell/packet processing and a set of microprogrammable, special-purpose processors, called Serial Data Processors (SDPs), that provide features such as Ethernet MAC and SONET framing, multichannel HDLC, and ATM cell delineation. This means you usually only need to include PHYs to complete the system.

Executive Processor

The Executive Processor (XP) serves as a centralized computing resource for the C-5e NP and manages the system interfaces.

The XP performs conventional supervisory tasks in the C-5e NP, including:

- Reset and initialization of the C-5e NP
- Program loading and control of CPs
- Centralized exception handling
- Management of a host interface through the PCI
- Management of system interfaces (PCI, Serial Bus, PROM)

System Interfaces

The system interfaces to the XP are:

- **PCI** — Provides an industry standard 32bit 33/66MHz PCI channel used for chip-level shared resources. The PCI has both *initiator* and *target* capabilities. The PCI interface is typically connected to a host processor.
- **Serial Bus Interface** — Provides a general purpose bi-directional, two-wire serial bus and I/O port that allows the C-5e NP to control external logic with either of two standard protocols:
  - The **MDIO (high-speed) protocol**: uses a 16bit data format with 10bits of addressing and supports transfers up to 25MHz.
  - The **low-speed protocol**: uses an 8bit data format followed by an acknowledge bit and supports transfers up to 400kbps.

  Software is used to select which protocol to use, by setting the appropriate bits in the Serial Bus Configuration Register. When a serial bus transfer is active, an external pin is driven by the C-5e NP to indicate which protocol is being used (SPLD=0 indicates MDIO protocol; SPLD=1 indicates low-speed protocol).

  Both SIDA and SICL are bi-directional lines that are connected, via an external pull-up resistor, to a positive supply voltage. When the bus is free, both lines are HIGH because of the pull-up resistor. The output stages of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism.

- **PROM Interface** — Allows the XP to boot from nonvolatile, flash memory. The PROM interface is a low-speed, serial I/O port that runs at $^1/_2$ to $^1/_{16}$ the core clock rate. The maximum PROM size is 8MBytes, and a 16bit wide configuration is required. External board logic is required to perform serial-to-parallel conversion for PROM address outputs and parallel-to-serial conversion for PROM data inputs.

Fabric Processor

The Fabric Processor (FP) acts as a high-speed network interface port with advanced functionality. It allows the C-5e NP to interface to an application-specific switching solution internal to your design. The FP port supports the bidirectional transfer of segments from the C-5e NP to a hardware interface that provides connectivity to other network processors or other similar line processing hardware. There are numerous parameters that can be configured within the FP to allow the interface to be adapted to different fabric protocols. The FP can be configured to conform to seven (7) different fabric interfaces that include: CSIX-L1, UTOPIA-1, -2, -3, PRIZMA, Power X(CSIX-L0), and UTOPIA3 like to M-5.

The FP can be configured to run at any frequency up to 125MHz, with the receive and transmit data buses up to 32 bits wide. This allows a wide range of supported bandwidths to and from the switching fabric, all the way up to 4000 Mbps full duplex bandwidth.

Buffer Management Unit

The Buffer Management Unit (BMU) interfaces the C-5e NP to external pipeline architecture, Single Data Rate Synchronous DRAM. The external memory is partitioned and used as buffers for receiving and transmitting data between CPs, the FP, and the XP. It is also used as second level storage in the XP memory hierarchy.

The interface to an array of SDRAM chips is 139bits wide, composed of 128 data bits, two internal control bits, and nine SECDED (single error correction-double error detection) ECC (error correction code) bits. The interface is compliant with the PC100 standard and operates at up to 133MHz with 3.3V LVTTL-compatible inputs and outputs. The refresh period, Trcd, Tcas, Trp, Tmrd, and Trc are configurable via boot time configuration (see the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D)* for more details).

The C-5e NP non-configurable interface transfers four beats of data for each read and write using a sequential burst type. In addition, the C-5e NP uses an auto-refresh mode for the RAM's.

Some of these parameters are programmed into the SDRAMs' mode register and can be applied only once per power cycle. The ECC functionality can be enabled or disabled via configuration register writes.

If needed, the interface can narrowed to 128bits by disabling ECC and providing board pull-ups for the two control bits and nine ECC bits. This is useful if DIMMs are used in the board design. If individual SDRAM parts are used, x16 and x32 are supported. The BMU supports SDRAM devices that use 12 address lines. Internal address calculation paths limit the maximum memory size to 128MBytes. Only one physical bank of SDRAM is supported.

Table Lookup Unit

The Table Lookup Unit (TLU) performs table lookups in external SRAM. It can also be used for statistics accumulation and retrieval and as general data storage. The TLU simultaneously supports multiple application-defined tables and multiple search strategies, such as those needed for routing, circuit switching, and QoS lookup tasks.

The C-5e NP uses external 64bit wide ZBT Pipelined Bursting Static RAM (SRAM) modules (at frequencies up to 133MHz) for storage of its tables. These modules allow implementation of tables with 2^{25} x 64bit entries using 8Mbit SRAM technology. The maximum amount of memory supported by the TLU is 128MBytes in four banks, when SRAM technology supports 4M x 18pins parts.

Table 4 TLU SRAM Configurations

SRAM TECHNOLOGY	MIN TABLE SIZE (ONE BANK)	MAXIMUM TABLE SIZE (FOUR BANKS)
1Mbit (32k x 32pins)	256kBytes	1MBytes
2Mbit (64k x 32pins)	512kBytes	2MBytes
4Mbit (256k x 18pins)	2MBytes	8MBytes
8Mbit (512k x 18pins)	4MBytes	16MBytes
16Mbit (1M x 18pins)	8MBytes	32MBytes
32Mbit (2M x 18pins)	16MBytes	64MBytes
64Mbit (4M x 18pins)	32MBytes	128MBytes

Queue Management Unit

The Queue Management Unit (QMU) autonomously manages a number of application-defined descriptor queues. It handles inter-CP and inter-C-5e NP descriptor flows by providing switching and buffering. It also performs descriptor replication for multicast applications. A number of up to 128 queues can be assigned to each CPRC for QoS-based services.

The QMU provides a queuing engine internal to the chip and uses external SRAM to store the descriptors. Scheduling is done by the CPs. The QMU supports up to 512 queues and 16, 384 descriptor buffers. A descriptor buffer holds an application-defined "descriptor", which is a structure that defines the payload buffer handle and other attributes of the forwarded cell or packet.

The QMU's external SRAM interface uses ZBT synchronous SRAMs organized in a single bank of up to 128k, 32bit words. This interface runs at up to 175MHz frequency.

The C-5e provides two modes for managing queues. They consist of:

- Internal Mode (using the internal QMU only)
- External Mode (using the internal QMU and the external Q-5 Traffic Management Coprocessor)

See the *C-5e/C-3e Network Processor Architecture Guide (part number C5EC3EARCH-RM/D)* for more details.

Chapter 2

SIGNAL DESCRIPTIONS

Signal Summary

There are ten (10) functional groupings of signals in the C-5e Network Processor:

- Clock — 11 pins
- Channel Processors (CP0 - CP15) — 16x7 = 112 pins
- Executive Processor (XP) — 57 pins
  - PCI Interface — 50 pins
  - PROM Interface — 4 pins
  - Serial Bus Interface — 2 pins
  - General System Interface — 1 pin
- Fabric Processor (FP) — 80 pins
- Buffer Management Unit (BMU) — 160 pins
- Table Lookup Unit (TLU) — 99 pins
- Queue Management Unit (QMU) — 59 pins
- Power — 238 pins
- Test — 14 pins
- No connection (NC) — 10 pins

Two (2) of the sections (CPs and FP) are configurable, depending on the type of device being implemented.

Pinout Diagram

The C-5e NP contains 840 pins. These pin numbers are referenced throughout the remaining chapter. Figure 2 shows the pin locations from the top view. In contrast, Figure 3 shows the pin locations from the bottom view.

Figure 2 Pin Locations (Top View)

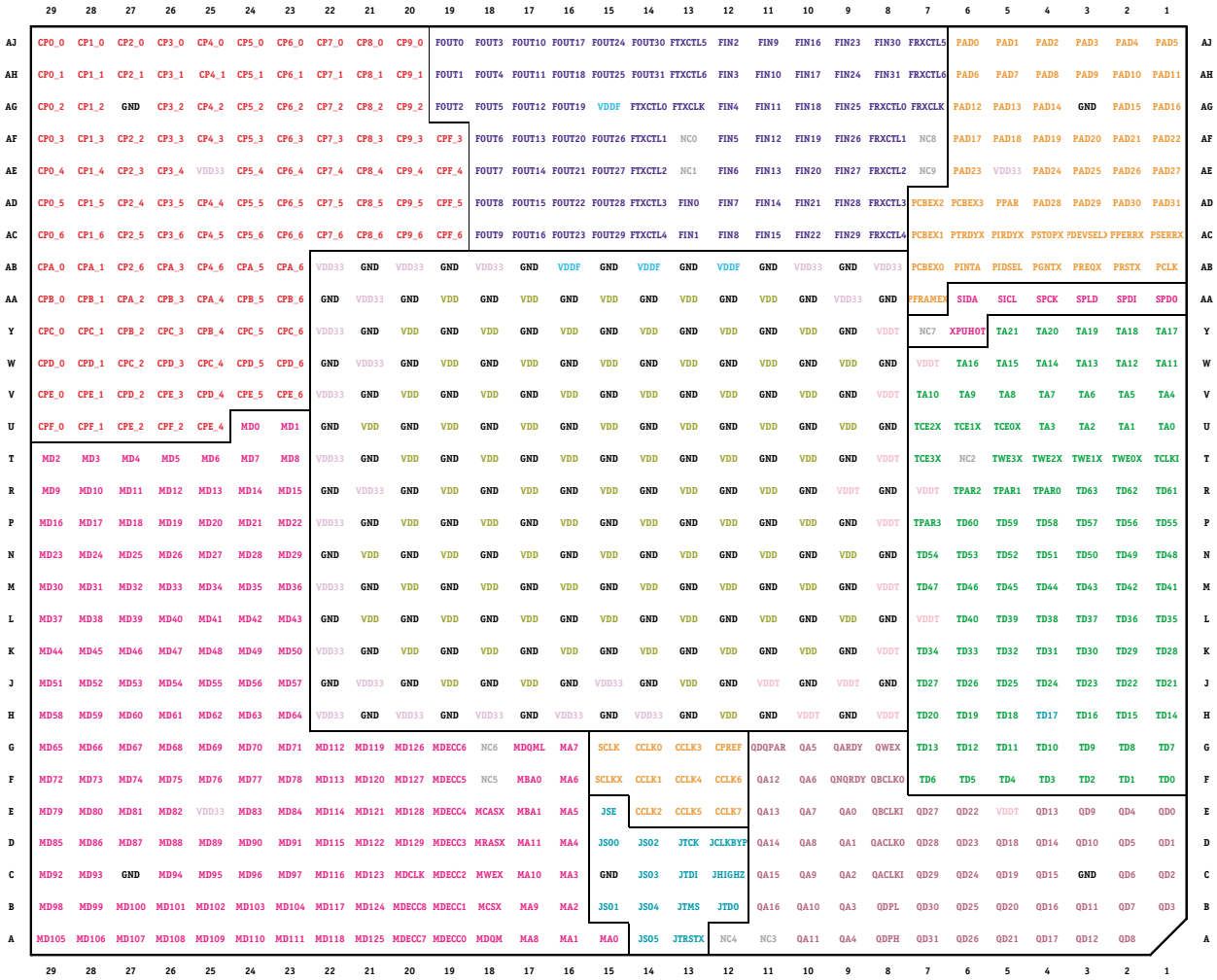
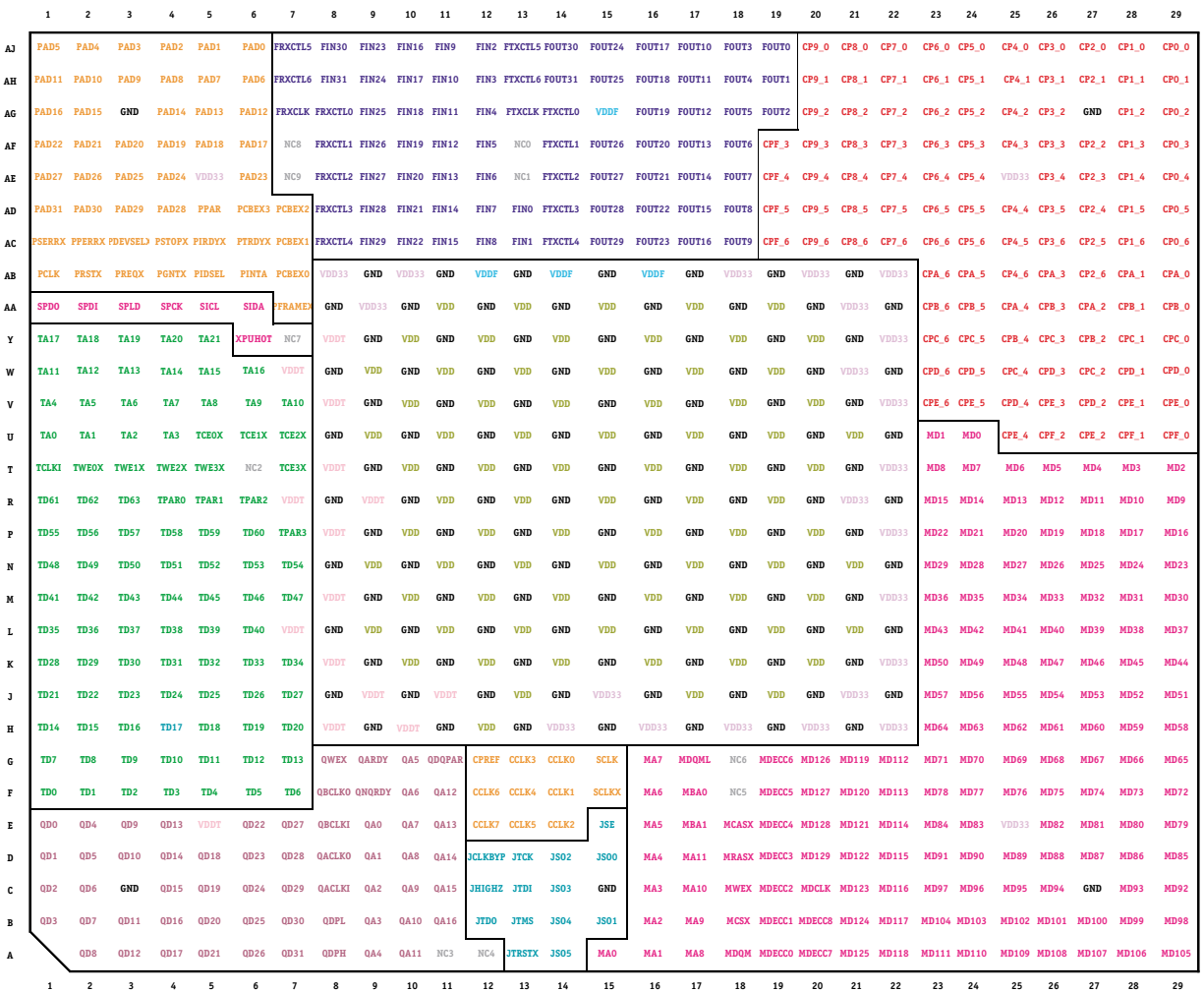


Figure 3 Pin Locations (Bottom View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AJ	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0	FRXCTL5	FIN30	FIN23	FIN16	FIN9	FIN2	FTXCTL5	FOUT30	FOUT24	FOUT17	FOUT10	FOUT3	FOUT0	CP9_0	CP8_0	CP7_0	CP6_0	CP5_0	CP4_0	CP3_0	CP2_0	CP1_0	CP0_0	AJ
AH	PAD11	PAD10	PAD9	PAD8	PAD7	PAD6	FRXCTL6	FIN31	FIN24	FIN17	FIN10	FIN3	FTXCTL6	FOUT31	FOUT25	FOUT18	FOUT11	FOUT4	FOUT1	CP9_1	CP8_1	CP7_1	CP6_1	CP5_1	CP4_1	CP3_1	CP2_1	CP1_1	CP0_1	AH
AG	PAD16	PAD15	GND	PAD14	PAD13	PAD12	FRXCLK	FRXCTL0	FIN25	FIN18	FIN11	FIN4	FTXCLK	FTXCTL0	VDDF	FOUT19	FOUT12	FOUT5	FOUT2	CP9_2	CP8_2	CP7_2	CP6_2	CP5_2	CP4_2	CP3_2	GND	CP1_2	CP0_2	AG
AF	PAD22	PAD21	PAD20	PAD19	PAD18	PAD17	NC8	FRXCTL1	FIN26	FIN19	FIN12	FIN5	NC0	FTXCTL1	FOUT26	FOUT20	FOUT13	FOUT6	CP_3	CP9_3	CP8_3	CP7_3	CP6_3	CP5_3	CP4_3	CP3_3	CP2_2	CP1_3	CP0_3	AF
AE	PAD27	PAD26	PAD25	PAD24	VDD33	PAD23	NC9	FRXCTL2	FIN27	FIN20	FIN13	FIN6	NC1	FTXCTL2	FOUT27	FOUT21	FOUT14	FOUT7	CP_4	CP9_4	CP8_4	CP7_4	CP6_4	CP5_4	VDD33	CP3_4	CP2_3	CP1_4	CP0_4	AE
AD	PAD31	PAD30	PAD29	PAD28	PPAR	PCBEX3	PCBEX2	FRXCTL3	FIN28	FIN21	FIN14	FIN7	FIN0	FTXCTL3	FOUT28	FOUT22	FOUT15	FOUT8	CP_5	CP9_5	CP8_5	CP7_5	CP6_5	CP5_5	CP4_4	CP3_5	CP2_4	CP1_5	CP0_5	AD
AC	PSERRX	PPERRX	PDEVSEL	PSTOPX	PIRDYX	PTRDYX	PCBEX1	FRXCTL4	FIN29	FIN22	FIN15	FIN8	FIN1	FTXCTL4	FOUT29	FOUT23	FOUT16	FOUT9	CP_6	CP9_6	CP8_6	CP7_6	CP6_6	CP5_6	CP4_5	CP3_6	CP2_5	CP1_6	CP0_6	AC
AB	PCLK	PRSTX	PREQX	PGNTX	PIDSEL	PINTA	PCBEX0	VDD33	GND	VDD33	GND	VDDF	GND	VDDF	GND	VDDF	GND	VDD33	GND	VDD33	GND	VDD33	CPA_6	CPA_5	CP4_6	CPA_3	CP2_6	CPA_1	CPA_0	AB
AA	SPDO	SPDI	SPLD	SPCK	SICL	SIDA	PFRAMEX	GND	VDD33	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	GND	CPB_6	CPB_5	CPA_4	CPB_3	CPA_2	CPB_1	CPB_0	AA
Y	TA17	TA18	TA19	TA20	TA21	XPUHOT	NC7	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	CPC_6	CPC_5	CPB_4	CPC_3	CPB_2	CPC_1	CPC_0	Y
W	TA11	TA12	TA13	TA14	TA15	TA16	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	GND	CPD_6	CPD_5	CPC_4	CPD_3	CPC_2	CPD_1	CPD_0	W
V	TA4	TA5	TA6	TA7	TA8	TA9	TA10	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	CPE_6	CPE_5	CPD_4	CPE_3	CPD_2	CPE_1	CPE_0	V
U	TA0	TA1	TA2	TA3	TCE0X	TCE1X	TCE2X	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD1	MD0	CPE_4	CPE_2	CPE_2	CPF_1	CPF_0	U
T	TCLKI	TWE0X	TWE1X	TWE2X	TWE3X	NC2	TCE3X	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD8	MD7	MD6	MD5	MD4	MD3	MD2	T
R	TD61	TD62	TD63	TPAR0	TPAR1	TPAR2	VDDT	GND	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	GND	MD15	MD14	MD13	MD12	MD11	MD10	MD9	R
P	TD55	TD56	TD57	TD58	TD59	TD60	TPAR3	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD22	MD21	MD20	MD19	MD18	MD17	MD16	P
N	TD48	TD49	TD50	TD51	TD52	TD53	TD54	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD29	MD28	MD27	MD26	MD25	MD24	MD23	N
M	TD41	TD42	TD43	TD44	TD45	TD46	TD47	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD36	MD35	MD34	MD33	MD32	MD31	MD30	M
L	TD35	TD36	TD37	TD38	TD39	TD40	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	MD43	MD42	MD41	MD40	MD39	MD38	MD37	L
K	TD28	TD29	TD30	TD31	TD32	TD33	TD34	VDDT	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD33	MD50	MD49	MD48	MD47	MD46	MD45	MD44	K
J	TD21	TD22	TD23	TD24	TD25	TD26	TD27	GND	VDDT	GND	VDDT	GND	VDD	GND	VDD33	GND	VDD	GND	VDD	GND	VDD33	GND	MD57	MD56	MD55	MD54	MD53	MD52	MD51	J
H	TD14	TD15	TD16	TD17	TD18	TD19	TD20	VDDT	GND	VDDT	GND	VDD	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	GND	VDD33	MD64	MD63	MD62	MD61	MD60	MD59	MD58	H
G	TD7	TD8	TD9	TD10	TD11	TD12	TD13	QWEX	QARDY	QA5	QDQPAR	CPREF	CCLK3	CCLK0	SCLK	MA7	MDQML	NC6	MDECC6	MD126	MD119	MD112	MD71	MD70	MD69	MD68	MD67	MD66	MD65	G
F	TD0	TD1	TD2	TD3	TD4	TD5	TD6	QBCLKO	QNQRDY	QA6	QA12	CCLK6	CCLK4	CCLK1	SCLKX	MA6	MBA0	NC5	MDECC5	MD127	MD120	MD113	MD78	MD77	MD76	MD75	MD74	MD73	MD72	F
E	QD0	QD4	QD9	QD13	VDDT	QD22	QD27	QBCLKI	QA0	QA7	QA13	CCLK7	CCLK5	CCLK2	JSE	MA5	MBA1	MCASX	MDECC4	MD128	MD121	MD114	MD84	MD83	VDD33	MD82	MD81	MD80	MD79	E
D	QD1	QD5	QD10	QD14	QD18	QD23	QD28	QACLKO	QA1	QA8	QA14	JCLKBYP	JTCK	JSO2	JSO0	MA4	MA11	MRASX	MDECC3	MD129	MD122	MD115	MD91	MD90	MD89	MD88	MD87	MD86	MD85	D
C	QD2	QD6	GND	QD15	QD19	QD24	QD29	QACLKI	QA2	QA9	QA15	JHIGHZ	JTDI	JSO3	GND	MA3	MA10	MWEX	MDECC2	MDCLK	MD123	MD116	MD97	MD96	MD95	MD94	GND	MD93	MD92	C
B	QD3	QD7	QD11	QD16	QD20	QD25	QD30	QDPL	QA3	QA10	QA16	JTDO	JTMS	JSO4	JSO1	MA2	MA9	MCSX	MDECC1	MDECC8	MD124	MD117	MD104	MD103	MD102	MD101	MD100	MD99	MD98	B
A		QD8	QD12	QD17	QD21	QD26	QD31	QDPH	QA4	QA11	NC3	NC4	JTRSTX	JSO5	MA0	MA1	MA8	MDQM	MDECC0	MDECC7	MD125	MD118	MD111	MD110	MD109	MD108	MD107	MD106	MD105	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Pin Descriptions Grouped by Function

The C-5e NP pins are categorized in groups, reflecting interfaces to the chip:

- Clock Signals
- CP Interface Signals
- Executive Processor System Interface Signals
- Fabric Processor Interface Signals
- BMU SDRAM Interface Signals
- TLU SRAM Interface Signals
- QMU SRAM (Internal Mode) Interface Signals
- QMU to Q-5 (External Mode) Interface Signals
- Power Supply Signals
- Test Signals
- No Connection Pins

LVTTL and LVPECL Specifications

C-5e NP pins are the following types:

- Low Voltage TTL-Compatible (LVTTL). The C-5e NP's LVTTL pins conform to the JEDEC JESD8-B specification.
- Low Voltage Positive Emitter Coupled Logic (LVPECL).

All of the signals in the following tables in this chapter denote whether the individual signal is an Input (I), Output (O), both Input and Output (I/O), or power (P). In addition, a PU, PD , and nc are used . The PU indicates that an internal resistor will pullup the pad if left unconnected. PD indicates an internal pulldown resistor. NC means the pad is to be left unconnected.

Clock Signals

Table 5 describes the C-5e NP clock signals.

Table 5 Clock and Reference Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
SCLK* SCLKX*	G15 F15	1 1	LVPECL LVPECL	I I	Core Clock Rate (Differential)
CCLK0	G14	1	LVTTL	I_{PD}	1_544MHZ_CLK (T1)†
CCLK1	F14	1	LVTTL	I_{PD}	2_048MHZ_CLK (E1)†
CCLK2	E14	1	LVTTL	I_{PD}	34_368MHZ_CLK (E3)†
CCLK3	G13	1	LVTTL	I_{PD}	44_736MHZ_CLK (T3)†
CCLK4	F13	1	LVTTL	I_{PD}	50MHZ_CLK (100Mbit Ethernet)†
CCLK5	E13	1	LVTTL	I_{PD}	106_25MHZ_CLK (Fibre Channel)†
CCLK6	F12	1	LVTTL	I_{PD}	125MHZ_CLK (Gigabit Ethernet)†
CCLK7	E12	1	LVTTL	I_{PD}	155_52MHZ_CLK (OC-3)†
CPREF‡	G12	1	LVPECL	I_{PD}	Reference
TOTAL		**11**			

* SCLK and SCLKX must not be AC-coupled.

† The frequencies specified for CCLK0 - CCLK7 allow full flexibility for the C-5e NP. It is also possible to use one or more CCLK*n* inputs for other frequencies. Contact your Motorola representative for more information.

‡ If any of the CPs are configured for LVPECL operation (OC3) using the pin mode registers, then CPREF must be wired to an external reference, as specified in Table 37 on page 77. If none of the CPs are configured for LVPECL operation, then the CPREF pin can be left unconnected.

CP Interface Signals

The C-5e NP's 16 CPs support various network physical interfaces, providing a serial interface to the PHY layer. Interfaces are configured via bits in the C-5e NP register set. Many interfaces are possible by programming the configuration registers. CPs can be used individually or in a cluster (four CPs) to implement the various interfaces.

Table 6 provides a quick reference of all the CP pins organized by clusters. There are seven physical I/O pins associated with each CP. All pins are capable of receiving data, with some configurable to be input clocks, output clocks, or data drivers. In addition, pairs of pins can be configured as differential pairs for LVPECL compatibility.

In the case of RMII, OC-3, DS1, and DS3, the drivers and receivers at the pin are locally configured to match the relevant PHY or Framer chip. OC-12 uses the aggregation of four CPs (one cluster), while GMII and Ten Bit Interface (TBI) can use either eight CPs (four for receive and four for transmit) or four CPs that share the transmit and receive functions for non-wire speed applications.

During CP aggregation, all 28 pins associated with a cluster are routed to all of the Serial Data Processors (SDPs) in that cluster. This allows round-robin usage of portions of the SDPs, with each getting access to the necessary I/O pins.

The signals for the following CP physical interfaces are included in this section:

- DS1/T1 Framer Interface Configuration
- 10/100 Ethernet (RMII) Configuration
- Gigabit Ethernet (GMII) Configuration
- Gigabit Ethernet and Fibre Channel TBI Configuration
- SONET OC-3 Transceiver Interface Configuration
- SONET OC-12 Transceiver Interface Configuration

Table 6 CP Physical Interface Signals and Pins (Grouped by Clusters)

CP CLUSTER 1		CP CLUSTER 2		CP CLUSTER 3		CP CLUSTER 4	
SIGNAL	**PIN #**	**SIGNAL**	**PIN #**	**SIGNAL**	**PIN #**	**SIGNAL**	**PIN #**
CP0_0	AJ29	CP4_0	AJ25	CP8_0	AJ21	CPC_0	Y29
CP0_1	AH29	CP4_1	AH25	CP8_1	AH21	CPC_1	Y28
CP0_2	AG29	CP4_2	AG25	CP8_2	AG21	CPC_2	W27
CP0_3	AF29	CP4_3	AF25	CP8_3	AF21	CPC_3	Y26
CP0_4	AE29	CP4_4	AD25	CP8_4	AE21	CPC_4	W25
CP0_5	AD29	CP4_5	AC25	CP8_5	AD21	CPC_5	Y24
CP0_6	AC29	CP4_6	AB25	CP8_6	AC21	CPC_6	Y23
CP1_0	AJ28	CP5_0	AJ24	CP9_0	AJ20	CPD_0	W29
CP1_1	AH28	CP5_1	AH24	CP9_1	AH20	CPD_1	W28
CP1_2	AG28	CP5_2	AG24	CP9_2	AG20	CPD_2	V27
CP1_3	AF28	CP5_3	AF24	CP9_3	AF20	CPD_3	W26
CP1_4	AE28	CP5_4	AE24	CP9_4	AE20	CPD_4	V25
CP1_5	AD28	CP5_5	AD24	CP9_5	AD20	CPD_5	W24
CP1_6	AC28	CP5_6	AC24	CP9_6	AC20	CPD_6	W23
CP2_0	AJ27	CP6_0	AJ23	CPA_0	AB29	CPE_0	V29
CP2_1	AH27	CP6_1	AH23	CPA_1	AB28	CPE_1	V28
CP2_2	AF27	CP6_2	AG23	CPA_2	AA27	CPE_2	U27
CP2_3	AE27	CP6_3	AF23	CPA_3	AB26	CPE_3	V26
CP2_4	AD27	CP6_4	AE23	CPA_4	AA25	CPE_4	U25
CP2_5	AC27	CP6_5	AD23	CPA_5	AB24	CPE_5	V24
CP2_6	AB27	CP6_6	AC23	CPA_6	AB23	CPE_6	V23
CP3_0	AJ26	CP7_0	AJ22	CPB_0	AA29	CPF_0	U29
CP3_1	AH26	CP7_1	AH22	CPB_1	AA28	CPF_1	U28
CP3_2	AG26	CP7_2	AG22	CPB_2	Y27	CPF_2	U26
CP3_3	AF26	CP7_3	AF22	CPB_3	AA26	CPF_3	AF19
CP3_4	AE26	CP7_4	AE22	CPB_4	Y25	CPF_4	AE19

Table 6 CP Physical Interface Signals and Pins (Grouped by Clusters) (continued)

CP CLUSTER 1		CP CLUSTER 2		CP CLUSTER 3		CP CLUSTER 4	
SIGNAL	**PIN #**	**SIGNAL**	**PIN #**	**SIGNAL**	**PIN #**	**SIGNAL**	**PIN #**
CP3_5	AD26	CP7_5	AD22	CPB_5	AA24	CPF_5	AD19
CP3_6	AC26	CP7_6	AC22	CPB_6	AA23	CPF_6	AC19

DS1/T1 Framer Interface Configuration

Table 7 describes the serial framer interface signals. For each CP (0-15), you can implement one serial Framer interface.

Table 7 DS1/T1 Framer Interface Signals

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 6	1	LVTTL	O_{PD}	TCLK	Transmit Clock (1.544MHz)
CP*n*_1	Table 6	1	LVTTL	I_{PU}	RCLK	Receive Clock (1.544MHz)
CP*n*_2	Table 6	1	LVTTL	O_{PD}	TData	Transmit Data
CP*n*_3	Table 6	1	LVTTL	O_{PU}	TFrame	Transmit Frame Synchronization
CP*n*_4	Table 6	1	LVTTL	I_{PD}	RData	Receive Data
CP*n*_5	Table 6	1	LVTTL	I_{PU}	RFrame	Receive Frame Synchronization
CP*n*_6	Table 6	1	nc	nc_{PU}	nc	nc
TOTAL PINS		**7**				

* *n* can be from 0 to 15. See Table 6.

† Reference Table 6 for pin numbers for the actual cluster(s) you are configuring.

10/100 Ethernet (RMII) Configuration

Table 8 describes the 10/100BASE-T Ethernet Reduced Media Independent Interface (RMII) signals. For each CP (0-15), you can implement one 10/100 Ethernet interface.

Table 8 10/100 Ethernet Signals

SIGNAL NAME*	PIN #	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 6	1	LVTTL	O_{PD}	REF_CLK	Transmit and Receive Clock (50MHz)
CP*n*_1	Table 6	1	LVTTL	I_{PU}	CRS_DV	Carrier Sense (CRS)/ Receive Data Valid (RX_DV). CRS indicates that traffic is on the link, and is asserted if the signal is a 1 or an alternating 1010... RX_DV indicates that a receive frame is in progress and the data present on the RXD pins is valid. It is asserted if this signal is a 1 for more than one cycle.
CP*n*_2	Table 6	1	LVTTL	O_{PD}	TXD(0)	Transmit Data 0 (first on wire)
CP*n*_3	Table 6	1	LVTTL	O_{PU}	TXD(1)	Transmit Data 1 (second on wire)
CP*n*_4	Table 6	1	LVTTL	I_{PD}	RXD(0)	Receive Data 0 (first on wire)
CP*n*_5	Table 6	1	LVTTL	I_{PU}	RXD(1)	Receive Data 1 (second on wire)
CP*n*_6	Table 6	1	LVTTL	O_{PU}	TX_EN	Transmit Enable. When asserted, the data on TXD is encoded and transmitted on the twisted pair cable.
TOTAL PINS		**7**				

* *n* can be from 0 to 15. See Table 6.

Gigabit Ethernet (GMII) Configuration

Gigabit Ethernet Media Independent Interface (GMII) is configured in one of two ways:

- Use one CP cluster when density is more important than wire-speed performance because you can then implement up to four Gigabit Ethernet ports per C-5e NP.
- Use two CP clusters for wire-speed performance and additional processing power. You can implement up to two Gigabit Ethernet ports per C-5e NP.

Table 9 lists the possible CP cluster combinations you can use and Figure 4 shows receive and transmit pin configurations by cluster. Table 10 lists the signals and pinouts for Gigabit Ethernet (GMII).

Table 9 Transmit and Receive Pin Combinations for Gigabit Ethernet and Fibre Channel

CLUSTER	SINGLE CLUSTER MODE (TBI OR GMII)	TWO CLUSTER MODE (GMII)*
0	Port 1 Tx and Rx	Port 1 Tx
1	Port 2 Tx and Rx	Port 1 Rx
2	Port 3 Tx and Rx	Port 2 Tx
3	Port 4 Tx and Rx	Port 2 Rx

* The Two Cluster Mode column lists typical configurations. Any cluster can be set up to either receive or transmit. So you could configure a dual cluster mode where cluster 0 receives and cluster 3 transmits.

Figure 4 GMII/TBI Transmit and Receive Pin Configurations

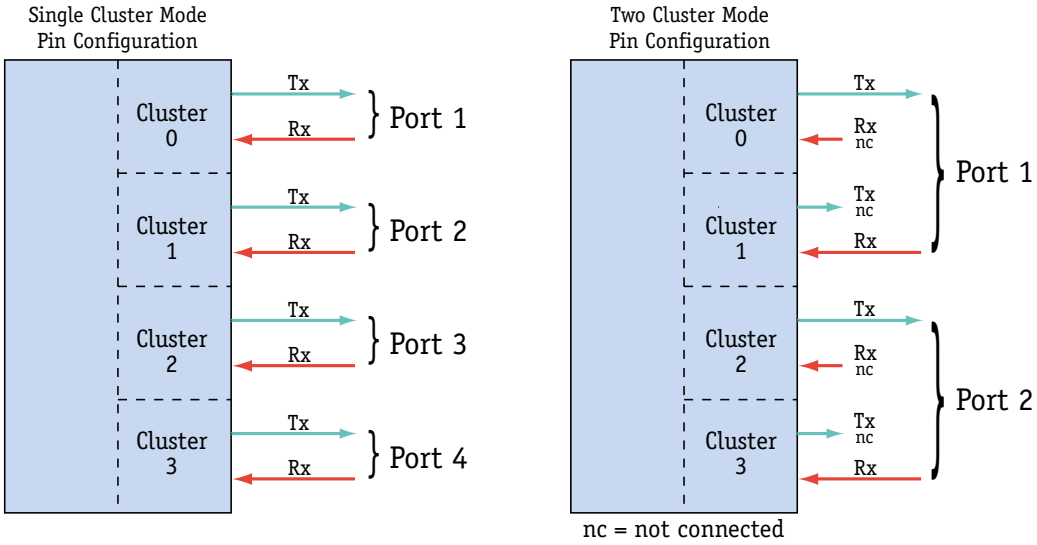


Table 10 Gigabit Ethernet (GMII/MII) Signals One Cluster Example

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 6	1	LVTTL	O_{PD}	T_CLK	GMII Transmit Clock (125MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 6	1	LVTTL	I_{PU}	TCLKI	MII transmit clock. Transmit data aligned to this clock input from phy in MII mode. 25 Mhz in 100BaseT, 2.5 in Mhz in 10BaseT
CP*n*_2	Table 6	1	LVTTL	O_{PD}	TXD(0)	Transmit Data (byte-wide data, least significant bit)
CP*n*_3	Table 6	1	LVTTL	O_{PU}	TXD(1)	Transmit Data
CP*n*_4	Table 6	1	LVTTL	O_{PD}	TXD(2)	Transmit Data
CP*n*_5	Table 6	1	LVTTL	O_{PU}	TXD(3)	Transmit Data
CP*n*_6	Table 6	1	LVTTL	O_{PU}	TX_EN	Transmit Enable. When asserted, the data on TXD is encoded and transmitted on the twisted pair cable.
CP*n+1*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+1*_1	Table 6	1	LVTTL	I_{PU}	COL	Collision. Asserted when both RX_DV and TX_EN are valid during half duplex operation.

Table 10 Gigabit Ethernet (GMII/MII) Signals One Cluster Example (continued)

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n+1*_2	Table 6	1	LVTTL	O_{PD}	TXD(4)	Transmit Data
CP*n+1*_3	Table 6	1	LVTTL	O_{PU}	TXD(5)	Transmit Data
CP*n+1*_4	Table 6	1	LVTTL	O_{PD}	TXD(6)	Transmit Data
CP*n+1*_5	Table 6	1	LVTTL	O_{PU}	TXD(7)	Transmit Data (byte-wide receive data, most significant bit)
CP*n+1*_6	Table 6	1	LVTTL	O_{PU}	TX_ER	Transmit Error. Asserting TX_ER when TX_EN is a 1 causes transmission of the designated "bad code" in lieu of the normal encoded data on the twisted pair data.
CP*n+2*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+2*_1	Table 6	1	LVTTL	I_{PU}	RCLK	Receive Clock (125MHz)
CP*n+2*_2	Table 6	1	LVTTL	I_{PD}	RXD(0)	Receive Data (byte-wide receive data, least significant bit)
CP*n+2*_3	Table 6	1	LVTTL	I_{PU}	RXD(1)	Receive Data
CP*n+2*_4	Table 6	1	LVTTL	I_{PD}	RXD(2)	Receive Data
CP*n+2*_5	Table 6	1	LVTTL	I_{PU}	RXD(3)	Receive Data
CP*n+2*_6	Table 6	1	LVTTL	I_{PU}	RX_DV	Receive Data Valid. Indicates that there is a receive frame in progress and that the data present on the RXD signals is valid.
CP*n+3*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+3*_1	Table 6	1	LVTTL	I_{PU}	CRS	Carrier Sense. Indicates traffic is on the link. CRS is asserted when a non-idle condition is detected on the receive data stream. CRS is deasserted when an end of frame or idle condition is detected.
CP*n+3*_2	Table 6	1	LVTTL	I_{PD}	RXD(4)	Receive Data
CP*n+3*_3	Table 6	1	LVTTL	I_{PU}	RXD(5)	Receive Data
CP*n+3*_4	Table 6	1	LVTTL	I_{PD}	RXD(6)	Receive Data
CP*n+3*_5	Table 6	1	LVTTL	I_{PU}	RXD(7)	Receive Data (most significant bit)
CP*n+3*_6	Table 6	1	LVTTL	I_{PU}	RX_ER	Receive Error Detected. Indicates that there has been an error received in the receive frame.
TOTAL PINS		**28**				

* n can be 0, 4, 8, or 12.

† Reference Table 6 for pin numbers for the actual cluster(s) you are configuring.

Gigabit Ethernet and Fibre Channel TBI Configuration

1000BASE-T Gigabit Ethernet and Fibre Channel TBI is implemented in much the same way as Gigabit Ethernet (GMII). Table 9 shows the possible CP pin combinations you can use and Figure 4 shows receive and transmit pin configurations by cluster. Table 11 shows the signals and pinouts for a single cluster for Gigabit Ethernet and Fibre Channel TBI.

The unused pins for the two cluster configurations should be wired down using a resistor.

Table 11 Gigabit Ethernet and Fibre Channel TBI Signals Example

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 6	1	LVTTL	O_{PD}	TCLK	Transmit Clock (125MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 6	1	nc	nc_{PU}	nc	nc
CP*n*_2	Table 6	1	LVTTL	O_{PD}	TXD(9)	Transmit Data (ten bits wide, last on wire)
CP*n*_3	Table 6	1	LVTTL	O_{PU}	TXD(8)	Transmit Data
CP*n*_4	Table 6	1	LVTTL	O_{PD}	TXD(7)	Transmit Data
CP*n*_5	Table 6	1	LVTTL	O_{PU}	TXD(6)	Transmit Data
CP*n*_6	Table 6	1	LVTTL	O_{PU}	TXD(1)	Transmit Data
CP*n+1*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+1*_1	Table 6	1	nc	nc_{PU}	nc	nc
CP*n+1*_2	Table 6	1	LVTTL	O_{PD}	TXD(5)	Transmit Data
CP*n+1*_3	Table 6	1	LVTTL	O_{PU}	TXD(4)	Transmit Data
CP*n+1*_4	Table 6	1	LVTTL	O_{PD}	TXD(3)	Transmit Data
CP*n+1*_5	Table 6	1	LVTTL	O_{PU}	TXD(2)	Transmit Data
CP*n+1*_6	Table 6	1	LVTTL	O_{PU}	TXD(0)	Transmit Data (ten bits wide, first on wire)
CP*n+2*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+2*_1	Table 6	1	LVTTL	I_{PU}	RCLK	Receive Clock (62.5 MHz)
CP*n+2*_2	Table 6	1	LVTTL	I_{PD}	RXD(9)	Receive Data (ten bits wide, last on wire)
CP*n+2*_3	Table 6	1	LVTTL	I_{PU}	RXD(8)	Receive Data
CP*n+2*_4	Table 6	1	LVTTL	I_{PD}	RXD(7)	Receive Data
CP*n+2*_5	Table 6	1	LVTTL	I_{PU}	RXD(6)	Receive Data
CP*n+2*_6	Table 6	1	LVTTL	I_{PU}	RXD(1)	Receive Data
CP*n+3*_0	Table 6	1	nc	nc_{PD}	nc	nc

Table 11 Gigabit Ethernet and Fibre Channel TBI Signals Example (continued)

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n+3*_1	Table 6	1	LVTTL	I_{PU}	RCLKN	Receive Clock Inverted
CP*n+3*_2	Table 6	1	LVTTL	I_{PD}	RXD(5)	Receive Data
CP*n+3*_3	Table 6	1	LVTTL	I_{PU}	RXD(4)	Receive Data
CP*n+3*_4	Table 6	1	LVTTL	I_{PD}	RXD(3)	Receive Data
CP*n+3*_5	Table 6	1	LVTTL	I_{PU}	RXD(2)	Receive Data
CP*n+3*_6	Table 6	1	LVTTL	I_{PU}	RXD(0)	Receive Data (ten bits wide, first on wire)
TOTAL PINS		**28**				

* n can be 0, 4, 8, or 12

† Reference Table 6 for pin numbers for the actual cluster(s) you are configuring.

SONET OC-3 Transceiver Interface Configuration

Table 12 describes the SONET Optical Carrier (OC) 3 transceiver interface signals. For each CP (0-15), you can implement a single OC-3 interface.

Table 12 OC-3 Signals

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 6	1	LVPECL	I_{PD}	RCLK_H	Receive Clock noninverted side of pair (155.52MHz)
CP*n*_1	Table 6	1	LVPECL	I_{PU}	RCLK_L	Receive Clock inverted side of pair (155.52MHz)
CP*n*_2	Table 6	1	LVPECL	O_{PD}	TXD_H	Transmit Data noninverted side of pair
CP*n*_3	Table 6	1	LVPECL	I_{PU}	TXD_L	Transmit Data inverted side of pair
CP*n*_4	Table 6	1	LVPECL	I_{PD}	RXD_H	Receive Data noninverted side of pair
CP*n*_5	Table 6	1	LVPECL	I_{PU}	RXD_L	Receive Data inverted side of pair
CP*n*_6	Table 6	1	LVPECL	I_{PU}	SIGNAL_DET	A light level above a certain threshold is present at the optical receiver - single ended LVPECL.
TOTAL PINS		**7**				

* *n* can be from 0 to 15.

† Reference Table 6 for pin numbers for the actual cluster(s) you are configuring.

SONET OC-12 Transceiver Interface Configuration

SONET Optical Carrier (OC) 12 is implemented by using one cluster of CPs. At any time, a CP within a cluster spends half its time performing receive functions, and the other half performing transmit functions. Table 13 shows a CP Cluster configured for one OC-12 interface.

Table 13 OC-12 Signals Example

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n*_0	Table 6	1	LVTTL	O_{PD}	TCLK	Deskewed Transmit Clock (77.76MHz). This clock is used to synchronize the transmit data.
CP*n*_1	Table 6	1	LVTTL	I_{PU}	TCLKI	Transceiver Transmit Clock. This clock sets the frequency of the transmit data and is typically sourced by the PHY chip.
CP*n*_2	Table 6	1	LVTTL	O_{PD}	TXD(0)	Transmit Data (byte-wide data, least significant bit)
CP*n*_3	Table 6	1	LVTTL	O_{PU}	TXD(1)	Transmit Data
CP*n*_4	Table 6	1	LVTTL	O_{PD}	TXD(2)	Transmit Data
CP*n*_5	Table 6	1	LVTTL	O_{PU}	TXD(3)	Transmit Data
CP*n*_6	Table 6	1	LVTTL	O_{PU}	00F	Out of Frame
CP*n+1*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+1*_1	Table 6	1	nc	nc_{PU}	nc	nc
CP*n+1*_2	Table 6	1	LVTTL	O_{PD}	TXD(4)	Transmit Data
CP*n+1*_3	Table 6	1	LVTTL	O_{PU}	TXD(5)	Transmit Data
CP*n+1*_4	Table 6	1	LVTTL	O_{PD}	TXD(6)	Transmit Data
CP*n+1*_5	Table 6	1	LVTTL	O_{PU}	TXD(7)	Transmit Data (byte-wide data, most significant bit)
CP*n+1*_6	Table 6	1	nc	nc_{PU}	nc	nc
CP*n+2*_0	Table 6	1	nc	nc_{PD}	nc	nc
CP*n+2*_1	Table 6	1	LVTTL	I_{PU}	RCLK	Receive Clock (77.76MHz)
CP*n+2*_2	Table 6	1	LVTTL	I_{PD}	RXD(0)	Receive Data (byte-wide receive data, least significant bit)
CP*n+2*_3	Table 6	1	LVTTL	I_{PU}	RXD(1)	Receive Data
CP*n+2*_4	Table 6	1	LVTTL	I_{PD}	RXD(2)	Receive Data
CP*n+2*_5	Table 6	1	LVTTL	I_{PU}	RXD(3)	Receive Data
CP*n+2*_6	Table 6	1	LVTTL	I_{PU}	FP	Frame Synchronization Pulse. This is valid during the third A2 of the receive SONET frame.
CP*n+3*_0	Table 6	1	nc	nc_{PD}	nc	nc

Table 13 OC-12 Signals Example (continued)

SIGNAL NAME*	PIN #†	TOTAL	TYPE	I/O	LABEL	SIGNAL DESCRIPTION
CP*n+3*_1	Table 6	1	nc	nc_{PU}	nc	nc
CP*n+3*_2	Table 6	1	LVTTL	I_{PD}	RXD(4)	Receive Data
CP*n+3*_3	Table 6	1	LVTTL	I_{PU}	RXD(5)	Receive Data
CP*n+3*_4	Table 6	1	LVTTL	I_{PD}	RXD(6)	Receive Data
CP*n+3*_5	Table 6	1	LVTTL	I_{PU}	RXD(7)	Receive Data (most significant bit)
CP*n+3*_6	Table 6	1	nc	nc_{PU}	nc	nc
TOTAL PINS		**28**				

* n can be 0, 4, 8, or 12

† Reference Table 6 for pin numbers for a different cluster.

Executive Processor System Interface Signals

The XP's system interface manages the supervisory controls for the network interfaces, as well as the set of pins that provide interfaces to other components in the system that are not memories or network interfaces. It is also the primary interface used for initializing the C-5e NP after reset. The XP signals include PCI signals, Serial interface signals, and PROM interface signals.

PCI Signals

The PCI can be configured to support a 32bit PCI capable of operating at either 33MHz or 66MHz. The PCI is fully compliant with PCI Specification revision 2.1. Table 14 describes the PCI signals.

Table 14 PCI Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
PAD0 - PAD31	AJ6, AJ5, AJ4, AJ3, AJ2, AJ1, AH6, AH5, AH4, AH3, AH2, AH1, AG6, AG5, AG4, AG2, AG1, AF6, AF5, AF4, AF3, AF2, AF1, AE6, AE4, AE3, AE2, AE1, AD4, AD3, AD2, AD1	32	PCI	I/O	Multiplexed Address/Data Bus. These signals are multiplexed address and data bits. The C-5e NP receives addresses as target and drives addresses as master. It drives the data and receives read data as master.
PCBEX0 - PCBEX3	AB7, AC7, AD7, AD6	4	PCI	I/O	Command byte enables. These signals are multiplexed command and byte enabled signals. The C-5e NP receives byte enables as target and drives byte enables as master.
PPAR	AD5	1	PCI	I/O	Parity. This signal carries even parity for AD and CBE# pins. It has the same receive and drive characteristics as the address and data bus, except that it is one PCI cycle later.
PFRAMEX	AA7	1	PCI	I/O	Cycle frame
PTRDYX	AC6	1	PCI	I/O	Target ready for data transfer
PIRDYX	AC5	1	PCI	I/O	Initiator ready for data transfer
PSTOPX	AC4	1	PCI	I/O	Target transaction stop request
PDEVSELX	AC3	1	PCI	I/O	Target device selected
PPERRX	AC2	1	PCI	I/O	Bus parity error
PSERRX	AC1	1	PCI	I/O	System error
PCLK	AB1	1	I_{PD}	I	Bus clock
PRSTX	AB2	1	PCI	I	Bus reset
PREQX	AB3	1	PCI	O	Initiator bus request (arbitration)

Table 14 PCI Signals (continued)

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
PGNTX	AB4	1	I_{PD}	I	Initiator bus grant (arbitration)
PIDSEL	AB5	1	PCI	I	Initialization device select
PINTA	AB6	1	PCI	O	Interrupt
TOTAL PINS		**50**			

Serial Interface Signals

The Serial interface is a bidirectional two-wire serial bus. It can use one of the following formats:

- An 8bit data format followed by an acknowledge bit, which supports transfers at up to 400kbps (low speed).
- a 16bit IEEE 802.3 MDIO data format with 10bits of addressing, which supports transfers up to 25MHz (high speed).

The signals and pins are identical for both the high and low speed protocols.

Which of the two data rates used is selected by the state of the PROM interface's SPLD signal that is asserted while the PROM interface is idle. When SPLD is asserted HI *the low speed serial bus protocol is selected and when SPLD is asserted* LOW *the MDIO protocol is selected.*

The bus only supports a single master hierarchy that can operate as either a receiver or a transmitter.

Both SIDA and SICL are bidirectional lines that are connected, through a pull-up resistor, to a positive supply voltage. When the bus is free, both lines are HIGH. The output stages of the devices connected to the bus must have either an open-drain or open-collector in order to perform the wired-AND function required for its arbitration mechanism.

Table 15 Serial Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
SICL	AA5	1	LVTTL	I_{PD}/O	Serial Clock line
SIDA	AA6	1	LVTTL	I_{PD}/O	Serial Data line
TOTAL PINS		**2**			

PROM Interface Signals

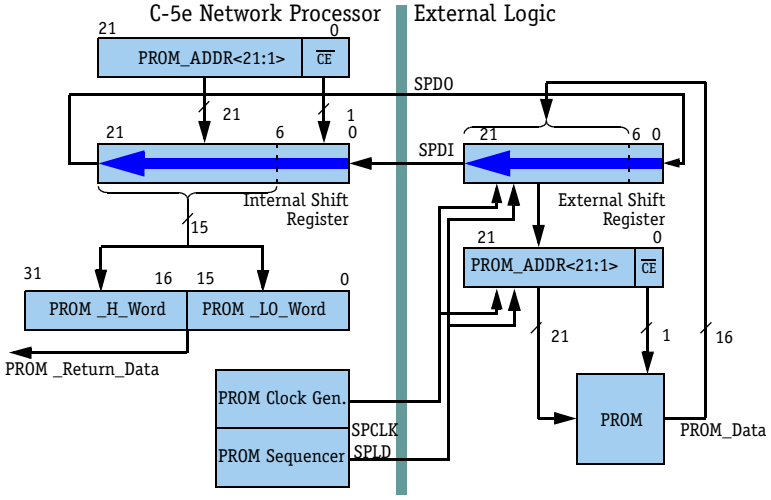
The PROM interface is a low speed I/O port that allows the C-5e NP to communicate through external logic to PROM. The PROM clock is $^1/_2$ to $^1/_{16}$ the core clock rate. The maximum PROM size is 4MBytes x 16, and configuration is required. The PROM signals are listed in Table 16.

Table 16 PROM Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
SPDO	AA1	1	LVTTL	O	Serial Data Out
SPDI	AA2	1	LVTTL	I_{PD}	Serial Data In
SPLD	AA3	1	LVTTL	O	When load is asserted on a positive clock edge, the external logic performs a parallel load. On each positive clock edge when load is de-asserted, the shift registers shift. When the PROM interface is idle: • if SPLD is asserted HI it indicates low speed serial protocol, • if asserted LOW it indicates MDIO serial protocol.
SPCK	AA4	1	LVTTL	O	Clock
TOTAL PINS		**4**			

Figure 5 shows the connections between the PROM Interface and external board logic. The application is required to provide an external shift register with parallel-in and parallel-out capabilities, and a parallel load register. Both devices should be positive-edge-triggered and perform a parallel load whenever SPLD is asserted. When SPLD is deasserted the shift register shifts.

Figure 5 PROM Interface Diagram



The PROM interface operates in the following manner (Note that two accesses are piplined together to execute one 32-bit fetch). The steps are shown in Figure 6.

1 The PROM_ADDR is loaded into the network processor internal shift register.

2 The PROM_ADDR is shifted into the external shift register for 22 SPCLK cycles.

3 SPLD is asserted for one SPCLK cycle, loading the PROM_ADDR into the external presentation register.

4 SPLD is deasserted for 22 SPCLK cycles. The PROM presents the first 16bit PROM_DATA. At the same time, the next PROM_ADDR is shifted into the external shift register.

5 SPLD is asserted for one SPCLK cycle, loading the PROM_ADDR into the external presentation register and the first PROM_DATA into the external shift register.

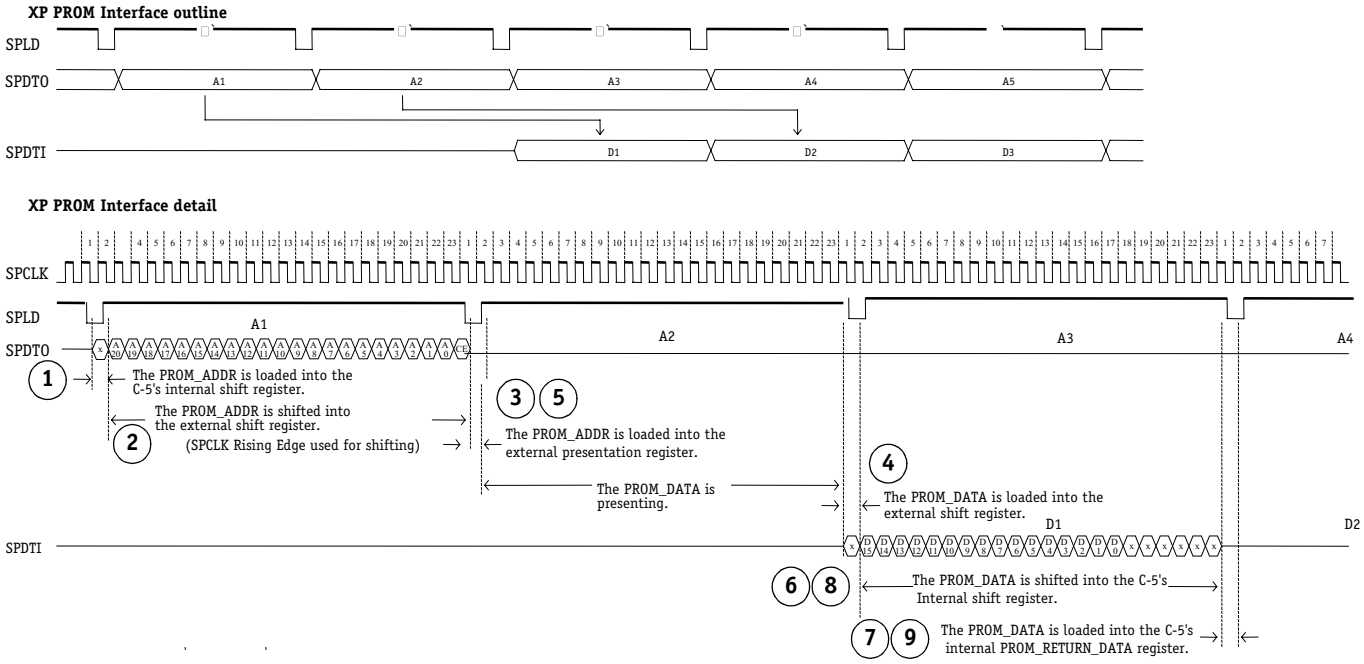
6 SPLD is deasserted for 22 SPCLK cycles, shifting the first PROM_DATA into the network processor internal shift register.

7 SPLD is asserted for one SPCLK cycle, loading the first PROM_DATA into the network processor PROM_RETURN_DATA register and the second PROM_DATA into the external shift register.

8 SPLD is deasserted for 22 SPCLK cycles, shifting the second PROM_DATA into the network processor internal shift register.

9 SPLD is asserted for one SPCLK cycle, loading the second PROM_DATA into the network processor PROM_RETURN_DATA register.

Figure 6 PROM Interface Timing Outline



General System Interface Signal

Table 17 provides the signal for the Executive Processor reset power status and I/O clock. The C-5e NP can be powered up with the XP either running or with the XP in reset mode similar to the CPs. When the XP remains in reset mode, an external host can be used to control the initialization of the C-5e NP.

Table 17 General System Interface Signal

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
XPUHOT	Y6	1	LVTTL	I_{PD}	Sample at Power On Reset determines if the XP RISC Core is held in reset. Low equals reset and High equals active. During normal operation, this is an external interrupt.
TOTAL PINS		**1**			

Fabric Processor Interface Signals

The FP has logical signal interfaces: a receive data interface and a transmit data interface, each with its own control, data, and clock signals. The interface has the following characteristic:

The interface clocks FRXCLK and FTXCLK can have a different frequency from the core C-5e NP clock frequency. The FP supports a fabric interface frequency from 10MHz to 125MHz.

FRXCLK and FTXCLK can be independent of each other; typically they have the same frequency, but are allowed to be skewed relative to each other.

Each data bus can be configured for widths of 8 (data bits 7:0 are used) , 16 (bits 15:0), or 32 (bits 31:0). In 8bit mode, data bits 31:8 are unused. In 16bit mode, data bits 31:16 are unused.

Table 18 Fabric Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
FIN0 - FIN31	AD13, AC13, AJ12, AH12, AG12, AF12, AE12, AD12, AC12, AJ11, AH11, AG11, AF11, AE11, AD11, AC11, AJ10, AH10, AG10, AF10, AE10, AD10, AC10, AJ9, AH9, AG9, AF9, AE9, AD9, AC9, AJ8, AH8	32	LVTTL	I_{PD}	Fabric Data Bus In
FOUT0 - FOUT31	AJ19, AH19, AG19, AJ18, AH18, AG18, AF18, AE18, AD18, AC18, AJ17, AH17, AG17, AF17, AE17, AD17, AC17, AJ16, AH16, AG16, AF16, AE16, AD16, AC16, AJ15, AH15, AF15, AE15, AD15, AC15, AJ14, AH14	32	LVTTL	O	Fabric Data Bus Out
FRXCLK	AG7	1	LVTTL	I_{PD}	Receive Clock
FTXCLK	AG13	1	LVTTL	I_{PD}	Transmit Clock
FRXCTL0 - FRXCTL6	AG8, AF8, AE8, AD8, AC8, AJ7, AH7	7	LVTTL	I_{PD}, O	Receive Control Signals
FTXCTL0 - FTXCTL6	AG14, AF14, AE14, AD14, AC14, AJ13, AH13	7	LVTTL	I_{PD}, O	Transmit Control Signals
TOTAL PINS		**80**			

The following tables list the Fabric Interface pin mappings:

- Utopia1, Utopia2, Utopia3 ATM Mode mappings are listed in Table 19
- Utopia1, Utopia2, Utopia3 PHY Mode mappings are listed in Table 20
- PRIZMA Mode mappings are listed in Table 21 (PRIZMA protocol is a subset of Utopia3 PHY)

- Power X(CSIX-L0) Mode mappings are listed in Table 22
- CSIX-L1 Mode mappings are listed in Table 23

Table 19 Utopia1*, 2*, 3 ATM Mode, C-5e Network Processor to Fabric Interface Pin Mapping

RECEIVE SIGNALS				TRANSMIT SIGNALS			
C-5E NETWORK PROCESSOR	I/O	UTOPIA	NOTE	C-5E NETWORK PROCESSOR	I/O	UTOPIA	NOTE
FRXCTL0	Output	RxEnb*	Pullup or No Connection	FTXCTL0	Output	TxEnb*	Pullup or No Connection
FRXCTL1	Input	RxClav		FTXCTL1	Input	TxClav	
FRXCTL2	Input	RxSOC		FTXCTL2	Output	TxSOC	
FRXCTL3	Input	n/a		FTXCTL3	Input	n/a	
FRXCTL4	Input	n/a		FTXCTL4	Input	n/a	
FRXCTL5	Input	n/a		FTXCTL5	Input	n/a	
FRXCTL6	Input	RxPrty		FTXCTL6	Output	TxPrty	

* Cell size must be 4Byte aligned. Both RxEnb and TxEnb are Active Low.

Table 20 Utopia1*, 2*, 3 PHY Mode, C-5e Network Processor to Fabric Interface Pin Mapping

RECEIVE SIGNALS				TRANSMIT SIGNALS			
C-5E NETWORK PROCESSOR	I/O	UTOPIA	NOTE	C-5E NETWORK PROCESSOR	I/O	UTOPIA	NOTE
FRXCTL0	Input	TxEnb*	Pullup	FTXCTL0	Input	RxEnb*	Pullup
FRXCTL1	Output	TxClav	No Connection	FTXCTL1	Output	RxClav	No Connection
FRXCTL2	Input	TxSOC		FTXCTL2	Output	RxSOC	
FRXCTL3	Input	n/a		FTXCTL3	Input	n/a	
FRXCTL4	Input	n/a		FTXCTL4	Input	n/a	
FRXCTL5	Input	n/a		FTXCTL5	Input	n/a	
FRXCTL6	Input	TxPrty		FTXCTL6	Output	RxPrty	

* Cell size must be 4Byte aligned. Both TxEnb and RxEnb are Active Low.

When configuring two C-5e network processors back-to-back using the Fabric Port, set up the transmit side of each C-5e network processor in Utopia ATM mode and the receive side of each C-5e network processor in Utopia PHY mode.

Table 21 PRIZMA Mode, C-5e Network Processor to Fabric Interface Pin Mapping

RECEIVE SIGNALS				TRANSMIT SIGNALS			
C-5E NETWORK PROCESSOR	I/O	UTOPIA	NOTE	C-5E NETWORK PROCESSOR	I/O	UTOPIA	NOTE
FRXCTL0	Input	TxEnb*	Not connected to fabric.	FTXCTL0	Input	RxEnb*	Not connected to fabric.
FRXCTL1	Output	TxClav	No connection	FTXCTL1	Output	RxClav	No Connection
FRXCTL2	Input	TxSOP		FTXCTL2	Output	RxSOP	
FRXCTL3	Input	n/a		FTXCTL3	Input	n/a	
FRXCTL4	Input	n/a		FTXCTL4	Input	n/a	
FRXCTL5	Input	n/a		FTXCTL5	Input	n/a	
FRXCTL6	Input	TxPrty	Optional	FTXCTL6	Output	RxPrty	Optional

* Both TxEnb and RxEnb are Active Low.

Table 22 Power X(CSIX-L0) Mode, C-5e Network Processor to Fabric Interface Pin Mapping

RECEIVE SIGNALS				TRANSMIT SIGNALS			
C-5E NETWORK PROCESSOR	I/O	POWER X	NOTE	C-5E NETWORK PROCESSOR	I/O	POWER X	NOTE
FRXCTL0	Input	RxCtrl[0]		FTXCTL0	Output	TxCtrl[0]	
FRXCTL1	Input	RxCtrl[1]		FTXCTL1	Output	TxCtrl[1]	
FRXCTL2	Input	RxCtrl[2]		FTXCTL2	Output	TxCtrl[2]	
FRXCTL3	Input	RxPrty[3]		FTXCTL3	Output	TxPrty[3]	
FRXCTL4	Input	RxPrty[2]		FTXCTL4	Output	TxPrty[2]	
FRXCTL5	Input	RxPrty[1]		FTXCTL5	Output	TxPrty[1]	
FRXCTL6	Input	RxPrty[0]		FTXCTL6	Output	TxPrty[0]	

For the CSIX-L1 Mode, VDDF= 2.5V.

Table 23 CSIX-L1 Mode, C-5e Network to Fabric Interface Pin Mapping

FPRX SIGNALS				FPTX SIGNALS			
C-5E NP	**I/O**	**CSIX-L1**	**NOTE**	**C-5E NP**	**I/O**	**CSIX-L1**	**NOTE**
FRxCTL0	Input	n/a		FTxCTL0	Input	n/a	
FRxCTL1	Input	n/a		FTxCTL1	Input	n/a	
FRxCTL2	Input	TxSOF		FTxCTL2	Output	RxSOF	
FRxCTL3	Input	n/a		FTxCTL3	Input	n/a	
FRxCTL4	Input	n/a		FTxCTL4	Input	n/a	
FRxCTL5	Input	n/a		FTxCTL5	Input	n/a	
FRxCTL6	Input	TxPrty		FTxCTL6	Output	RxPrty	

BMU SDRAM Interface Signals

The BMU and SDRAM interface signals are described in Table 24.

The BMU is designed to support SDRAM devices with 12 address lines. All 139 data lines and all 12 address lines must be connected to the SDRAM in order for the BMU to be able to read and write external SDRAM properly.

Table 24 BMU SDRAM Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
MD0 - MD129	U24, U23, T29, T28, T27, T26, T25, T24, T23, R29, R28, R27, R26, R25, R24, R23, P29, P28, P27, P26, P25, P24, P23, N29, N28, N27, N26, N25, N24, N23, M29, M28, M27, M26, M25, M24, M23, L29, L28, L27, L26, L25, L24, L23, K29, K28, K27, K26, K25, K24, K23, J29, J28, J27, J26, J25, J24, J23, H29, H28, H27, H26, H25, H24, H23, G29, G28, G27, G26, G25, G24, G23, F29, F28, F27, F26, F25, F24, F23, E29, E28, E27, E26, E24, E23, D29, D28, D27, D26, D25, D24, D23, C29, C28, C26, C25, C24, C23, B29, B28, B27, B26, B25, B24, B23, A29, A28, A27, A26, A25, A24, A23, G22, F22, E22, D22, C21, C22, B22, A22, G21, F21, E21, D21, B21, A21, G20, F20, E20, D20,	130	LVTTL	I_{PD}/O	Data Lines In
MDECC0 - MDECC8	A19, B19, C19, D19, E19, F19, G19, A20, B20	9	LVTTL	I_{PD}/O	Stored as data, ECC bits
MA0 - MA11	A15, A16, B16, C16, D16, E16, F16, G16, A17, B17, C17, D17	12	LVTTL	O_{PD}	Address Outputs: A0-A11 are sampled during the ACTIVE command and READ/WRITE to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a LOAD MODE REGISTER command
MBA0 - MBA1	F17, E17	2	LVTTL	O_{PD}	Bank Address Outputs: BA0 and BA1 define which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
MCASX	E18	1	LVTTL	O_{PD}	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. *NOTE: MCSX is considered part of the command code.*

Table 24 BMU SDRAM Interface Signals (continued)

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
MRASX	D18	1	LVTTL	O_{PD}	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. MCSX is considered part of the command code.
MWEX	C18	1	LVTTL	O_{PD}	Command Outputs: MRASX, MCASX, MWEX and MCSX define the command being entered. MCSX is considered part of the command code.
MCSX	B18	1	LVTTL	O_{PD}	Chip Select: MCSX enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when MCSX is registered HIGH. MCSX provides the external bank selection on systems with multiple banks. MCSX is considered part of the command code.
MDQM MDQML	A18 G17	1 1	LVTTL LVTTL	O_{PD} O_{PD}	Input/Output Mask: MDQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when MDQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a high Z state (two-clock latency) when MDQM is sampled HIGH during the READ cycle. *NOTE: MDQML is an identical copy of MDQM used to drive the loading on SDRAM configurations with 2 DQM pins.*
MDCLK	C20	1	LVTTL	I_{PD}	Clock: MDCLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of the MDCLK. MDCLK also increments the internal burst counter and controls the output registers.
TOTAL PINS		**160**			

TLU SRAM Interface Signals

The TLU SRAM interface supports up to 128MBytes of SRAM at frequencies to 133MHz using LVTTL signaling levels (in single bank-mode only) and SRAM technologies up to 64Mbits. The TLU SRAM interface signals are described in Table 25.

Table 25 TLU SRAM Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
TD0 - TD63	F1, F2, F3, F4, F5, F6, F7, G1, G2, G3, G4, G5, G6, G7, H1, H2, H3, H4, H5, H6, H7, J1, J2, J3, J4, J5, J6, J7, K1, K2, K3, K4, K5, K6, K7, L1, L2, L3, L4, L5, L6, M1, M2, M3, M4, M5, M6, M7, N1, N2, N3, N4, N5, N6, N7, P1, P2, P3, P4, P5, P6, R1, R2, R3	64	LVTTL	I_{PD}/O	TLU Memory Data
TA0 - TA21	U1, U2, U3, U4, V1, V2, V3, V4, V5, V6, V7, W1, W2, W3, W4, W5, W6, Y1, Y2, Y3, Y4, Y5	22	LVTTL	O_{PD}	TLU Memory Address
TPAR0 - TPAR3	R4, R5, R6, P7	4	LVTTL	I_{PD}/O	Word Data Parity (i.e. TPAR0 across TD15:0)
TCE0X - TCE3X	U5, U6, U7, T7	4	LVTTL	O_{PD}	TLU Memory Chip Enable
TWE0X - TWE3X	T2, T3, T4, T5	4	LVTTL	O_{PD}	TLU Memory Write Enable
TCLKI	T1	1	LVTTL	I_{PD}	TLU Clock Input
TOTAL PINS		**99**			

QMU SRAM (Internal Mode) Interface Signals

The QMU signals are described in Table 26.

Table 26 QMU SRAM (Internal Mode) Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
QA0 - QA16	E9, D9, C9, B9, A9, G10, F10, E10, D10, C10, B10, A10, F11, E11, D11, C11, B11	17	LVTTL	O	Address [16:0]
QD0 - QD31	E1, D1, C1, B1, E2, D2, C2, B2, A2, E3, D3, B3, A3, E4, D4, C4, B4, A4, D5, C5, B5, A5, E6, D6, C6, B6, A6, E7, D7, C7, B7, A7	32	LVTTL	I_{PD}/O	Data
QDQPAR	G11	1	LVTTL	I_{PD}	nc
QARDY	G9	1	LVTTL	I_{PD}	nc
QNQRDY	F9	1	LVTTL	nc	nc
QWEX	G8	1	LVTTL	O	Write Enable
QBCLKO	F8	1	LVTTL	O	nc
QBCLKI	E8	1	LVTTL	I_{PD}	nc
QACLKO	D8	1	LVTTL	O	nc
QACLKI	C8	1	LVTTL	I_{PD}	Input Clock
QDPL	B8	1	LVTTL	I_{PD}/O	Data Parity Low
QDPH	A8	1	LVTTL	I_{PD}/O	Data Parity High
TOTAL PINS		**59**			

QMU to Q-5 (External Mode) Interface Signals

The QMU to Q-5 signals are described in Table 27.

Table 27 QMU to Q-5 (External Mode) Interface Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
QA0 - QA15	E9, D9, C9, B9, A9, G10, F10, E10, D10, C10, B10, A10, F11, E11, D11, C11	16	LVTTL	I_{PD}	Enqueue Data [8:23]
QA16	B11	1	LVTTL	I_{PD}	Enqueue Parity
QD0 - QD23	E1, D1, C1, B1, E2, D2, C2, B2, A2, E3, D3, B3, A3, E4, D4, C4, B4, A4, D5, C5, B5, A5, E6, D6	24	LVTTL	I_{PD}	Dequeue Data [0:23]
QD24 - QD31	C6, B6, A6, E7, D7, C7, B7, A7	8	LVTTL	I_{PD}	Enqueue Data [0:7]
QDQPAR	G11	1	LVTTL	I_{PD}	Dequeue Parity
QARDY	G9	1	LVTTL	I_{PD}	Dequeue Ready
QNQRDY	F9	1	LVTTL	I_{PD}	Enqueue Ready
QWEX	G8	1	LVTTL	I_{PD}	Dequeue Ready
QBCLKO	F8	1	LVTTL	O	Output ClockB
QBCLKI	E8	1	LVTTL	I_{PD}	Input ClockB
QACLKO	D8	1	LVTTL	O	Output ClockA
QACLKI	C8	1	LVTTL	I_{PD}	Input ClockA
QDPL	B8	1	LVTTL	I_{PD}	Dequeue Ack [0]
QDPH	A8	1	LVTTL	I_{PD}	Dequeue Ack [1]
TOTAL PINS		**59**			

Power Supply Signals Power supply, and ground signals are described in Table 28.

Table 28 Power Supply Signals

SIGNAL NAME	PIN #	TOTAL	TYPE	SIGNAL DESCRIPTION
VDD	H12, J13, J17, J19, K10, K12, K14, K16, K18, K20, L9, L11, L13, L15, L17, L19, L21, M10, M12, M14, M16, M18, M20, N9, N11, N13, N15, N17, N19, N21, P10, P12, P14, P16, P18, P20, R11, R13, R15, R17, R19, T10, T12, T14, T16, T18, T20, U9, U11, U13, U15, U17, U19, U21, V10, V12, V14, V16, V18, V20, W9, W11, W13, W15, W17, W19, Y10, Y12, Y14, Y16, Y18, Y20, AA11, AA13, AA15, AA17, AA19	77	P	Core Supply Voltage (1.2V Input)
VDD33	E25, H14, H16, H18, H20, H22, J15, J21, K22, M22, P22, R21, T22, V22, W21, Y22, AA9, AA21, AB8, AB10, AB18, AB20, AB22, AE5, AE25	25	P	I/O Supply Voltage (3.3V Input)
GND	C3, C15, C27, H9, H11, H13, H15, H17, H19, H21, J8, J10, J12, J14, J16, J18, J20, J22, K9, K11, K13, K15, K17, K19, K21, L8, L10, L12, L14, L16, L18, L20, L22, M9, M11, M13, M15, M17, M19, M21, N8, N10, N12, N14, N16, N18, N20, N22, P9, P11, P13, P15, P17, P19, P21, R8, R10, R12, R14, R16, R18, R20, R22, T9, T11, T13, T15, T17, T19, T21, U8, U10, U12, U14, U16, U18, U20, U22, V9, V11, V13, V15, V17, V19, V21, W8, W10, W12, W14, W16, W18, W20, W22, Y9, Y11, Y13, Y15, Y17, Y19, Y21, AA8, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AG3, AG27	117	P	Ground
VDDF	AB12, AB14, AB16, AG15	4	P	Fabric I/O supply (3.3 or 2.5V)
VDDT	E5, H8, H10, J9, J11, K8, L7, M8, P8, R7, R9, T8, V8, W7, Y8	15	P	TLU and QMU I/O supply (3.3V)
TOTAL PINS		**238**		

Test Signals

Test signals are described in Table 29.

Table 29 Miscellaneous Test Signals For JTAG, Scan, and Internal Test Routines

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
JTCK	D13	1	LVTTL	I_{PD}	Test Clock
JTMS	B13	1	LVTTL	I_{PD}	Test Mode Select. High selects modes as defined in the IEEE 1149.1 JTAG specification.
JTRSTX†	A13	1	LVTTL	I_{PD}	Test Reset (low active)
JTDI†	C13	1	LVTTL	I_{PD}	Test Data In
JTDO	B12	1	LVTTL	O	Test Data Out
JHIGHZ	C12	1	LVTTL	I_{PD}	Turns off all output drivers when High
JCLKBYP	D12	1	LVTTL	I_{PD}	1X or 2X Clock Mode Select. Low selects 1X, High selects 2X.
JSE	E15	1	LVTTL	I_{PD}	Scan Enable. High enables scan test.
JS00-JS05	D15, B15, D14, C14, B14, A14	6	LVTTL	O	Scan Out Pins
TOTAL PINS		**14**			

During JTAG, SCLK and SCLKX must remain as differential inputs.

No Connection Pins

No connection pins are listed in Table 30.

Table 30 No Connection Pins

SIGNAL NAME	PIN #	TOTAL	TYPE	I/O	SIGNAL DESCRIPTION
NC0 - NC9	AF13, AE13, T6, A11, A12, F18, G18, Y7, AF7, AE7	10	nc	I_{PD}/O	Reserved for future functionality
TOTAL PINS		**10**			

Signals Grouped by Pin Number

The C-5e NP signals are listed by pin number in Table 31.

Table 31 Signals Listed by Pin Number

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
A 1-29							
A1	Not present	A9	QA4	A17	MA8	A25	MD109
A2	QD8	A10	QA11	A18	MDQM	A26	MD108
A3	QD12	A11	NC3	A19	MDECC0	A27	MD107
A4	QD17	A12	NC4	A20	MDECC7	A28	MD106
A5	QD21	A13	JTRSTX	A21	MD125	A29	MD105
A6	QD26	A14	JS05	A22	MD118		
A7	QD31	A15	MA0	A23	MD111		
A8	QDPH	A16	MA1	A24	MD110		
B 1-29							
B1	QD3	B9	QA3	B17	MA9	B25	MD102
B2	QD7	B10	QA10	B18	MCSX	B26	MD101
B3	QD11	B11	QA16	B19	MDECC1	B27	MD100
B4	QD16	B12	JTDO	B20	MDECC8	B28	MD99
B5	QD20	B13	JTMS	B21	MD124	B29	MD98
B6	QD25	B14	JS04	B22	MD117		
B7	QD30	B15	JS01	B23	MD104		
B8	QDPL	B16	MA2	B24	MD103		
C 1-29							
C1	QD2	C9	QA2	C17	MA10	C25	MD95
C2	QD6	C10	QA9	C18	MWEX	C26	MD94
C3	GND	C11	QA15	C19	MDECC2	C27	GND
C4	QD15	C12	JHIGHZ	C20	MDCLK	C28	MD93
C5	QD19	C13	JTDI	C21	MD123	C29	MD92
C6	QD24	C14	JS03	C22	MD116		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
C7	QD27	C15	GND	C23	MD97		
C8	QACLKI	C16	MA3	C24	MD96		
D 1-29							
D1	QD1	D9	QA1	D17	MA11	D25	MD89
D2	QD5	D10	QA8	D18	MRASX	D26	MD88
D3	QD10	D11	QA14	D19	MDECC3	D27	MD87
D4	QD14	D12	JCLKBYP	D20	MD129	D28	MD86
D5	QD18	D13	JTCK	D21	MD122	D29	MD85
D6	QD23	D14	JS02	D22	MD115		
D7	QD28	D15	JS00	D23	MD91		
D8	QACLKO	D16	MA4	D24	MD90		
E 1-29							
E1	QD0	E9	QA0	E17	MBA1	E25	VDD33
E2	QD4	E10	QA7	E18	MCASX	E26	MD82
E3	QD9	E11	QA13	E19	MDECC4	E27	MD81
E4	QD13	E12	CCLK7	E20	MD128	E28	MD80
E5	VDDT	E13	CCLK5	E21	MD121	E29	MD79
E6	QD22	E14	CCLK2	E22	MD114		
E7	QD27	E15	JSE	E23	MD84		
E8	QBCLKI	E16	MA5	E24	MD83		
F 1-29							
F1	TD0	F9	QNQRDY	F17	MBA0	F25	MD76
F2	TD1	F10	QA6	F18	NC5	F26	MD75
F3	TD2	F11	QA12	F19	MDECC5	F27	MD74
F4	TD3	F12	CCLK6	F20	MD127	F28	MD73
F5	TD4	F13	CCLK4	F21	MD120	F29	MD72
F6	TD5	F14	CCLK1	F22	MD113		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
F7	TD6	F15	SCLKX	F23	MD78		
F8	QBCLKO	F16	MA6	F24	MD77		
G 1-29							
G1	TD7	G9	QARDY	G17	MDQML	G25	MD69
G2	TD8	G10	QA5	G18	NC6	G26	MD68
G3	TD9	G11	QDQPAR	G19	MDECC6	G27	MD67
G4	TD10	G12	CPREF	G20	MD126	G28	MD66
G5	TD11	G13	CCLK3	G21	MD119	G29	MD65
G6	TD12	G14	CCLK0	G22	MD112		
G7	TD13	G15	SCLK	G23	MD71		
G8	QWEX	G16	MA7	G24	MD70		
H 1-29							
H1	TD14	H9	GND	H17	GND	H25	MD62
H2	TD15	H10	VDDT	H18	VDD33	H26	MD61
H3	TD16	H11	GND	H19	GND	H27	MD60
H4	TD17	H12	VDD	H20	VDD33	H28	MD59
H5	TD18	H13	GND	H21	GND	H29	MD58
H6	TD19	H14	VDD33	H22	VDD33		
H7	TD20	H15	GND	H23	MD64		
H8	VDDT	H16	VDD33	H24	MD63		
J 1-29							
J1	TD21	J9	VDDT	J17	VDD	J25	MD55
J2	TD22	J10	GND	J18	GND	J26	MD54
J3	TD23	J11	VDDT	J19	VDD	J27	MD53
J4	TD24	J12	GND	J20	GND	J28	MD52
J5	TD25	J13	VDD	J21	VDD33	J29	MD51
J6	TD26	J14	GND	J22	GND		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
J7	TD27	J15	VDD33	J23	MD57		
J8	GND	J16	GND	J24	MD56		
K 1-29							
K1	TD28	K9	GND	K17	GND	K25	MD48
K2	TD29	K10	VDD	K18	VDD	K26	MD47
K3	TD30	K11	GND	K19	GND	K27	MD46
K4	TD31	K12	VDD	K20	VDD	K28	MD45
K5	TD32	K13	GND	K21	GND	K29	MD44
K6	TD33	K14	VDD	K22	VDD33		
K7	TD34	K15	GND	K23	MD50		
K8	VDDT	K16	VDD	K24	MD49		
L 1-29							
L1	TD35	L9	VDD	L17	VDD	L25	MD41
L2	TD36	L10	GND	L18	GND	L26	MD40
L3	TD37	L11	VDD	L19	VDD	L27	MD39
L4	TD38	L12	GND	L20	GND	L28	MD38
L5	TD39	L13	VDD	L21	VDD	L29	MD37
L6	TD40	L14	GND	L22	GND		
L7	VDDT	L15	VDD	L23	MD43		
L8	GND	L16	GND	L24	MD42		
M 1-29							
M1	TD41	M9	GND	M17	GND	M25	MD34
M2	TD42	M10	VDD	M18	VDD	M26	MD33
M3	TD43	M11	GND	M19	GND	M27	MD32
M4	TD44	M12	VDD	M20	VDD	M28	MD31
M5	TD45	M13	GND	M21	GND	M29	MD30
M6	TD46	M14	VDD	M22	VDD33		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
M7	TD47	M15	GND	M23	MD36		
M8	VDDT	M16	VDD	M24	MD35		
N 1-29							
N1	TD48	N9	VDD	N17	VDD	N25	MD27
N2	TD49	N10	GND	N18	GND	N26	MD26
N3	TD50	N11	VDD	N19	VDD	N27	MD25
N4	TD51	N12	GND	N20	GND	N28	MD24
N5	TD52	N13	VDD	N21	VDD	N29	MD23
N6	TD53	N14	GND	N22	GND		
N7	TD54	N15	VDD	N23	MD29		
N8	GND	N16	GND	N24	MD28		
P 1-29							
P1	TD55	P9	GND	P17	GND	P25	MD20
P2	TD56	P10	VDD	P18	VDD	P26	MD19
P3	TD57	P11	GND	P19	GND	P27	MD18
P4	TD58	P12	VDD	P20	VDD	P28	MD17
P5	TD59	P13	GND	P21	GND	P29	MD16
P6	TD60	P14	VDD	P22	VDD33		
P7	TPAR3	P15	GND	P23	MD22		
P8	VDDT	P16	VDD	P24	MD21		
R 1-29							
R1	TD61	R9	VDDT	R17	VDD	R25	MD13
R2	TD62	R10	GND	R18	GND	R26	MD12
R3	TD63	R11	VDD	R19	VDD	R27	MD11
R4	TPAR0	R12	GND	R20	GND	R28	MD10
R5	TPAR1	R13	VDD	R21	VDD33	R29	MD9
R6	TPAR2	R14	GND	R22	GND		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
R7	VDDT	R15	VDD	R23	MD15		
R8	GND	R16	GND	R24	MD14		
T 1-29							
T1	TCLKI	T9	GND	T17	GND	T25	MD6
T2	TWE0X	T10	VDD	T18	VDD	T26	MD5
T3	TWE1X	T11	GND	T19	GND	T27	MD4
T4	TWE2X	T12	VDD	T20	VDD	T28	MD3
T5	TWE3X	T13	GND	T21	GND	T29	MD2
T6	NC2	T14	VDD	T22	VDD33		
T7	TCE3X	T15	GND	T23	MD8		
T8	VDDT	T16	VDD	T24	MD7		
U 1-29							
U1	TA0	U9	VDD	U17	VDD	U25	CPE_4
U2	TA1	U10	GND	U18	GND	U26	CPF_2
U3	TA2	U11	VDD	U19	VDD	U27	CPE_2
U4	TA3	U12	GND	U20	GND	U28	CPF_1
U5	TCE0X	U13	VDD	U21	VDD	U29	CPF_0
U6	TCE1X	U14	GND	U22	GND		
U7	TCE2X	U15	VDD	U23	MD1		
U8	GND	U16	GND	U24	MD0		
V 1-29							
V1	TA4	V9	GND	V17	GND	V25	CPD_4
V2	TA5	V10	VDD	V18	VDD	V26	CPE_3
V3	TA6	V11	GND	V19	GND	V27	CPD_2
V4	TA7	V12	VDD	V20	VDD	V28	CPE_1
V5	TA8	V13	GND	V21	GND	V29	CPE_0
V6	TA9	V14	VDD	V22	VDD33		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
V7	TA10	V15	GND	V23	CPE_6		
V8	VDDT	V16	VDD	V24	CPE_5		
W 1-29							
W1	TA11	W9	VDD	W17	VDD	W25	CPC_4
W2	TA12	W10	GND	W18	GND	W26	CPD_3
W3	TA13	W11	VDD	W19	VDD	W27	CPC_2
W4	TA14	W12	GND	W20	GND	W28	CPD_1
W5	TA15	W13	VDD	W21	VDD33	W29	CPD_0
W6	TA16	W14	GND	W22	GND		
W7	VDDT	W15	VDD	W23	CPD_6		
W8	GND	W16	GND	W24	CPD_5		
Y 1-29							
Y1	TA17	Y9	GND	Y17	GND	Y25	CPB_4
Y2	TA18	Y10	VDD	Y18	VDD	Y26	CPC_3
Y3	TA19	Y11	GND	Y19	GND	Y27	CPB_2
Y4	TA20	Y12	VDD	Y20	VDD	Y28	CPC_1
Y5	TA21	Y13	GND	Y21	GND	Y29	CPC_0
Y6	XPUHOT	Y14	VDD	Y22	VDD33		
Y7	NC7	Y15	GND	Y23	CPC_6		
Y8	VDDT	Y16	VDD	Y24	CPC_5		
AA 1-29							
AA1	SPDO	AA9	VDD33	AA17	VDD	AA25	CPA_4
AA2	SPDI	AA10	GND	AA18	GND	AA26	CPB_3
AA3	SPLD	AA11	VDD	AA19	VDD	AA27	CPA_2
AA4	SPCK	AA12	GND	AA20	GND	AA28	CPB_1
AA5	SICL	AA13	VDD	AA21	VDD33	AA29	CPB_0
AA6	SIDA	AA14	GND	AA22	GND		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
AA7	PFRAMEX	AA15	VDD	AA23	CPB_6		
AA8	GND	AA16	GND	AA24	CPB_5		
AB 1-29							
AB1	PCLK	AB9	GND	AB17	GND	AB25	CP4_6
AB2	PRSTX	AB10	VDD33	AB18	VDD33	AB26	CPA_3
AB3	PREQX	AB11	GND	AB19	GND	AB27	CP2_6
AB4	PGNTX	AB12	VDDF	AB20	VDD33	AB28	CPA_1
AB5	PIDSEL	AB13	GND	AB21	GND	AB29	CPA_0
AB6	PINTA	AB14	VDDF	AB22	VDD33		
AB7	PCBEX0	AB15	GND	AB23	CPA_6		
AB8	VDD33	AB16	VDDF	AB24	CPA_5		
AC 1-29							
AC1	PSERRX	AC9	FIN29	AC17	FOUT16	AC25	CP4_5
AC2	PPERRX	AC10	FIN22	AC18	FOUT9	AC26	CP3_6
AC3	PDEVSELX	AC11	FIN15	AC19	CPF_6	AC27	CP2_5
AC4	PSTOPX	AC12	FIN8	AC20	CP9_6	AC28	CP1_6
AC5	PIRDYX	AC13	FIN1	AC21	CP8_6	AC29	CP0_6
AC6	PTRDYX	AC14	FTXCTL4	AC22	CP7_6		
AC7	PCBEX1	AC15	FOUT29	AC23	CP6_6		
AC8	FRXCTL4	AC16	FOUT23	AC24	CP5_6		
AD 1-29							
AD1	PAD31	AD9	FIN28	AD17	FOUT15	AD25	CP4_4
AD2	PAD30	AD10	FIN21	AD18	FOUT8	AD26	CP3_5
AD3	PAD29	AD11	FIN14	AD19	CPF_5	AD27	CP2_4
AD4	PAD28	AD12	FIN7	AD20	CP9_5	AD28	CP1_5
AD5	PPAR	AD13	FIN0	AD21	CP8_5	AD29	CP0_5
AD6	PCBEX3	AD14	FTXCTL3	AD22	CP7_5		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
AD7	PCBEX2	AD15	FOUT28	AD23	CP6_5		
AD8	FRXCTL3	AD16	FOUT22	AD24	CP5_5		
AE 1-29							
AE1	PAD27	AE9	FIN27	AE17	FOUT14	AE25	VDD33
AE2	PAD26	AE10	FIN20	AE18	FOUT7	AE26	CP3_4
AE3	PAD25	AE11	FIN13	AE19	CPF_4	AE27	CP2_3
AE4	PAD24	AE12	FIN6	AE20	CP9_4	AE28	CP1_4
AE5	VDD33	AE13	NC1	AE21	CP8_4	AE29	CP0_4
AE6	PAD23	AE14	FTXCTL2	AE22	CP7_4		
AE7	NC9	AE15	FOUT27	AE23	CP6_4		
AE8	FRXCTL2	AE16	FOUT21	AE24	CP5_4		
AF 1-29							
AF1	PAD22	AF9	FIN26	AF17	FOUT13	AF25	CP4_3
AF2	PAD21	AF10	FIN19	AF18	FOUT6	AF26	CP3_3
AF3	PAD20	AF11	FIN12	AF19	CPF_3	AF27	CP2_2
AF4	PAD19	AF12	FIN5	AF20	CP9_3	AF28	CP1_3
AF5	PAD18	AF13	NC0	AF21	CP8_3	AF29	CP0_3
AF6	PAD17	AF14	FTXCTL1	AF22	CP7_3		
AF7	NC8	AF15	FOUT26	AF23	CP6_3		
AF8	FRXCTL1	AF16	FOUT20	AF24	CP5_3		
AG 1-29							
AG1	PAD16	AG9	FIN25	AG17	FOUT12	AG25	CP4_2
AG2	PAD15	AG10	FIN18	AG18	FOUT5	AG26	CP3_2
AG3	GND	AG11	FIN11	AG19	FOUT2	AG27	GND
AG4	PAD14	AG12	FIN4	AG20	CP9_2	AG28	CP1_2
AG5	PAD13	AG13	FTXCLK	AG21	CP8_2	AG29	CP0_2
AG6	PAD12	AG14	FTXCTL0	AG22	CP7_2		
AG7	FRXCLK	AG15	VDDF	AG23	CP6_2		

Table 31 Signals Listed by Pin Number (continued)

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
AG8	FRXCTL0	AG16	FOUT19	AG24	CP5_2		
AH 1-29							
AH1	PAD11	AH9	FIN24	AH17	FOUT11	AH25	CP4_1
AH2	PAD10	AH10	FIN17	AH18	FOUT4	AH26	CP3_1
AH3	PAD9	AH11	FIN10	AH19	FOUT1	AH27	CP2_1
AH4	PAD8	AH12	FIN3	AH20	CP9_1	AH28	CP1_1
AH5	PAD7	AH13	FTXCTL6	AH21	CP8_1	AH29	CP0_1
AH6	PAD6	AH14	FOUT31	AH22	CP7_1		
AH7	FRXCTL6	AH15	FOUT25	AH23	CP6_1		
AH8	FIN31	AH16	FOUT18	AH24	CP5_1		
AJ 1-29							
AJ1	PAD5	AJ9	FIN23	AJ17	FOUT10	AJ25	CP4_0
AJ2	PAD4	AJ10	FIN16	AJ18	FOUT3	AJ26	CP3_0
AJ3	PAD3	AJ11	FIN9	AJ19	FOUT0	AJ27	CP2_0
AJ4	PAD2	AJ12	FIN2	AJ20	CP9_0	AJ28	CP1_0
AJ5	PAD1	AJ13	FTXCTL5	AJ21	CP8_0	AJ29	CP0_0
AJ6	PAD0	AJ14	FOUT30	AJ22	CP7_0		
AJ7	FRXCTL5	AJ15	FOUT24	AJ23	CP6_0		
AJ8	FIN30	AJ16	FOUT17	AJ24	CP5_0		

JTAG Support

The C-5e NP contains JTAG test logic compliant with the IEEE 1149.1 specification. All required public instructions are implemented, as well as some optional instructions. This section contains information regarding the pinout, instructions, identification codes, and boundary scan cell types.

Pinout

The C-5e NP uses the standard JTAG pins including the optional test reset pin. Table 29 describes the pins and their functions. These ports do not have internal pullups as required by the 1149.1 specification.

JTAG Data Registers

The C-5e NP contains the standard internal registers as specified in IEEE 1149.1. These registers are described in Table 32.

Table 32 JTAG Internal Register Descriptions

REGISTER NAME	REGISTER LENGTH	DESCRIPTION
Bypass	1	Standard JTAG bypass register
Boundary	1549	Boundary Scan Register
Device Identification	32	Standard JTAG IDCODE Register

Boundary Scan Cell Types

The C-5e NP boundary scan register contains only two cell types. All input cells are *observe only* cells of type BC_4. All enable and output cells are standard cells of type BC_1. In IEEE 1149.1-1990 specification, the BC_4 cell is shown in Figure 7 and the BC_1 cell is shown in Figure 8.

Figure 7 Observe-Only Cell

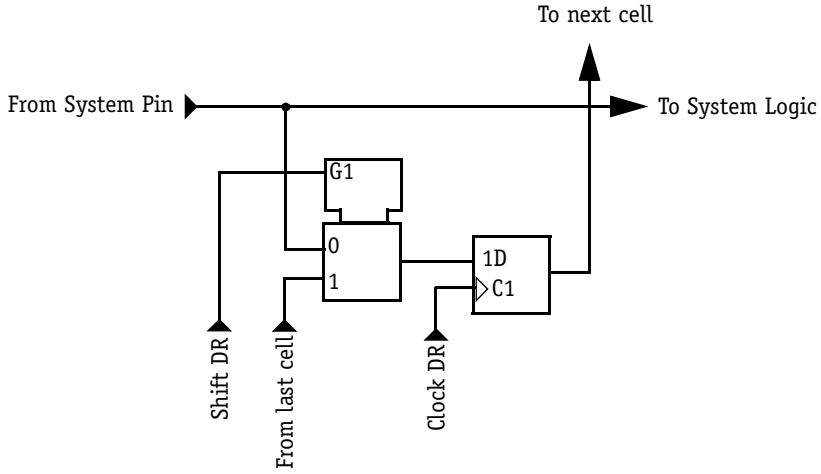
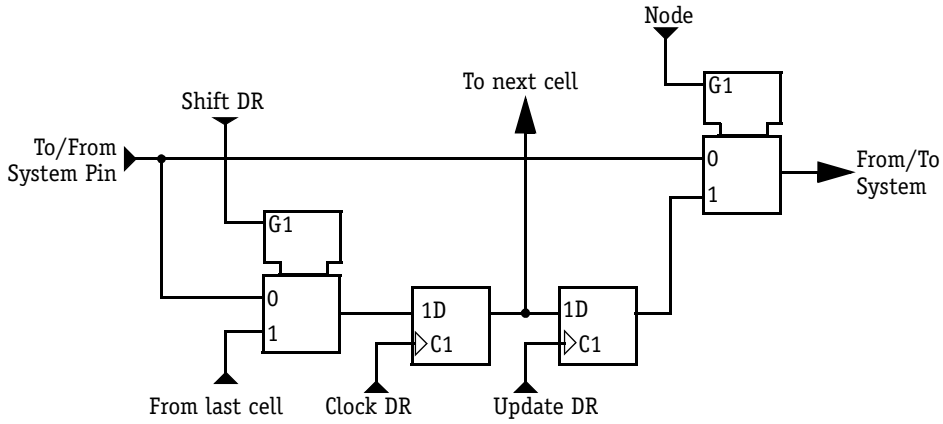


Figure 8 Cell Design That Can Be Used for Both Input and Output Pins



IDcode Register

The C-5e NP implements a standard 32bit JTAG identification register. Table 33 lists the value of the code for full identification and its subcomponents.

Table 33 JTAG Identification Code and Its Subcomponents

FIELD NAME	WIDTH	BIT POSITIONS	BINARY VALUE
Version	4	31-28	0000
Part Number	16	27-12	0000_0000_0010_0001
Manufacturer Identity	11	11-1	001_1001_0110
LSB	1	0	1

The concatenated 32bit value is hexidecimal 0002132d.

JTAG Instruction Register

The C-5e NP contains a 4bit instruction register. Table 34 lists the instructions that are supported.

Table 34 Instruction Register Instructions

INSTRUCTION MNEMONIC	SELECTED REGISTER	INSTRUCTION OPCODE
Extest	Boundary Scan	0000
Idcode	Identification Register	0001
Sample/Preload	Boundary Scan	0010
Highz	Bypass Register	0011
Clamp	Bypass Register	0100
Bypass	Bypass Register	0101
Reserved*	Bypass Register	0110
Reserved*	Bypass Register	0111
Bypass	Bypass Register	1000
Bypass	Bypass Register	1001
Bypass	Bypass Register	1010
Bypass	Bypass Register	1011
Bypass	Bypass Register	1100
Bypass	Bypass Register	1101

Table 34 Instruction Register Instructions (continued)

INSTRUCTION MNEMONIC	SELECTED REGISTER	INSTRUCTION OPCODE
Bypass	Bypass Register	1110
Bypass	Bypass Register	1111

* There are two reserved instructions intended for Motorola Corporation's internal use. These should not be programmed by users.

Boundary Scan Description Language

In order to simplify board test, Motorola Corporation has provided a boundary scan description language (BSDL) file (c5e.bsdl) in the Motorola web site that describes the complete set of instructions, boundary scan order, and identification code value in an industry standard format.

http://www.motorola.com/networkprocessors

Chapter 3

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 35 lists the absolute maximum ratings for the C-5e network processor. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" (Table 36) is possible.

Exposure to conditions beyond Table 35 can:

- Reduce device reliability
- Result in premature device failure, even with no immediate sign of failure

Prolonged exposure to conditions at or near the absolute maximum ratings could also result in reduced useful life and reliability of the C-5e NP.

Table 35 C-5e Network Processor Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
V_{DD33} Supply Voltage (3.3V input)*	-0.5	+5	V
V_{DD} Supply Voltage (1.2V input)*	-0.5	+2.2	V
Voltage on any pin	-0.5	V_{DD33} + 0.5	V
Static Discharge Voltage	2000/500		V
Storage Temperature	-40	+125	°C
Absolute Maximum Junction Temperature	-40	+125	°C
Body Temperature (soldering 10 seconds)			°C
Lead Temperature (soldering 10 seconds)			°C

* Voltages are relative to Ground

Recommended Operating Conditions

The recommended operating conditions describe an environment the C-5e NP network processor is expected to encounter during normal operation. Table 36 delineates the recommended operating parameters for the C-5e NP.

Table 36 C-5e Network Processor Recommended Operating Conditions

PARAMETER	MIN	MAX	UNIT
V_{DD33} Supply Voltage	3.135	3.465	V
V_{DD} Supply Voltage	1.14	1.26	V
I_{DD33} - V_{DD33} Supply Current		1.3	A
I_{DD} - V_{DD} Supply Current		8.5	A
T_j Junction Temperature	-40	125	°C

DC Characteristics

The DC electrical characteristics define the input operating conditions for proper operation and the output responses to applied DC signals and switch characteristics over specified voltage and temperature ranges. The DC electrical characteristics are specified within the *recommended operating conditions* including operating temperature and power supply range as stated in this data sheet. Table 37 outlines the C-5e NP DC characteristics.

Table 37 C-5e Network Processor DC Characteristics

PARAMETER*	MIN	MAX	UNIT	NOTES
LVTTL Input High Voltage	2.0	V_{DD33}+.3	V	
LVTTL Input Low Voltage	-0.3	0.8	V	
LVTTL Output High Voltage	2.4		V	@I_{OH} = -2mA
LVTTL Output Low Voltage		0.4	V	@I_{OL} = +2mA
LVTTL Input Current	-100	+100	µA	V_{IN} = 0V or V_{DD33}
LVPECL Input High Voltage	V_{DD33} -1.165	V_{DD33}+.3V	V	
LVPECL Input Low Voltage	-0.3	V_{DD33} -1.475	V	
LVPECL Output High Voltage	V_{DD33} -1.025	V_{DD33} -0.60	V	Load = 50ohm to V_{DD33} - 2V
LVPECL Output Low Voltage	V_{DD33} -2.20	V_{DD33} -1.620	V	Load = 50ohm to V_{DD33} - 2V
LVPECL Input Current	-100	+100	µA	
CPREF	V_{DD33} -1.38	V_{DD33} -1.26	V	Single-ended LVPECL reference

* All voltages are relative to Ground unless otherwise indicated.

Each control input pin has a capacitance associated with it. The capacitance at the control input is due to the package and the input circuitry connected to the pin. Capacitance is based on these conditions: T_A = 25°C; V_{DD33} = 3.3V; f = 1MHz. Table 38 provides capacitance data.

Table 38 C-5e Network Processor Capacitance Data

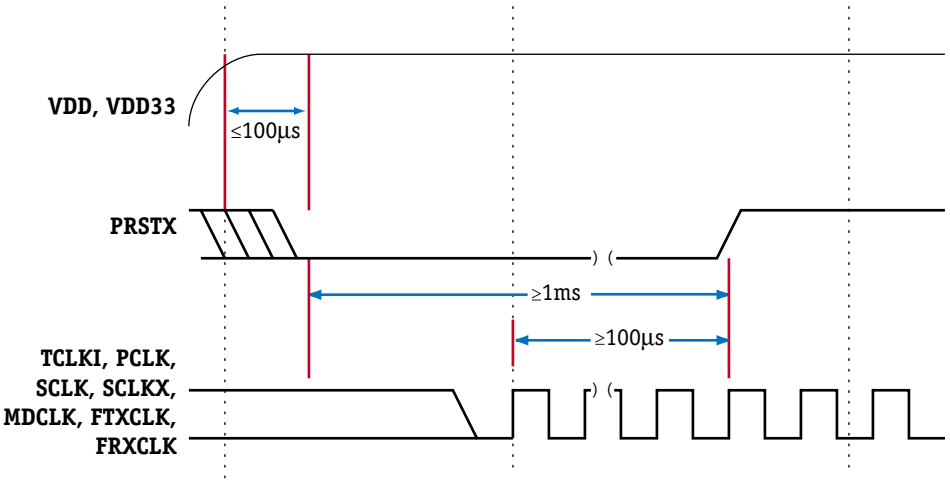
PARAMETER	TYPICAL	UNIT
All Pins	5	pF

Power Sequencing

It is intended that the VDD and VDD33 rails are sequenced to their final value together for most applications.

It is also required that SCLK, SCLKX, TCLKI, PCLK, MDCLK, FTXCLK, and FRXCLK be running or begin running during power sequencing to propagate reset inside the C-5e NP. Figure 9 indicates the relationship between the clocks and PRSTX. There is no requirement that the asserting and deasserting edges of PRSTX be synchronous to the clocks. Reset must be asserted within 100µs of power initiation. Typically, reset is held low during power initiation.

Figure 9 Bringup Clock Timing Diagram



Power and Thermal Characteristics

Table 39 provides the derived power and thermal characteristics for the production version of the C-5e NP.

Table 39 C-5e Network Processor Power and Thermal Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Power Dissipation, P_D	TBD	9.2	13.0	W	266MHz core clock See Note below
Maximum Junction Temperature, T_J			125	°C	See Note below
Thermal Resistance, junction to case, θ_{JC}		<0.1		°C/W	See Note below
Thermal Resistance, junction to printed circuit board, θ_{JB}		TBD		°C/W	See Note below

Table 39 *note: Power dissipation values assume the following conditions:*

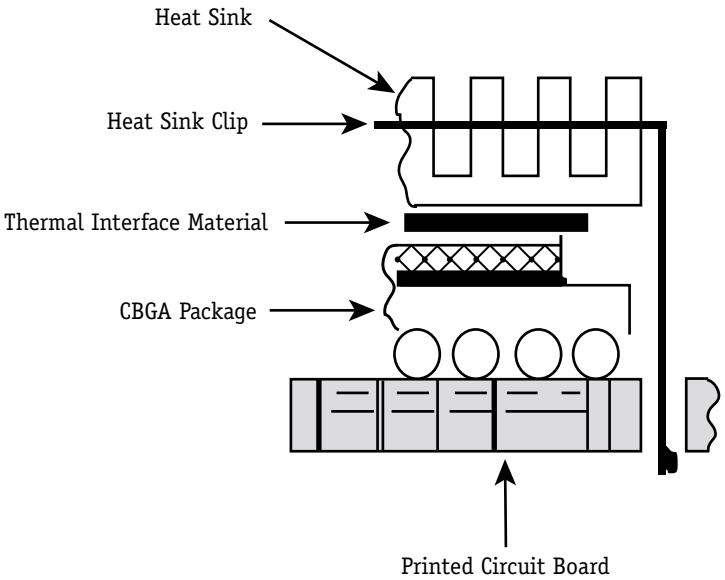
- *BMU memory operating at 133MHz.*
- *TLU memory operating at 133MHz.*
- *QMU operating at 175MHz.*
- *VDD = 1.2V, VDD33 = 3.3V, TJ at approximately 50°C for typical values. VDD and VDD33 are 5% higher for maximum values.*
- *"Minimum" PD based on idle condition (clocks running and no programs executing).*
- *"Typical" PD based on test application that implements Fast Ethernet forwarding actively running on all CPs.*
- *"Maximum" PD based on maximum consumption for any high-bandwidth communications application executing on all CPs, FP, and XP.*

Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (refer to Figure 10); however, due to the potential

large mass of the heat sink, attachment through the printed circuit board is suggested. If a spring clip is used, the spring force should not exceed 5.5 pounds.

Figure 10 Package Cross Section View with Several Heat Sink Options



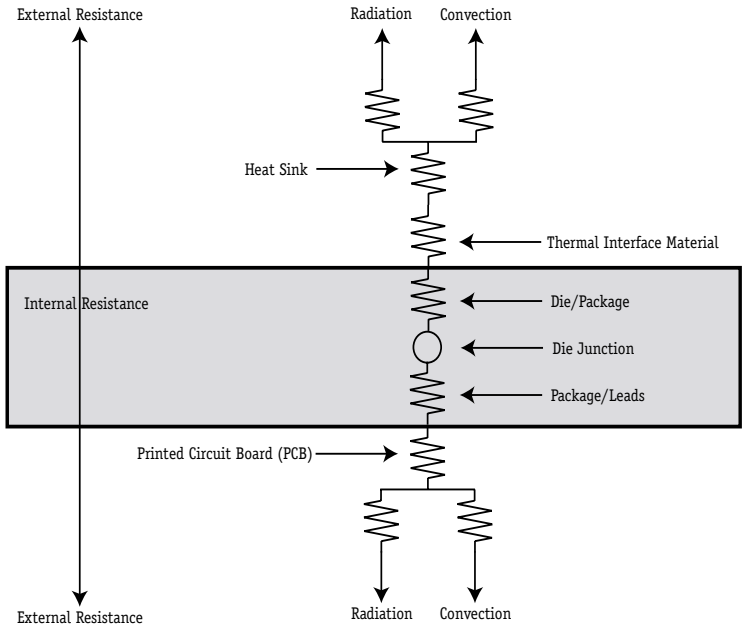
Internal Package Conduction Resistance

For the exposed-die packaging technology the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 11 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 11 Package with Heat Sink Mounted to the Printed Circuit Board



Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by convection.

Because the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.

Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 39. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1.5°C/W. For example, assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $\theta_{jc} = 0.1$, and a maximum power consumption (P_d) of 13.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.5°C/W + \theta_{sa}) \times 13.0\ W$

For this example, a θ_{sa} value of 5.3°C/W or less is required to maintain the die junction temperature below the maximum value of Table 39.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection,and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as system-level designs.

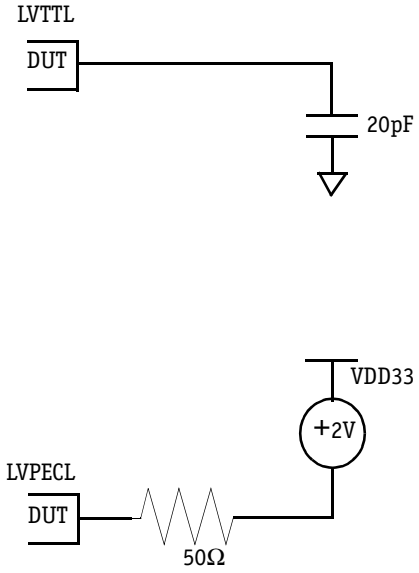
AC Timing Specifications

AC timing specifications consist of input requirements and output responses. The input requirements include setup and hold times, pulse widths, and high and low times. The output responses include delays from clock to signal. The AC timing specifications are defined separately for each interface to the C-5e NP.

Unless otherwise noted, all AC specifications were tested within the functional operating range.

See Figure 12. Output timing specifications for LVTTL pins are given with a 20pF load on the output. Other loads can be simulated with the IBIS model available from Motorola. The LVPECL driver is specified into a 50Ω load terminated to a (VDD33 - 2V) reference.

Figure 12 Test Loading Conditions



Clock Timing Specifications

The system clock timing is shown in Figure 13 and described in Table 40.

Figure 13 System Clock Timing Diagram

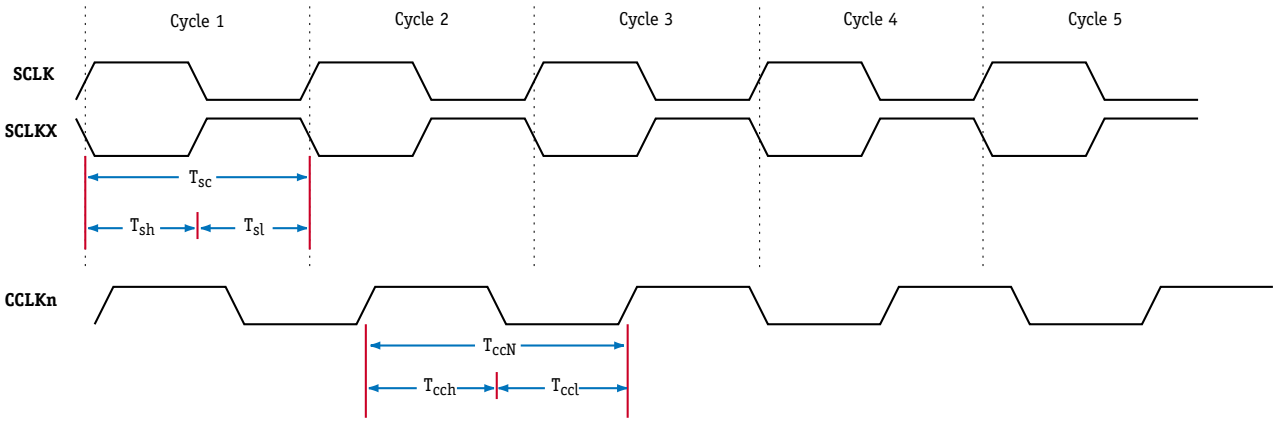


Table 40 System Clock Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tsc	System Cycle Time	3.76			ns	266MHz core clock
Tsh	Sys Clk High Pulse	45		55		Duty cycle*
Tsl	Sys Clk Low Pulse	45		55		Duty cycle*
Tcc0	CCLK0 Cycle Time		647.67		ns	T1†
Tcc1	CCLK1 Cycle Time		488.28		ns	E1†
Tcc2	CCLK2 Cycle Time		29.097		ns	E3†
Tcc3	CCLK3 Cycle Time		22.353		ns	T3†
Tcc4	CCLK4 Cycle Time		20.00		ns	RMII†
Tcc5	CCLK5 Cycle Time		9.412		ns	Fibre Channel†
Tcc6	CCLK6 Cycle Time		8.00		ns	GMII†
Tcc7	CCLK7 Cycle Time		6.43		ns	OC-3†
Tcch	CCLKm High Time	40%		60%		% cycle pulse is high
Tccl	CCLKm Low Time	40%		60%		% cycle pulse is low

* Pulse duty cycle measured at crossing voltage of SCLK/SCLKX

† The frequencies specified for CCLK0 - CCLK7 allow full flexibility for the C-5e NP. It is also possible to use one or more CCLK*n* inputs for other frequencies; contact your Motorola representative for more information.

CP Timing Specifications

This section describes the timing for the following CP interfaces:

- DS1/DS3
- 10/100 Ethernet
- Gigabit Ethernet
- OC-3
- OC-12

DS1/DS3 Timing Specifications

The DS1/DS3 interface timing is shown in Figure 14 and described in Table 41.

Figure 14 DS1/DS3 Ethernet Timing Diagram

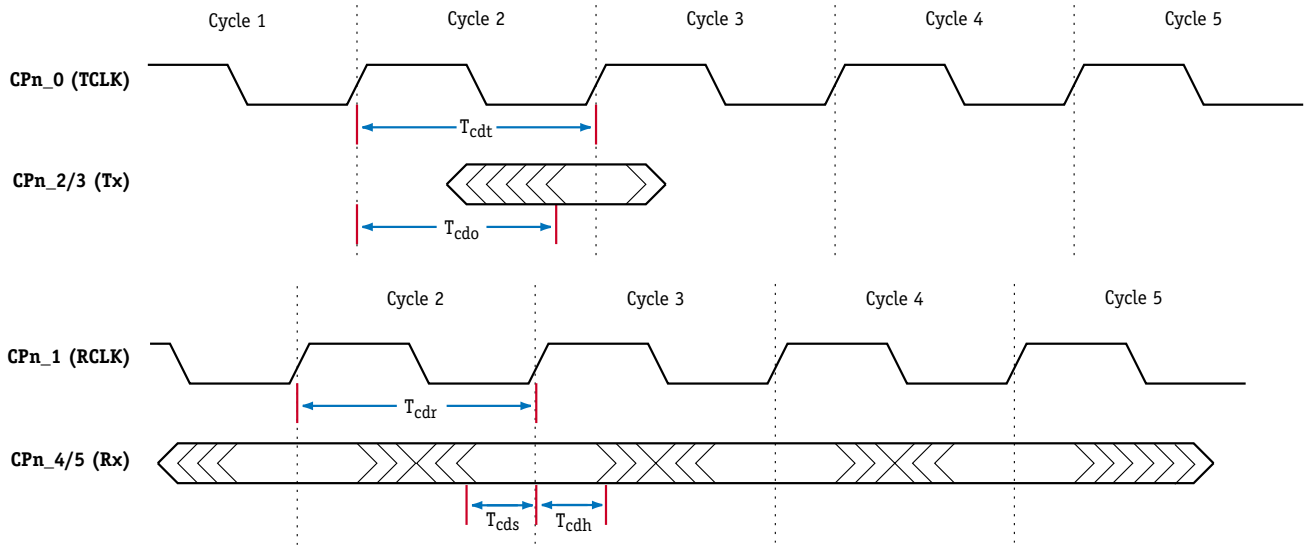


Table 41 DS1/DS3 Ethernet Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tcdt	DS1/DS3 Transmit Cycle Time		647/22.4		ns
Tcdo	DS1/DS3 Output Time	3.0/3.0		400/15.0	ns
Tcdr	DS1/DS3 Receive Cycle Time		647/22.4		ns

Table 41 DS1/DS3 Ethernet Timing Description (continued)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tcds	DS1/DS3 Setup Time	2.0			ns
Tcdh	DS1/DS3 Hold Time	0			ns

10/100 Ethernet Timing Specifications

The 10/100 Ethernet interface timing is shown in Figure 15 and described in Table 42.

Figure 15 10/100 Ethernet Timing Diagram

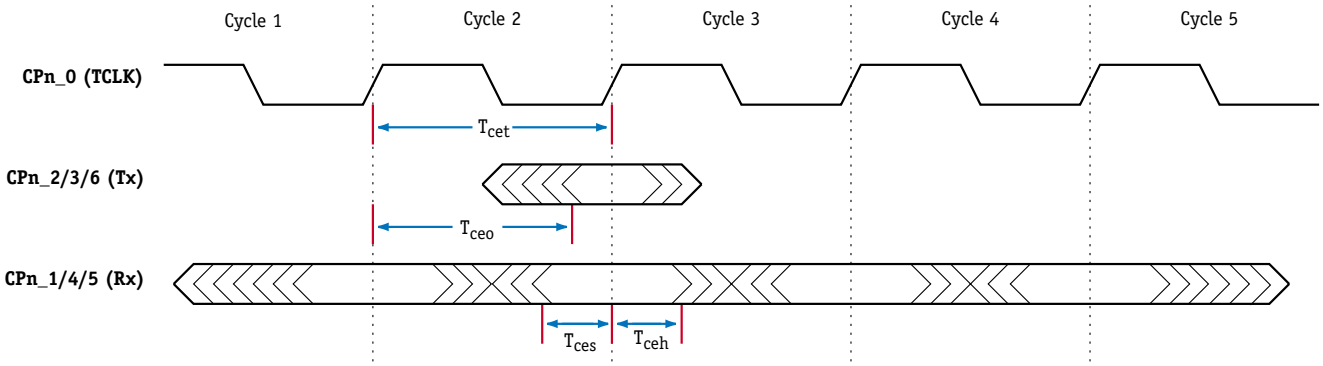


Table 42 10/100 Ethernet Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tcet	Transmit Cycle Time*		20		ns
Tceo	Output Time	3.0		15.0	ns
Tces	Setup Time	2.0			ns
Tceh	Hold Time	0			ns

* STD/Fast Ethernet

Gigabit GMII Ethernet, TBI and MII Interface Timing Specifications

The Gigabit GMII Ethernet interface timing is shown in Figure 16 and described in Table 43. The TBI interface timing is shown in Figure 16 and described in Table 44.

Figure 16 Gigabit Ethernet and TBI Interface Timing Diagram

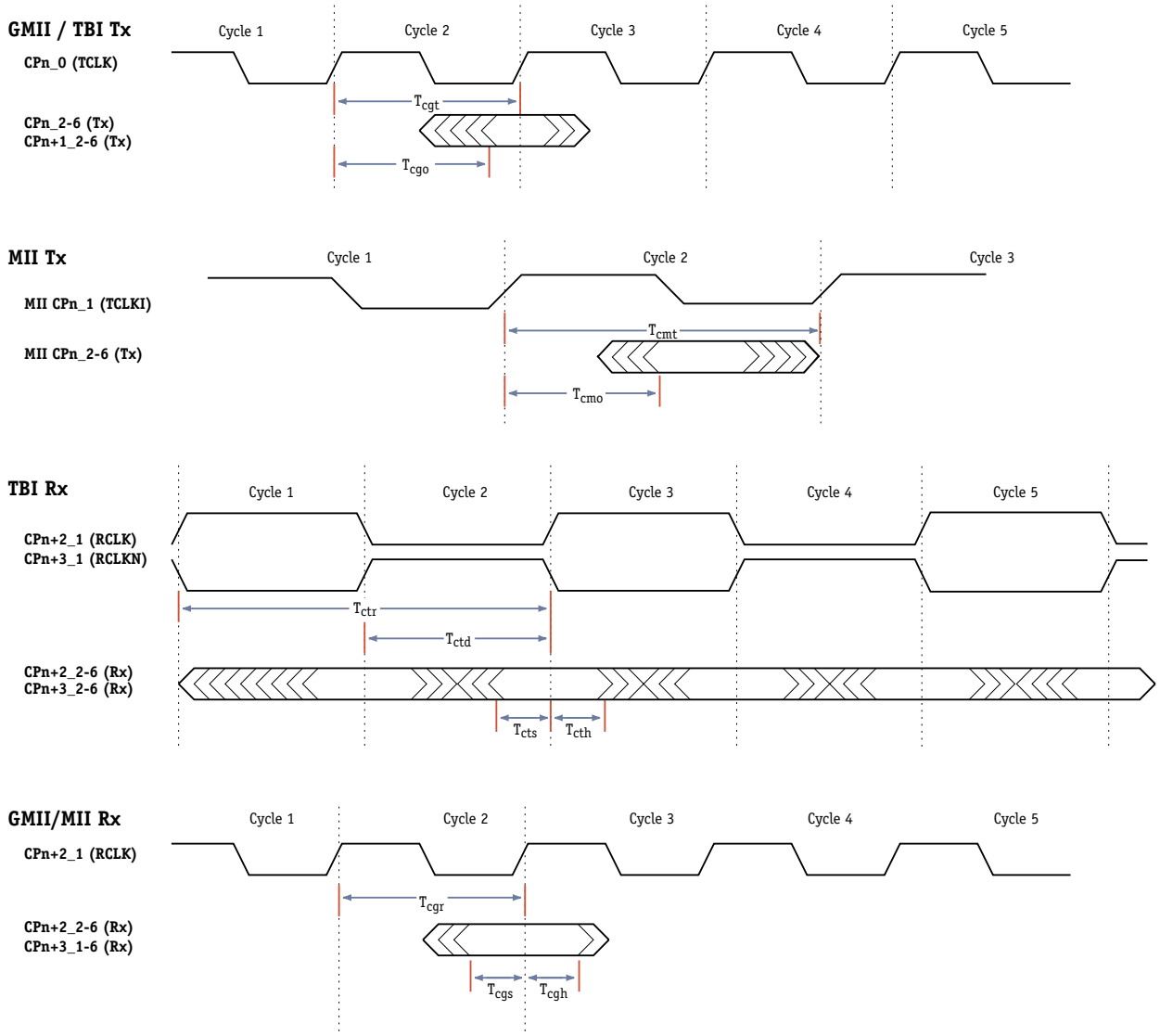


Table 43 Gigabit GMII/MII Ethernet Interface Timing Description

SYMBOL GIGABIT	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tcgt	Transmit Cycle Time, GMII		8.0		ns	
Tcgo	Output Time, GMII	3.0		6.0	ns	
Tcgr	Receive Cycle Time		8.0		ns	
Tcgs	Setup Time	2.0			ns	
Tcgh	Hold Time	0.0			ns	
Tcmt	Transmit Cycle Time, MII		40/400		ns	100BaseT/10BaseT
Tcmo	Output Time, MII	2		12	ns	

Table 44 Gigabit TBI Interface Timing Description

SYMBOL TBI	PARAMETER	MIN	TYP	MAX	TOL	UNIT
Tctt	Transmit Cycle Time		8.0			ns
Tcto	Output Time	3.0		6.0*		ns
Tctr	Receive Cycle Time		16.0			ns
Tctd	Rclk/Rclkn Deviation				1.0	ns
Tcts	Setup Time	2.0				ns
Tcth	Hold Time	0.0				ns

* For Fibre Channel applications this value is 7.0ns for a transmit cycle time of 9.4ns.

OC-3 Timing Specifications

The OC-3 interface timing is shown in Figure 17 and described in Table 45.

Figure 17 OC-3 Timing Diagram

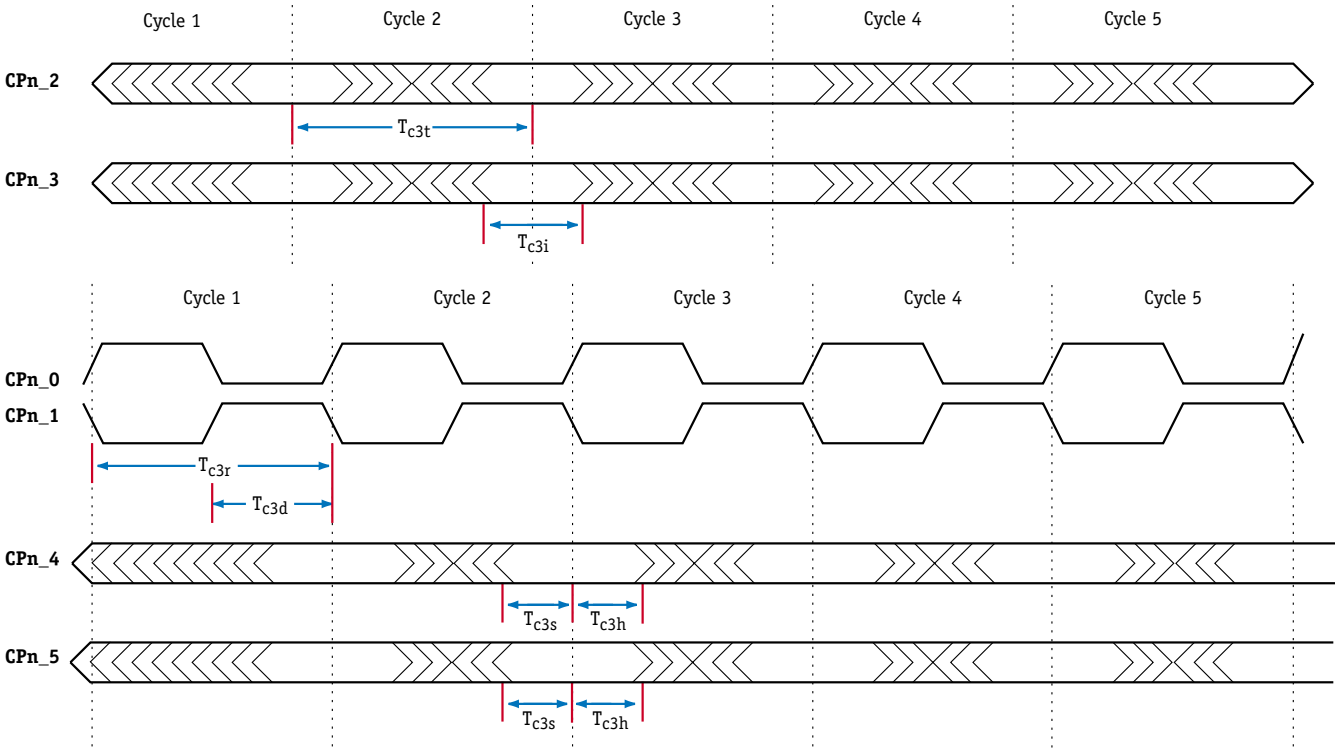


Table 45 OC-3 Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tc3t	OC-3 Transmit Cycle Time		6.43		ns
Tc3i	OC-3 Pulse Width	2.0			ns
Tc3r	OC-3 Receive Cycle Time*	6.0			ns
Tc3d	OC-3 Clock Duty Cycle	40		60	%
Tc3s	OC-3 Setup Time	2.0			ns
Tc3h	OC-3 Hold Time	0.0			ns

* 155.52MHz

OC-12 Timing Specifications

The OC-12 interface timing is shown in Figure 18 and described in Table 46.

Figure 18 OC-12 Timing Diagram

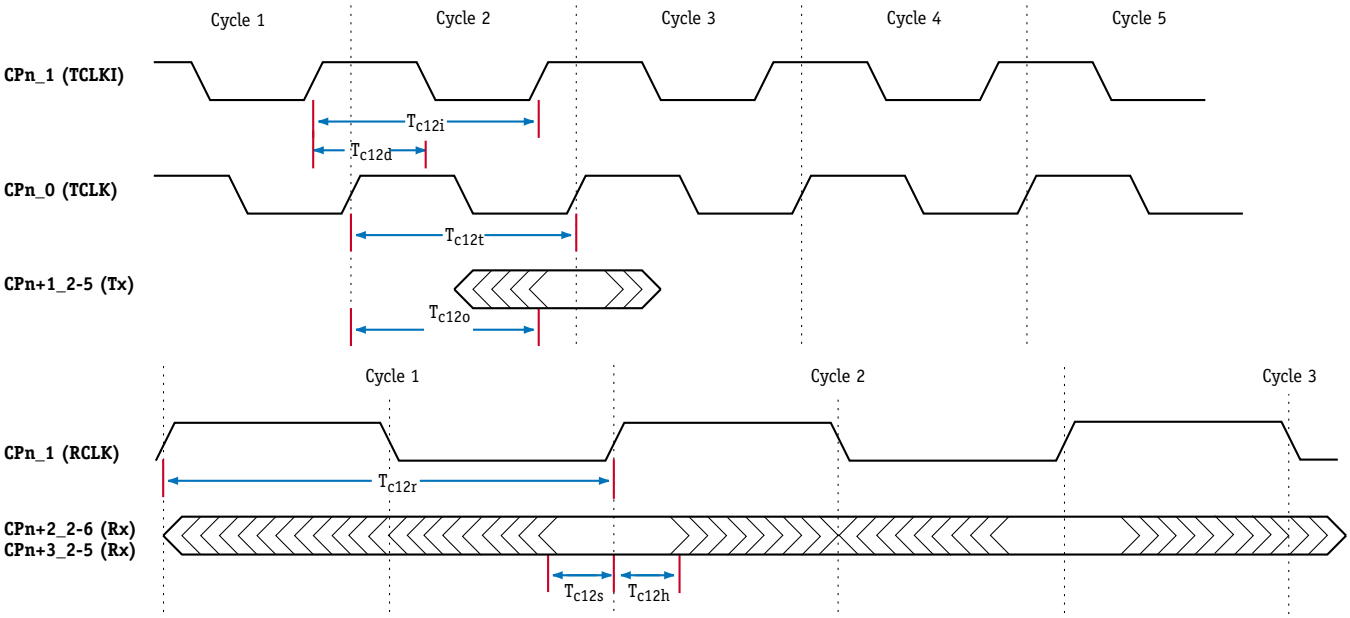


Table 46 OC-12 Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tc12i	OC-12 Transmit Cycle Time*		12.86		ns
Tc12d	OC-3 Clock Duty Cycle	40		60	%
Tc12t	OC-12 Transmit Cycle Time†		12.86		ns
Tc12o	OC-12 Output Time‡	3.0		10.0	ns
Tc12r	OC-12 Receive Cycle Time	12.0	12.86		ns
Tc12s	OC-12 Setup Time	2.0			ns
Tc12h	OC-12 Hold Time	0.0			ns

* Input from PHY
† Output from C-5e NP
‡ Aligned to TCLK

Executive Processor Timing Specifications

The XP timing specifications include:

- PCI Timing Specifications
- MDIO Serial Interface Timing Specifications
- Low Speed Serial Interface Timing Specifications
- PROM Interface Timing Specifications

PCI Timing Specifications

The PCI timing is shown in Figure 19 and described in Table 47.

Figure 19 PCI Timing Diagram

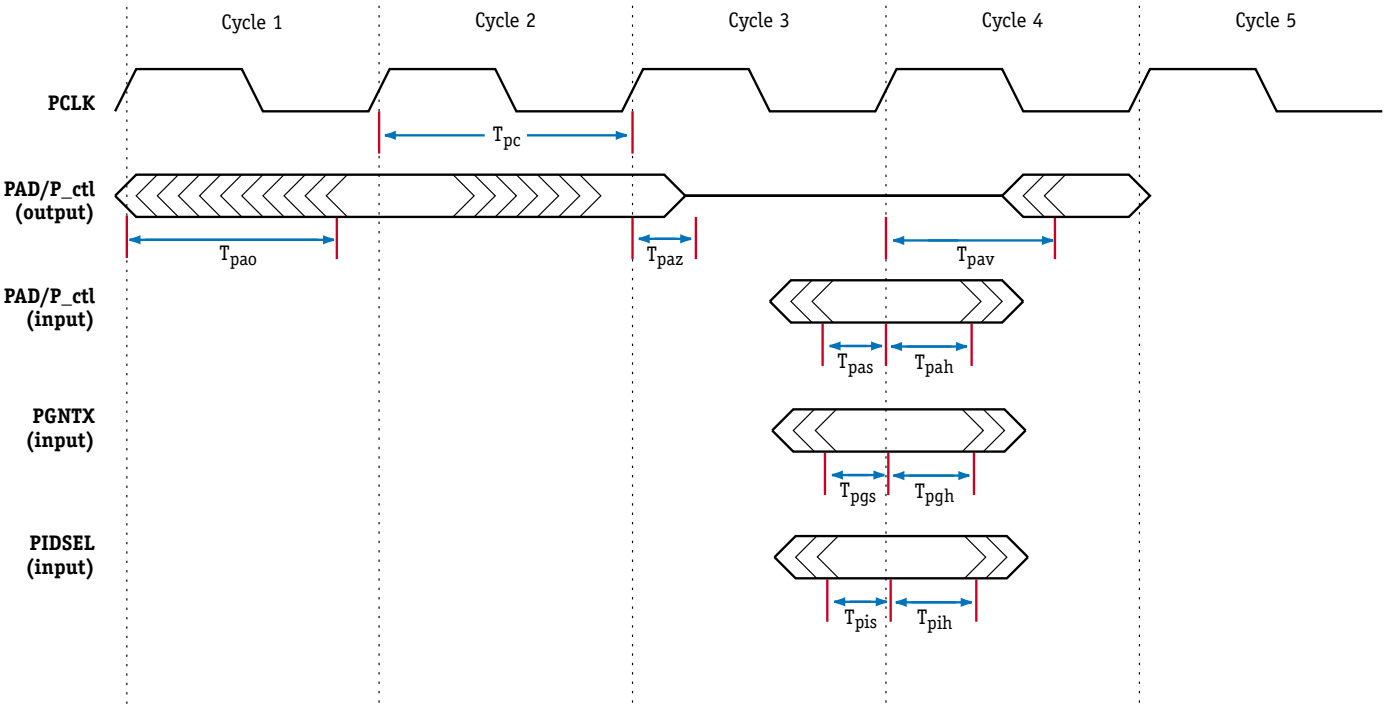


Table 47 PCI Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tpc	PCI Cycle Time*	15.0			ns
Tpas	PAD/P_ctl† Setup	3.0			ns
Tpah	PAD/P_ctl Hold	0.0			ns
Tpao	PAD/P_ctl Output	2.0		6.0	ns
Tpaz	PAD/P_ctl Clk to Tri‡	2.0		6.0	ns
Tpav	PAD/P_ctl Clk to Driven‡	2.0		6.0	ns
Tpgs	PGNTX Setup	5.1			ns
Tpgh	PGNTX Hold	0.0			ns
Tpis	PIDSEL Setup	3.0			ns
Tpih	PIDSEL Hold	0.0			ns
	PRSTX**				ns
	PINTA**				ns

* 66MHz PCI

† P_ctl includes all PCI control parameters including: PPAR, PFRAMEX, PTRDYX, PIRDYX, PSTOPX, PDEVSELX, PPERRX, PSERRX

‡ Not fully tested, values based on design/characterization.

** Asynchronous

MDIO Serial Interface Timing Specifications

The MDIO serial interface timing is shown in Figure 20 and described in Table 48.

Figure 20 MDIO Serial Interface Timing Diagram

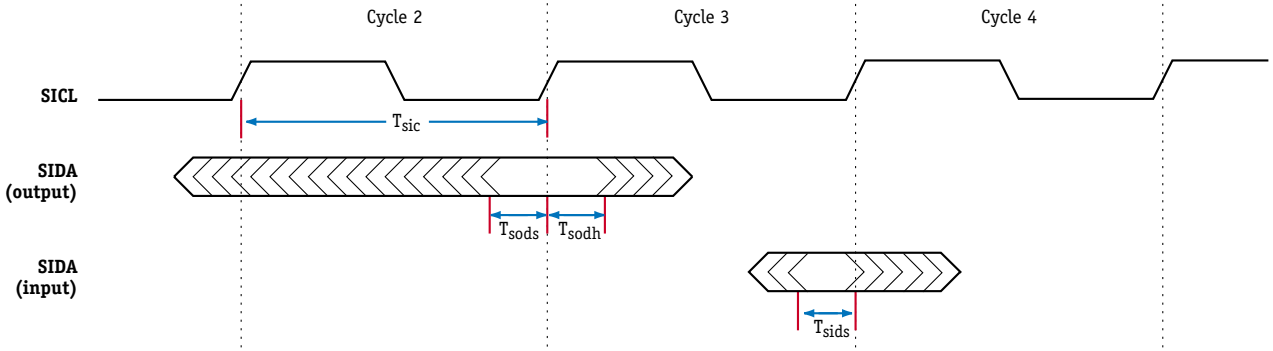


Table 48 MDIO Serial Interface Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tsic	SICL Cycle Time	40			ns
Tsids	SIDA Input Setup	10			ns
Tsidh	SIDA Input Hold	0.0			ns
Tsods	SIDA Output Setup	10			ns
Tsodh	SIDA Output Hold	10			ns

Low Speed Serial Interface Timing Specifications

The low speed serial interface timing is shown in Figure 21 and described in Table 49.

Figure 21 Low Speed Serial Interface Timing Diagram

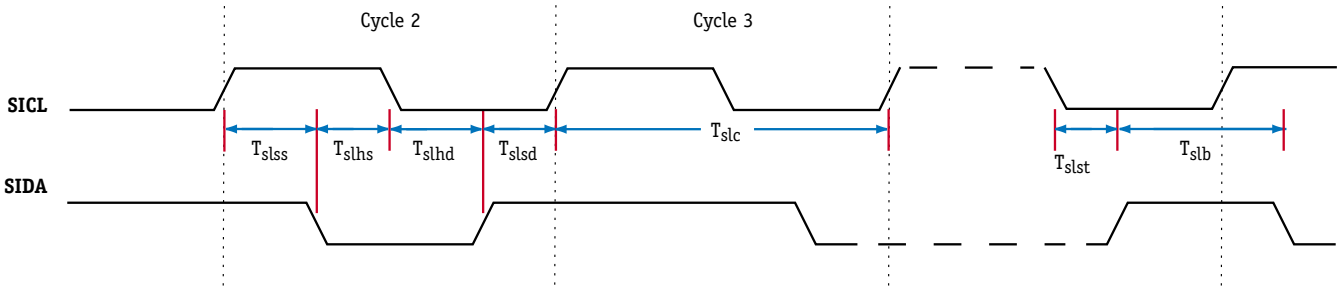


Table 49 Low Speed Serial Interface Timing Description

SYMBOL	PARAMETER	MIN	MAX	UNIT
Tslc	SICL Cycle Time	2500		ns
Tslss	Set-up Time for Repeated START Condition	600		ns
Tslhs	Hold Time START Condition	600		ns
Tslsd	Data Set-up Time	250		ns
Tslhd	Data Hold Time	0.0		ns
Tslst	Set-up Time for STOP Condition	600		ns
Tslb	Bus Free Time Between a STOP and START Condition	1250		ns
Cmax	Capacitive load for each line of the bus		400	pF

PROM Interface Timing Specifications

The PROM interface timing is shown in Figure 22 and described in Table 50.

Figure 22 PROM Interface Timing Diagram

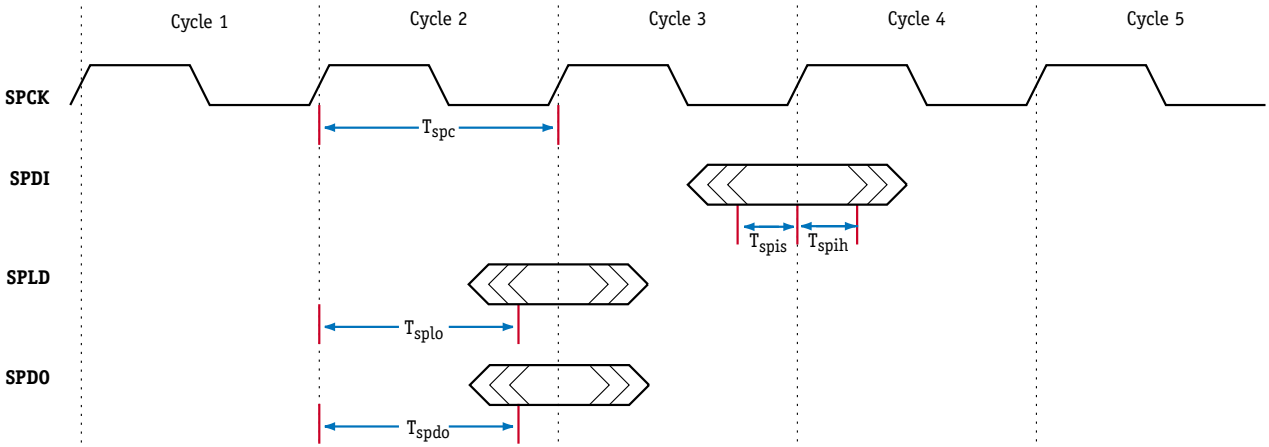


Table 50 PROM Interface Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tspc	SPCK Cycle Time	40.0			ns
Tspis	SPDI Setup	10.0			ns
Tspih	SPDI Hold	0.0			ns
Tsplo	SPLD Output	Tsc		Tsc + 3.0	ns
Tspdo	SPDO Output	Tsc		Tsc + 3.0	ns

Fabric Processor Timing Specifications

The FP timing specifications are shown in Figure 23 and described in Table 51.

Figure 23 Fabric Processor Timing Diagram

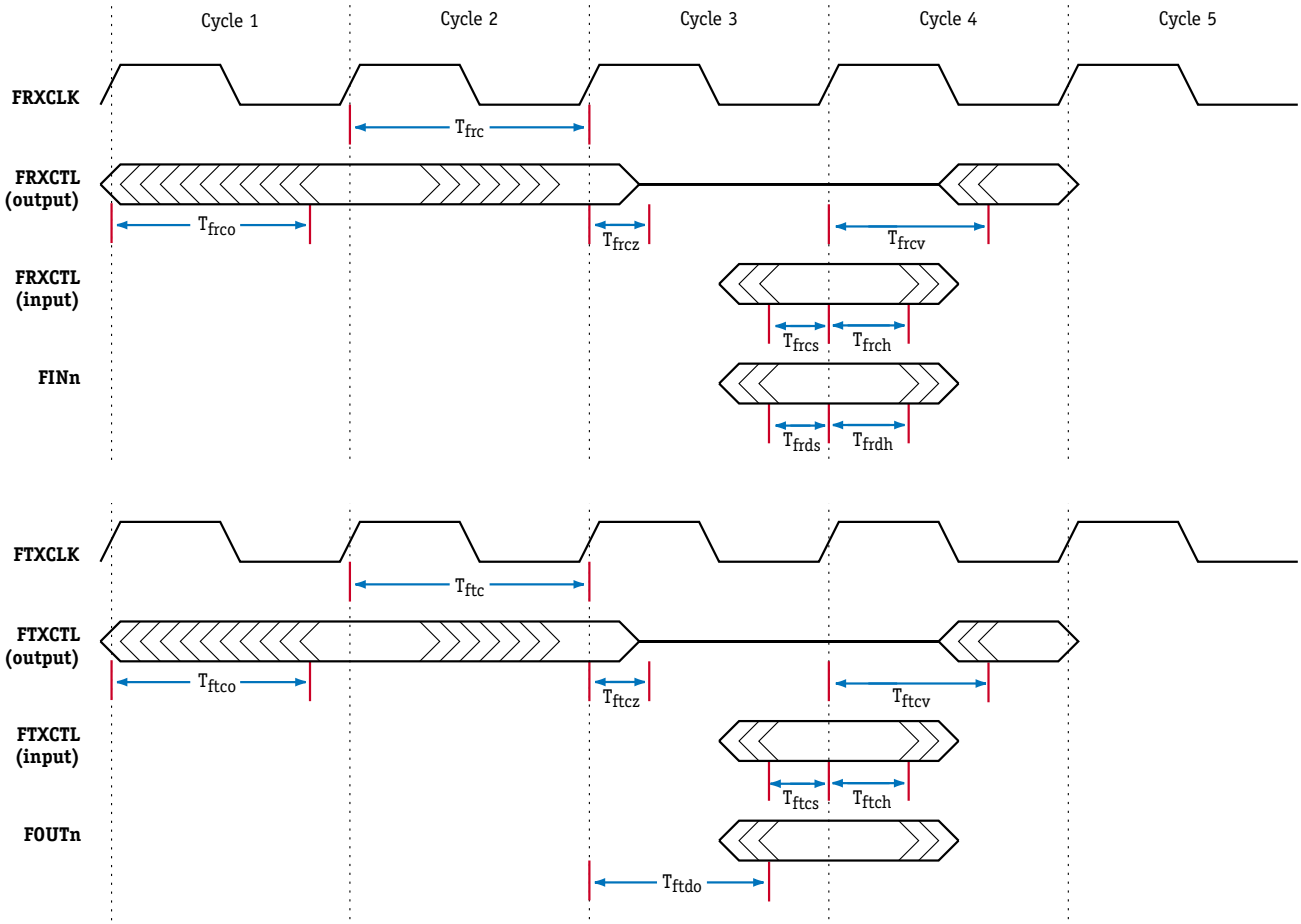


Table 51 Fabric Processor Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tfrc	FRX Cycle Time	8.0			ns	
Tfrcs	FRXCTL Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tfrch	FRXCTL Hold	0.0			ns	
Tfrco	FRXCTL Output	1.0		4.0	ns	
Tfrcz	FRXCTL Clk to Tri*	1.0		4.0	ns	
Tfrcv	FRXCTL Clk to Driven*	1.0		4.0	ns	
Tfrds	FIN Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tfrdh	FIN Hold	0.0			ns	
Tftc	FTX Cycle Time	8.0			ns	
Tftcs	FTXCTL Setup	4.0 1.5			ns	Utopia2 Mode All other modes
Tftch	FTXCTL Hold	0.0			ns	
Tftco	FTXCTL Output	1.0		4.0	ns	
Tftcz	FTXCTL Clk to Tri*	1.0		4.0	ns	
Tftcv	FTXCTL Tri to Driven*	1.0		4.0	ns	
Tftdo	FOUT Output	1.0		4.0	ns	

* Not fully tested, values based on design/characterization.

BMU Timing Specifications

The BMU timing specifications are shown in Figure 24 and described in Table 52.

The BMU synchronous DRAM interface is PC100-compliant and designed to work with industry standard SDRAM components with 12 or fewer address lines. The information below is intended to provide the output, setup, and hold data required to design this interface without duplicating the transaction waveform diagrams in SDRAM data sheets.

Figure 24 BMU Timing Diagram

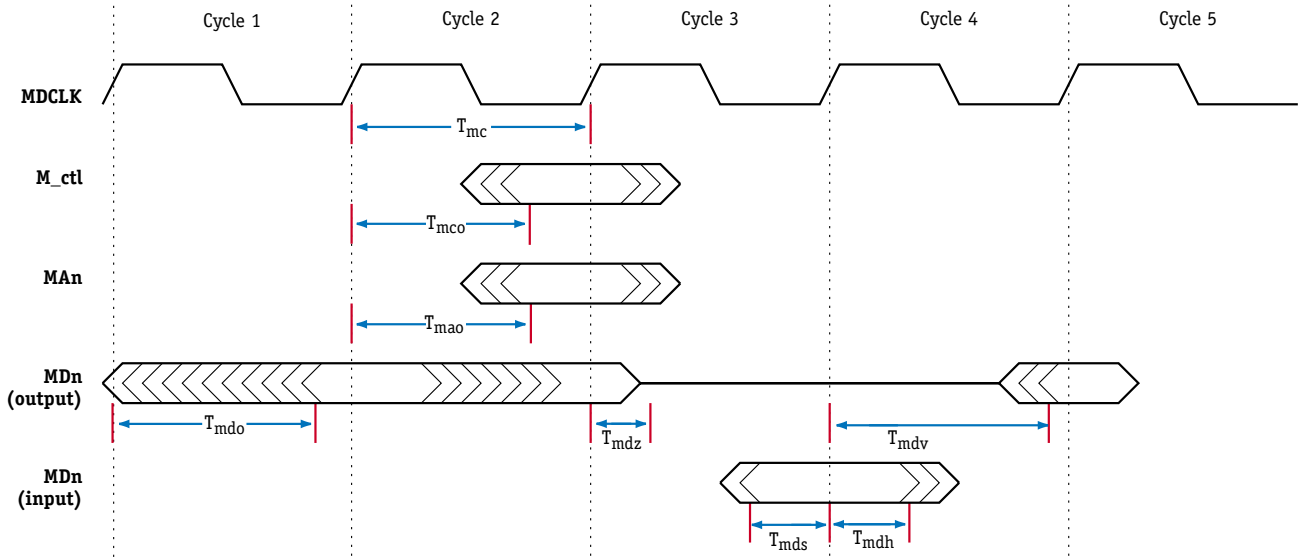


Table 52 BMU Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Tmc	BMU Cycle Time	7.5			ns
Tmco	BMU Ctrl Output	0.8		3.4	ns
Tmao	BMU Addr Output	0.8		3.4	ns
Tmds	BMU Data Setup	0.5			ns
Tmdh	BMU Data Hold	1.1			ns
Tmdo	BMU Data Output	0.8		4.0	ns
Tmdz	BMU Data Clk to Tri*	0.8		4.0	ns
Tmdv	BMU Data Clk to Driven*	0.8		4.0	ns

* Not fully tested, values based on design/characterization.

Table 53 Signal Groups in BMU Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Control (M_ctl)	MBA0, MBA1, MCASX, MRASX, MWEX, MCSX, MDQM, MDQML
Address (MAn)	MA0 - MA11
Data (MDn)	MD0 - MD129, MDECC0 - MDECC8

TLU Timing Specifications

The TLU timing specifications are shown in Figure 25 and described in Table 54.

Figure 25 TLU Timing Diagram

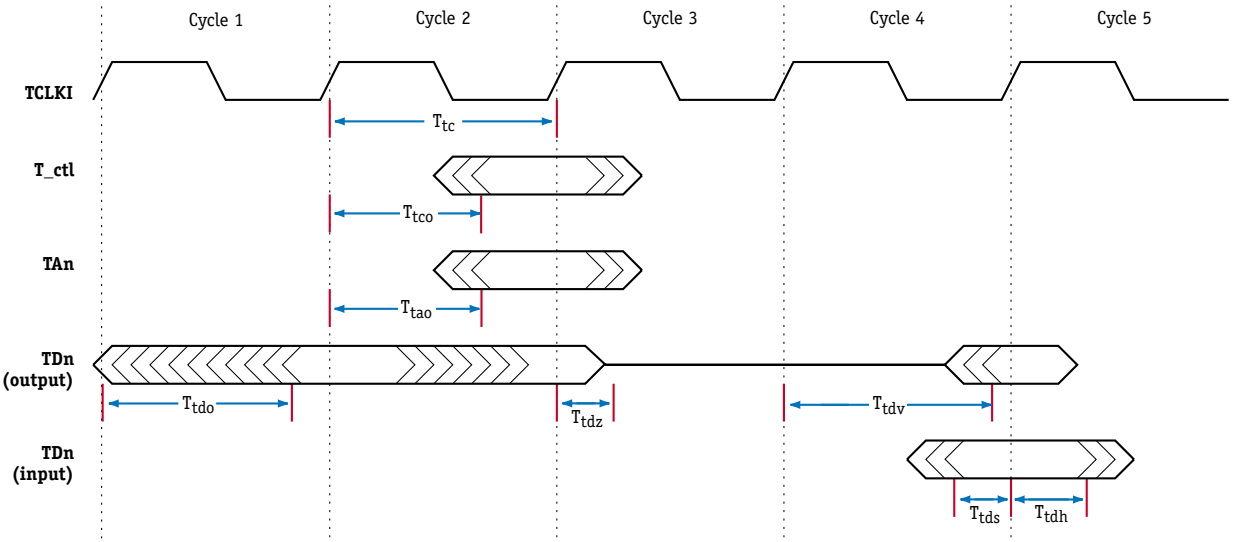


Table 54 TLU Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
Ttc	TLU Cycle Time	7.5			ns
Ttco	TLU Ctrl Output	0.8		3.4	ns
Ttao	TLU Addr Output	0.8		3.4	ns
Ttds	TLU Data Setup	1.0			ns
Ttdh	TLU Data Hold	1.2			ns
Ttdo	TLU Data Output	0.8		3.7	ns
Ttdz	TLU Data Clk to Tri*	0.8		3.7	ns
Ttdv	TLU Data Clk to Driven*	0.8		3.7	ns

* Not fully tested, values based on design/characterization.

Table 55 Signal Groups in TLU Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Control (T_ctl)	TCE0X - TCE3X, TWE0X - TWE3X
Address (TAn)	TA0 - TA21

Table 55 Signal Groups in TLU Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Data (TDn)	TD0 - TD63, TPAR0-3

QMU SRAM (Internal Mode) Timing Specifications

The QMU SRAM (Internal Mode) timing specifications are shown in Figure 26 and described in Table 56.

Figure 26 QMU SRAM (Internal Mode) Timing Diagram

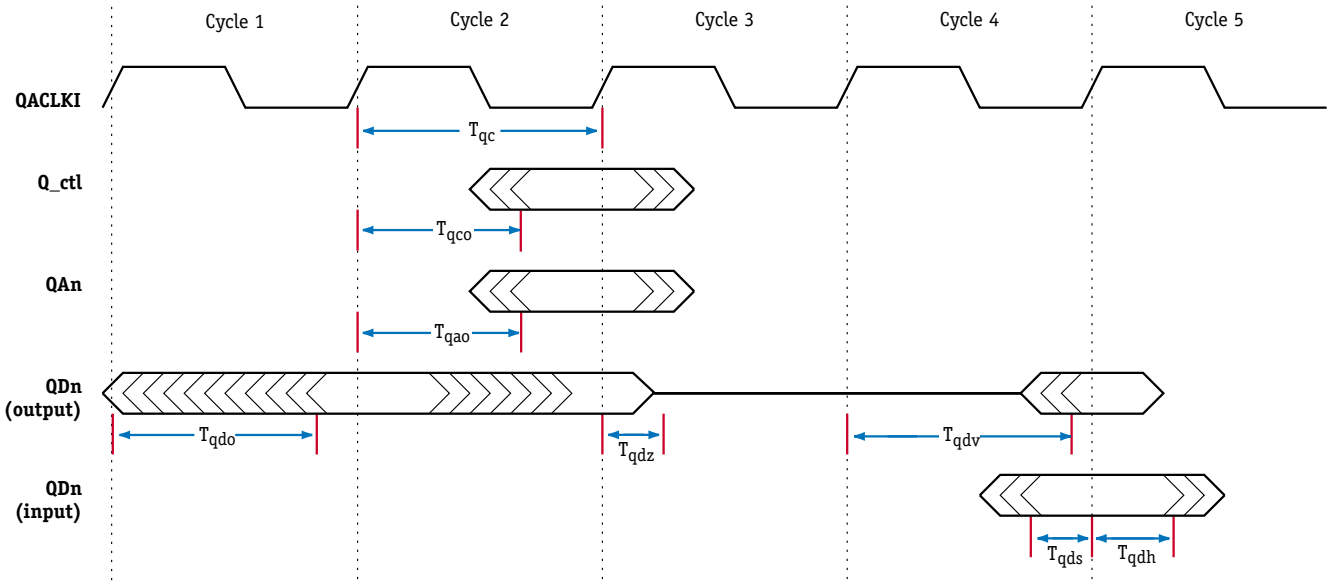


Table 56 QMU SRAM (Internal Mode) Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tqc	QMU Cycle Time	5.7			ns	
Tqco	QMU Ctrl Output	0.8		3.4	ns	Loading is 50Ω transmission line.
Tqao	QMU Addr Output	0.8		3.4	ns	Loading is 50Ω transmission line.

Table 56 QMU SRAM (Internal Mode) Timing Description (continued)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tqds	QMU Data Setup	0.8			ns	
Tqdh	QMU Data Hold	0.8			ns	
Tqdo	QMU Data Output	0.9		3.4	ns	Loading is 50Ω transmission line.
Tqdz	QMU Data Clk to Tri*	0.9		3.4	ns	
Tqdv	QMU Data Clk to Driven*	0.9		3.4	ns	

* Not fully tested, values based on design/characterization.

Table 57 Signal Groups in QMU SRAM (Internal Mode) Timing Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Control (Q_ctl)	QWEX
Address (QAn)	QA0-QA16
Data (QDn)	QD0-QD31, QDPL, QDPH

QMU to Q-5 (External Mode) Timing Specifications

The QMU to Q-5 (External Mode) timing specifications are shown in Figure 27 and described in Table 58.

Figure 27 QMU to Q-5 (External Mode) Timing Diagram

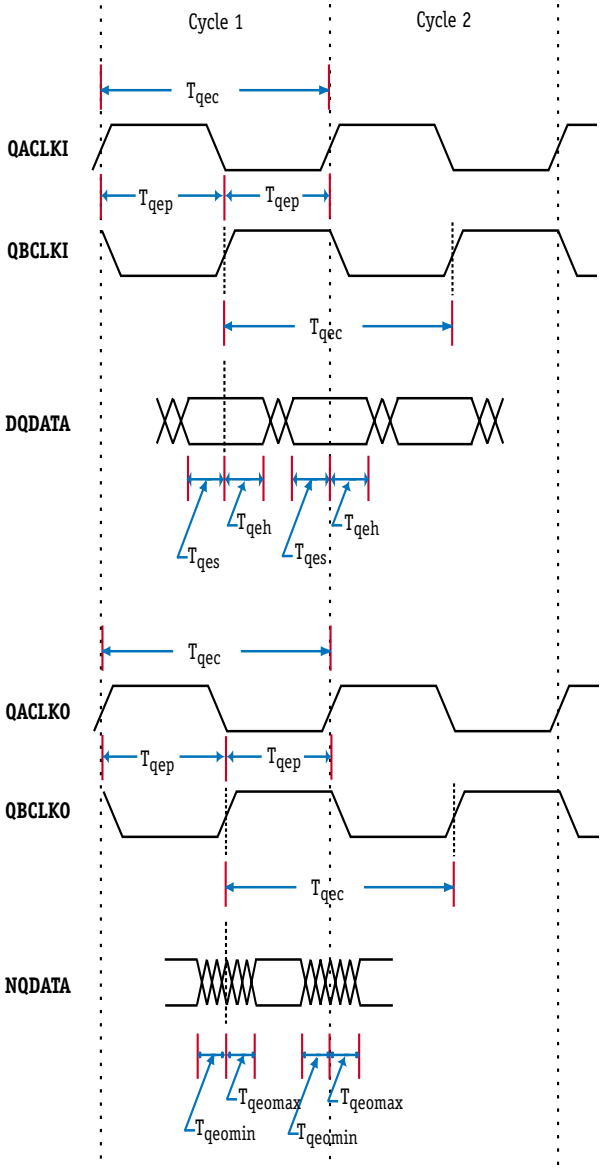


Table 58 QMU to Q-5 (External Mode) Timing Description

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	COMMENT
Tqec	QMU External Cycle Time	10.0			ns	QACLKO/QBCLKO derived from QACLKI/QBCLKI
Tqep	QMU CLKA-CLKB delta between rising edges	4.8			ns	
Tqes	QMU Input Data Setup	0.6			ns	
Tqeh	QMU Input Data Hold	0.8			ns	
Tqeo	QMU Data Output	-.85		1.3	ns	Determines valid time for data from each clock rising edge

Table 59 Signal Groups in QMU to Q-5 (External Mode) Timimg Diagrams

SIGNAL GROUP	INCLUDED SIGNALS
Input Clocks (QnCLKI)	QACLKI, QBCLKI
Output Clocks (QnCLKO)	QACLKO, QBCLKO
Input Data (DQDATA)	QD0-23, QARDY, QDPL, QDPH, QNQRDY, QDQPAR
Output Data (NQDATA)	QA0-16, QWEX, QD24-31

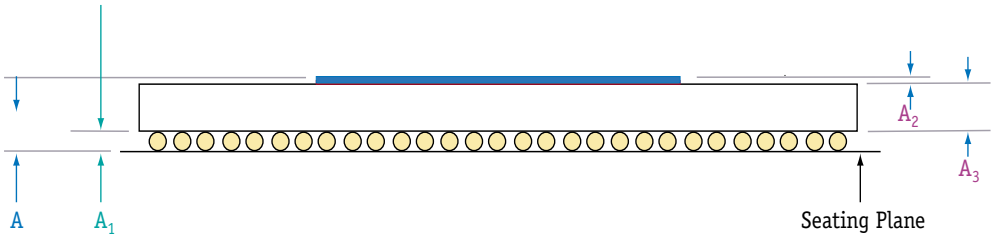
Chapter 4

MECHANICAL SPECIFICATIONS

Package Views

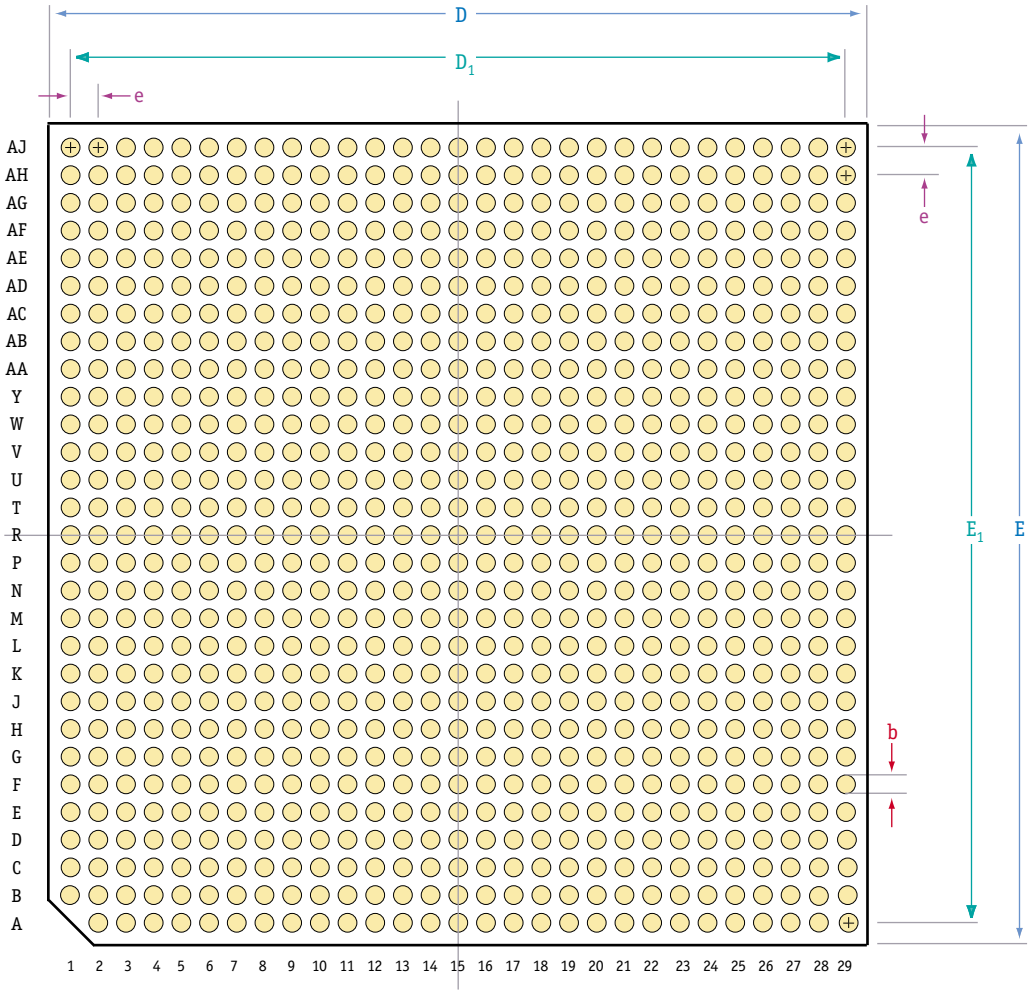
The C-5e network processor is an 840 pin (29 pins x 29 pins) Ball Grid Array (BGA) package as shown in the following illustrations. Table 60 defines the package measurements.

Figure 28 C-5e Network Processor BGA Package Side View



HiTCE: Green ceramic is thermally matched to FR4 circuit board.

Figure 29 C-5e Network Processor BGA Package (Bottom View)



Package Measurements

Table 60 defines the C-5e NP package measurements, providing nominal, minimum, and maximum sizes where appropriate.

Table 60 Package Measurements (Reference Figure 28 and Figure 29 for Symbols)

SYMBOL	DEFINITION	NOM. (MM)	MIN. (MM)	MAX. (MM)
A	Overall	3.26	2.97	3.26
A_1	Ball height	0.70		
A_2	C4 and Die	0.86		
A_3	Body thickness	1.7	1.55	1.85
D	Body size	31.00	30.80	31.20
D_1	Ball footprint (X)	28.00		
E	Body size	31.00	30.80	31.20
E_1	Ball footprint (Y)	28.00		
e	Ball pitch	1.00		
b	Ball diameter	0.70		

Marking Codes

Table 61 explains the marking on the C-5e NP.

Table 61 C-5e Network Processor Marking Codes

MARKING (EXPLANATION OF CODES)	
Top	Logo/Part#/Country of Origin/Date Code
Bottom	N/A
Pin 1 Marking	Chamfered Corner

Reflow

Typical Reflow Profile for the C-5e Switch Module comprises:

1 Follow the guidelines recommended by your solder paste supplier.

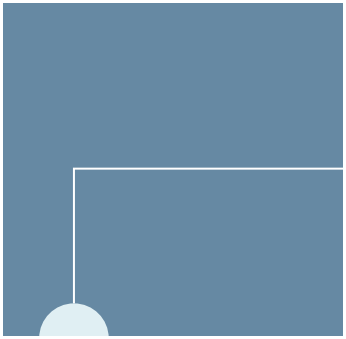
Flux requirements must be met for best solderability.

2 The temperature profile should be carefully characterized to ensure uniform temperature across the board and package.

Solder ball voiding may be affected by ramp rates and dwell times below and above liquidus.

3 A nitrogen atmosphere is not required, but will make the process more robust. It can make a difference for marginally solderable PC board pads.

4 Full convection forced air furnaces work best, but IR, Convection/IR, or vapor phase can be used.



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