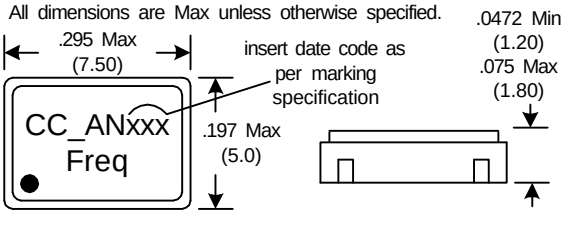
Crystek Corporation

239-561-3311 FAX 239-561-1025

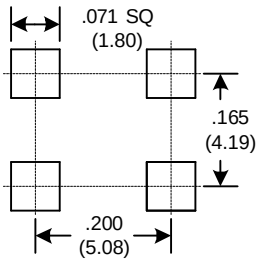
5.0V 5x7 mm SMD HCMOS/TTL Oscillator with High Load

Dimensions inches (mm)
All dimensions are Max unless otherwise specified.



PIN	Function
1	Tri-State
2	GND
3	OUT
4	VDD

SUGGESTED PAD LAYOUT



MARKING SPECIFICATION
1 Crystek Corporation 2 "C" Oscillator 3 Blank = 0/70, E = -40/85 4 Oscillator ID (See Table 1) 5 Date Code Year, i.e. 2 = 2002 6 Date Code Week in 2 week increments, (i.e. M = weeks 25 and 26) 7 Lot Code

1 2 3 4 5 6 7
CC_AN2ME

Crystek Part No.
Example: C3292-10.000MHZ
Example: CE3292-10.000MHZ

40/60		45/55 Symmetry		
Tri-state	ID	Tri-state	ID	Freq. Stability
*3290	C	*3296	AN	+/-100ppm
*3291	P	*3991	BA	+/- 25ppm
*3292	D	*3992	BC	+/- 50ppm
C3295	BS	C3995	BT	+/- 15ppm
C3298	BE	C3998	BG	+/- 20ppm

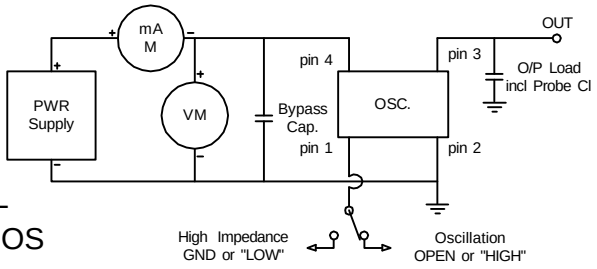
* C = 0/70, * CE = -40/85

Table 1

Frequency Range: 1.0MHz to 125 MHz
Part Number: See Table 1
Options: Operating Temp. (Blank = 0 to 70°C)
(E = -40 to 85°C)
Duty Cycle: 10 TTL @ 1.4v, CMOS @ 50% Vdd
(40/60 % See Table 1)
(45/55 % See Table 1)
Frequency Stability: See Table 1
Input Voltage: 5.0V ± 10%
Input Current: 1.0 MHz - 25.0 MHz , 35 mA Max
25.0 MHz - 50.0 MHz , 45 mA Max
50.0 MHz - 125.0 MHz , 60 mA Max
Output Level: Vol 0.4V Max , Voh 2.4V Min TTL
4.5V Min CMOS

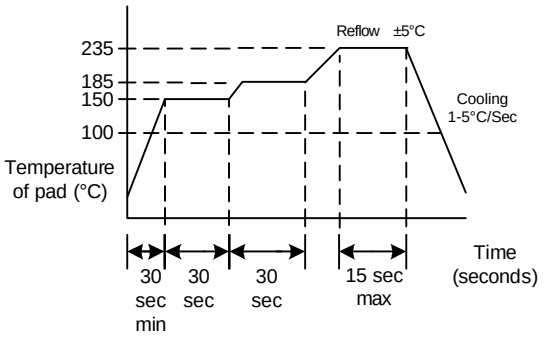
Tri-State Function

Function pin 1	Output pin
Open	Active
"1" level 2.4V Min	Active
"0" level 0.4V Max	High Z



Output Waveform: HCMOS/TTL
Output Load: 50pF Max
Rise & Fall Time: TTL, from 0.8V to 2.4V (4nSec Max)
CMOS, 15pF 20 to 80% (4nSec Max)
CMOS, 30pF 20 to 80% (6nSec Max)
CMOS, 50pF 20 to 80% (6nSec Max)
Aging: <3ppm 1st/yr, 1ppm every year thereafter
Jitter: 100ps max negative transition with respect to the positive transistion (pulse width)
Storage Temperature: -55°C to 125°C
Note: 0.01uF to 0.1uF External Bypass Capacitor Recommeded

RECOMMENDED REFLOW SOLDERING PROFILE



Spec.	a3
Rev.	B