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General Purpose Transistor Arrays

The CA3018 and CA3018A consist of four general purpose silicon NPN transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3018 (obsolete)	-55 to 125	12 Pin Metal Can	T12.B
CA3018A	-55 to 125	12 Pin Metal Can	T12.B

Features

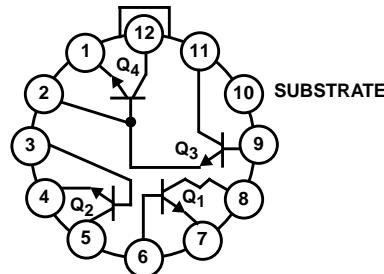
- Matched Monolithic General Purpose Transistors
- h_{FE} Matched ±10%
- V_{BE} Matched
 - CA3018A ±2mV
 - CA3018 ±5mV
- Operation From DC to 120MHz
- Wide Operating Current Range
- CA3018A Performance Characteristics Controlled from 10µA to 10mA
- Low Noise Figure 3.2dB (Typ) at 1kHz
- Full Military Temperature Range -55°C to 125°C

Applications

- Two Isolated Transistors and a Darlington Connected Transistor Pair for Low Power Applications at Frequencies from DC through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, AN5296 "Application of the CA3018 Integrated Circuit Transistor Array" for Suggested Applications

Pinout

CA3018, CA3018A
(METAL CAN)
TOP VIEW



CA3018, CA3018A

Absolute Maximum Ratings

	CA3018	CA3018A
Collector-to-Emitter Voltage, V_{CEO}	15V	15V
Collector-to-Base Voltage, V_{CBO}	20V	30V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)	20V	40V
Emitter-to-Base Voltage, V_{EBO}	5V	5V
Collector Current, I_C	50mA	50mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	200	120
Maximum Power Dissipation (Any One Transistor)	300mW	
Maximum Junction Temperature		175°C
Maximum Storage Temperature Range	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)		300°C

Operating Conditions

Temperature Range -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. The substrate (Terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	CA3018			CA3018A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS									
Collector Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10\text{V}$, $I_E = 0$	-	0.002	100	-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10\text{V}$, $I_B = 0$	-	See Fig. 2	5	-	See Fig. 2	0.5	μA
Collector Cutoff Current Darlington Pair	I_{CEOD}	$V_{CE} = 10\text{V}$, $I_B = 0$	-	-	-	-	-	5	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{mA}$, $I_B = 0$	15	24	-	15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu\text{A}$, $I_E = 0$	20	60	-	30	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu\text{A}$, $I_C = 0$	5	7	-	5	7	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu\text{A}$, $I_{CI} = 0$	20	60	-	40	60	-	V
Collector-to-Emitter Saturation Voltage	V_{CES}	$I_B = 1\text{mA}$, $I_C = 10\text{mA}$	-	0.23	-	-	0.23	0.5	V
Forward Current Transfer Ratio (Note 3) (Figure 3)	h_{FE}	$V_{CE} = 3\text{V}$	$I_C = 10\text{mA}$	-	100	-	50	100	-
			$I_C = 1\text{mA}$	30	100	200	60	100	200
			$I_C = 10\mu\text{A}$	-	54	-	30	54	-
Magnitude of Static-Beta Ratio (Isolated Transistors Q ₁ and Q ₂) (Figure 3)		$V_{CE} = 3\text{V}$, $I_{C1} = I_{C2} = 1\text{mA}$	0.9	0.97	-	0.9	0.97	-	-
Forward Current Transfer Ratio Darlington Pair (Q ₃ and Q ₄) (Figure 4)	h_{FED}	$V_{CE} = 3\text{V}$	$I_C = 1\text{mA}$	1500	5400	-	2000	5400	-
			$I_C = 100\mu\text{A}$	-	-	-	1000	2800	-
Base-to-Emitter Voltage (Figure 5)	V_{BE}	$V_{CE} = 3\text{V}$	$I_E = 1\text{mA}$	-	0.715	-	0.600	0.715	0.800
			$I_E = 10\text{mA}$	-	0.800	-	-	0.800	0.900
Input Offset Voltage (Figures 5, 7)	$ V_{BE1} $ $- V_{BE2} $	$V_{CE} = 3\text{V}$, $I_E = 1\text{mA}$	-	0.48	5	-	0.48	2	mV
Temperature Coefficient: Base-to-Emitter Voltage Q ₁ , Q ₂ (Figure 6)	$\frac{ \Delta V_{BE} }{\Delta T}$	$V_{CE} = 3\text{V}$, $I_E = 1\text{mA}$	-	-1.9	-	-	-1.9	-	mV/°C

CA3018, CA3018A

Electrical Specifications $T_A = 25^\circ\text{C}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		CA3018			CA3018A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Base (Q ₃)-to-Emitter (Q ₄) Voltage Darlington Pair (Figure 8)	V_{BED} (V_{9-1})	$V_{CE} = 3\text{V}$	$I_E = 10\text{mA}$	-	1.46	-	-	1.46	1.60	V
			$I_E = 1\text{mA}$	-	1.32	-	1.10	1.32	1.50	V
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair (Q ₃ and Q ₄) (Figure 9)	$\frac{ \Delta V_{BED} }{\Delta T}$	$V_{CE} = 3\text{V}$, $I_E = 1\text{mA}$			-	4.4	-	-	4.4	-
Temperature Coefficient: Magnitude of Input Offset Voltage	$\frac{ V_{BE1} - V_{BE2} }{\Delta T}$	$V_{CC} = 6\text{V}$, $V_{EE} = -6\text{V}$, $I_C1 = I_C2 = 1\text{mA}$			-	10	-	-	10	-
DYNAMIC CHARACTERISTICS										
Low Frequency Noise Figure (Figures 10 - 12)	NF	$f = 1\text{kHz}$, $V_{CE} = 3\text{V}$, $I_C = 100\mu\text{A}$, Source Resistance = $1\text{k}\Omega$		-	3.25	-	-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics	h_{FE}			-	110	-	-	110	-	-
		Forward Current Transfer Ratio (Figure 13)		-	3.5	-	-	3.5	-	$\text{k}\Omega$
		Short Circuit Input Impedance (Figure 13)		-	15.6	-	-	15.6	-	μs
		Open Circuit Output Impedance (Figure 13)		-	1.8×10^{-4}	-	-	1.8×10^{-4}	-	-
		Open Circuit Reverse Voltage Transfer Ratio (Figure 13)		-	$31 - j1.5$	-	-	$31 - j1.5$	-	mS
Admittance Characteristics	Y_{FE}			-	$0.3 + j0.04$	-	-	$0.3 + j0.04$	-	mS
		Forward Transfer Admittance (Figure 14)		-	$0.001 + j0.03$	-	-	$0.001 + j0.03$	-	mS
		Input Admittance (Figure 15)		-	$See \text{ Figure } 17$					MHz
		Output Admittance (Figure 16)		-	$f = 1\text{MHz}$, $V_{CE} = 3\text{V}$, $I_C = 1\text{mA}$					pF
		Reverse Transfer Admittance (Figure 17)		-	$f = 1\text{MHz}$, $V_{CE} = 3\text{V}$, $I_C = 1\text{mA}$					pF
Gain Bandwidth Product (Figure 18)	f_T	$V_{CE} = 3\text{V}$, $I_C = 3\text{mA}$		300	500	-	300	500	-	MHz
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3\text{V}$, $I_E = 0$		-	0.6	-	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 3\text{V}$, $I_C = 0$		-	0.58	-	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	$V_{CI} = 3\text{V}$, $I_C = 0$		-	2.8	-	-	2.8	-	pF

NOTE:

3. Actual forcing current is via the emitter for this test.

Typical Performance Curves

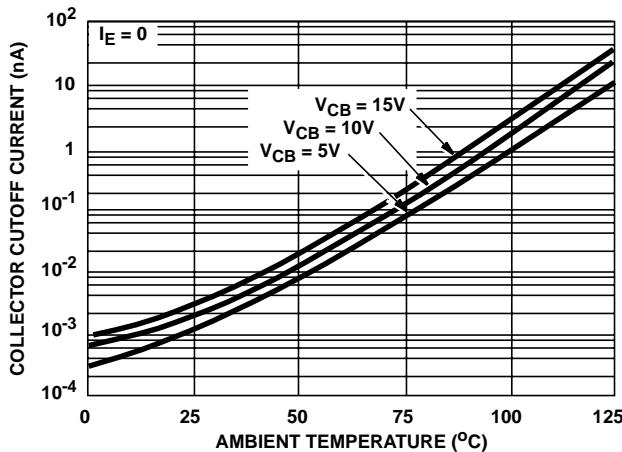


FIGURE 1. TYPICAL COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE

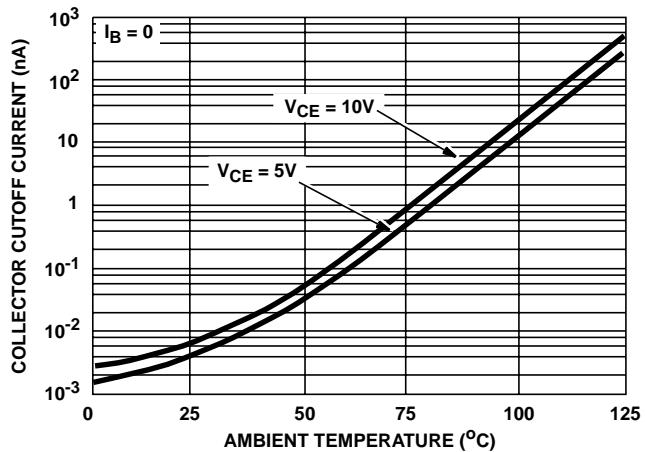


FIGURE 2. TYPICAL COLLECTOR-TO-EMITTER CUTOFF CURRENT vs TEMPERATURE

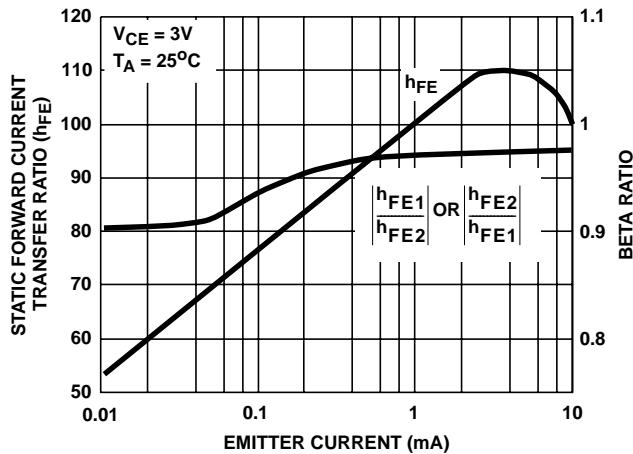


FIGURE 3. TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO AND BETA RATIO FOR TRANSISTORS Q₁ AND Q₂ vs Emitter Current

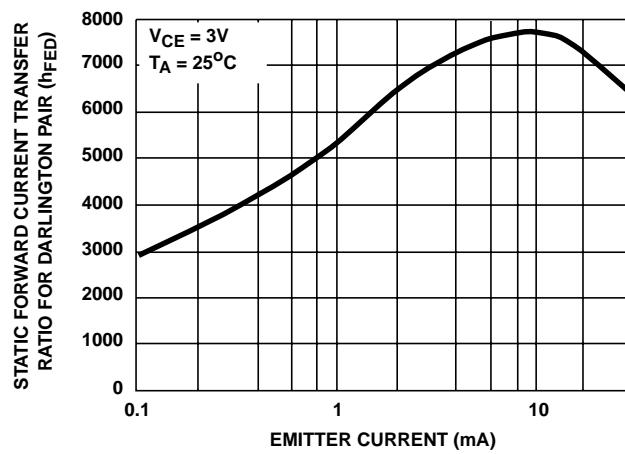


FIGURE 4. TYPICAL STATIC FORWARD CURRENT - TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q₃ AND Q₄ vs Emitter Current

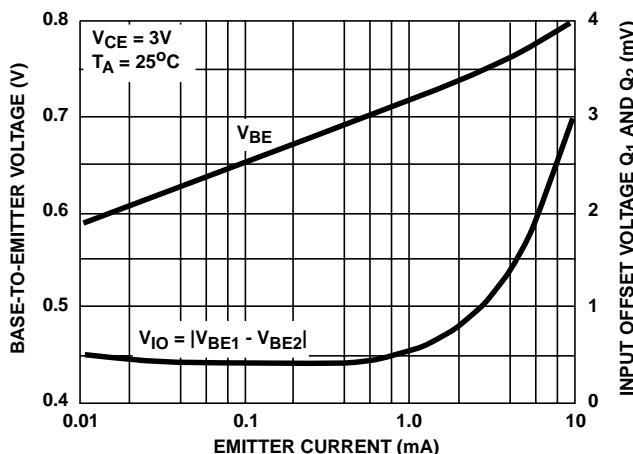


FIGURE 5. TYPICAL STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR Q₁ AND Q₂ vs Emitter Current

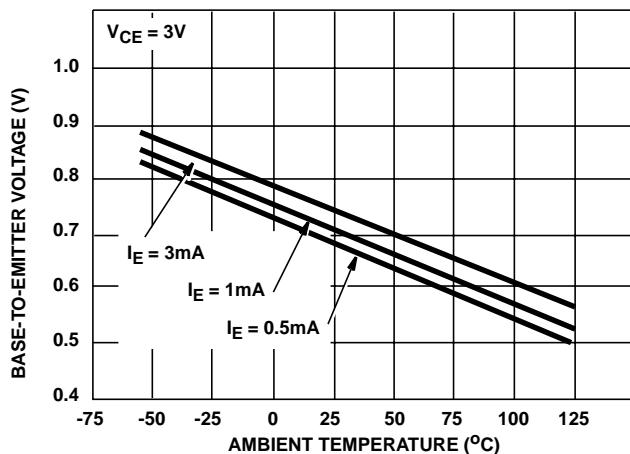
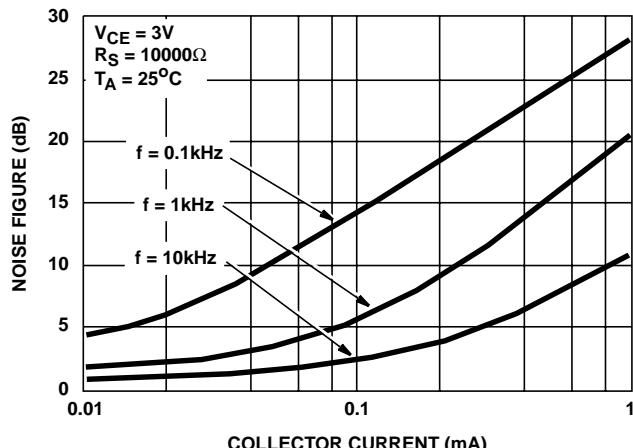
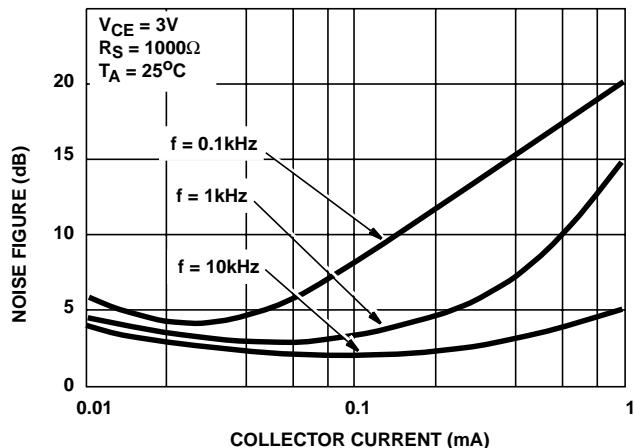
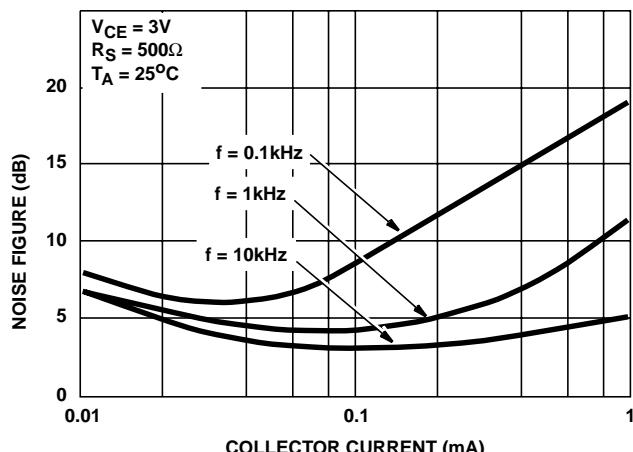
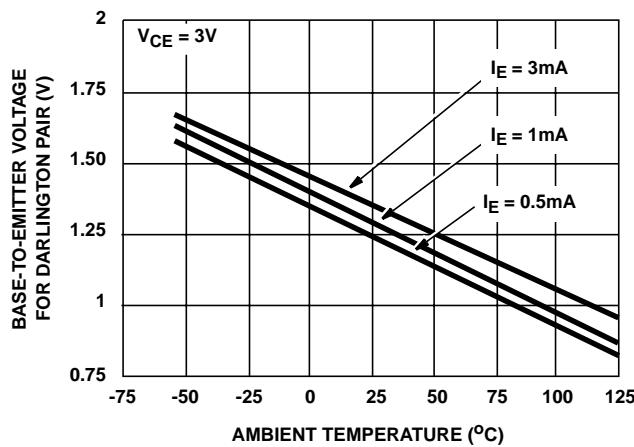
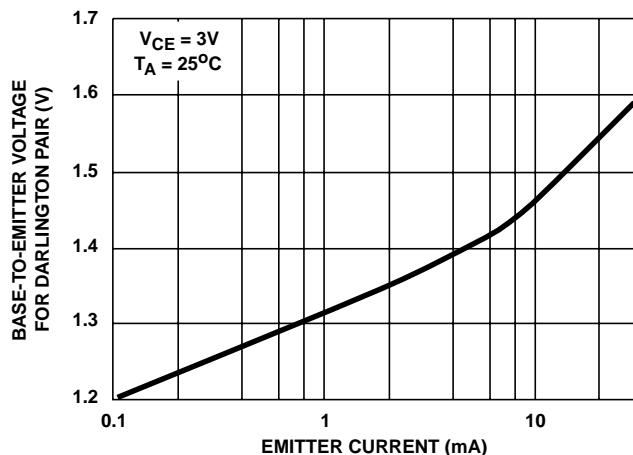
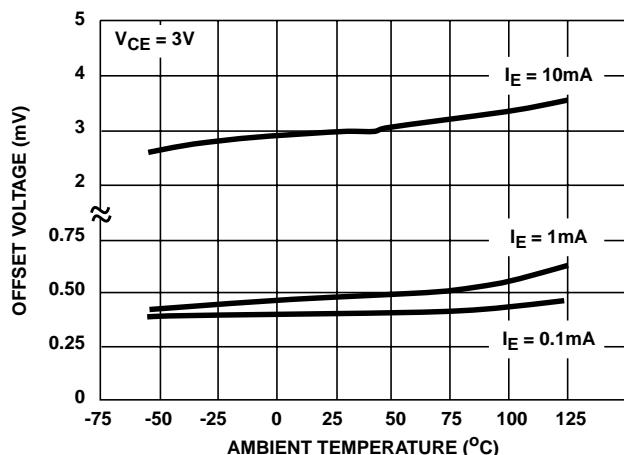


FIGURE 6. TYPICAL BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR vs TEMPERATURE

Typical Performance Curves (Continued)



Typical Performance Curves (Continued)

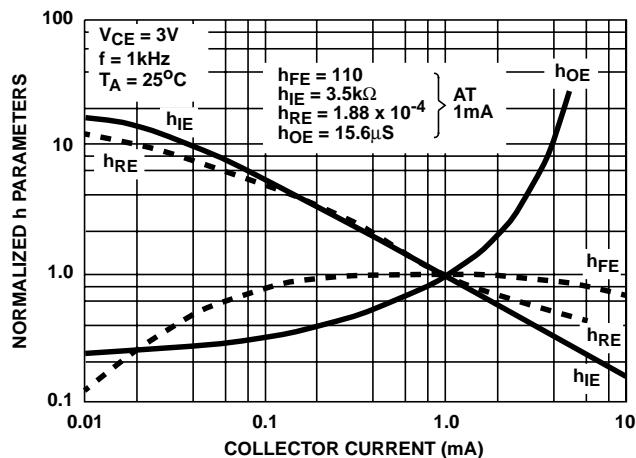


FIGURE 13. h PARAMETERS vs COLLECTOR CURRENT

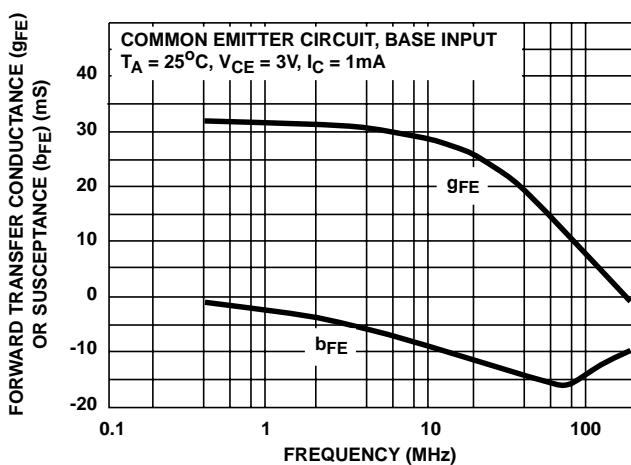


FIGURE 14. FORWARD TRANSFER ADMITTANCE (Y_{FE})

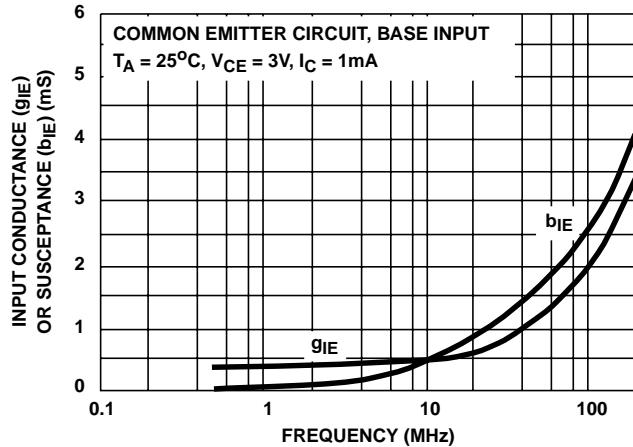


FIGURE 15. INPUT ADMITTANCE (Y_{IE})

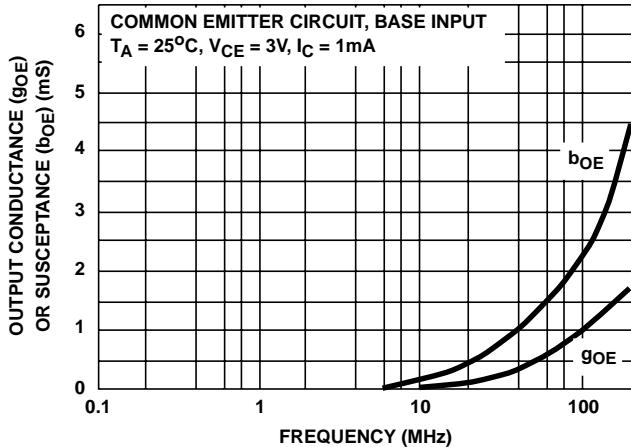


FIGURE 16. OUTPUT ADMITTANCE (Y_{OE})

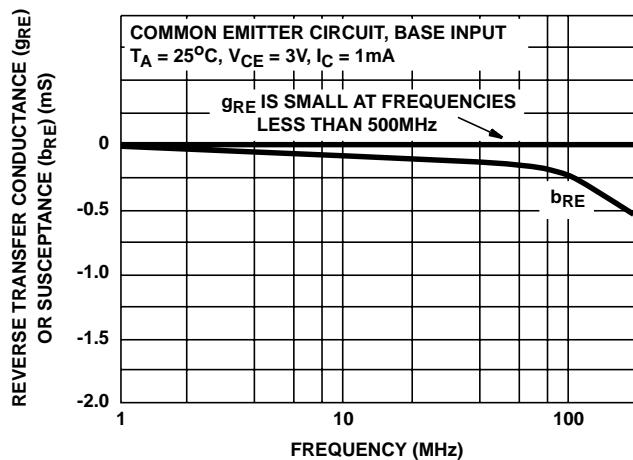


FIGURE 17. REVERSE TRANSFER ADMITTANCE (Y_{RE})

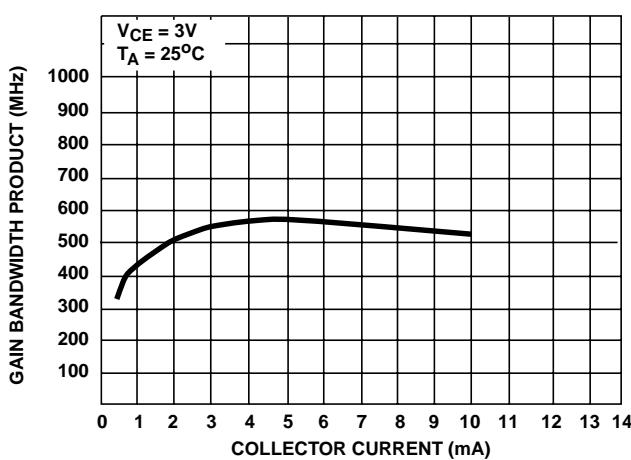


FIGURE 18. TYPICAL GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT