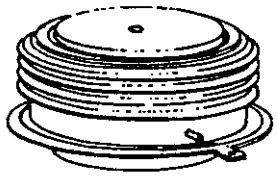
SILICON POWER

C713
53mm Inverter Thyristor
2000V / 1000A

The C713 reverse blocking thyristor is a pressure mounted, high current reverse blocking thyristor designed for power switching. It utilizes an involute interdigitated pilot gate and is manufactured by the proven multi-diffusion process.

Features:

- Off-State and Reverse Blocking Capabilities to 2000 Volts
- Very Low Switching Losses at High Frequencies
- 50 usec Maximum Turn-Off Time at Severe Operating Conditions with Feedback Diode
- Involute, Interdigitated Gate for High di/dt Capability
- Narrow Pulse Capability for PWM Inverter Commutating SCR Socket
- 1" Creepage-Path, Glazed Ceramic Package



MAXIMUM ALLOWABLE RATINGS

TYPE	V_{DRM}/V_{RRM}[1] REPETITIVE T_J = -40°C to +125°C	V_{DRM}/V_{RRM}[1] REPETITIVE T_J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE, V_{RSM}[1] T_J = -40°C to +125°C
C713L	2000 Volts	2100 Volts	2100 Volts
C713PT	1900	2000	2000
C713PN	1800	1900	1900
C713PS	1700	1800	1800
C713PM	1600	1700	1700
C713PE	1500	1600	1600

Consult factory for lower rated voltage devices.

Peak One-Cycle Surge On-State Current, I_{TSM} (8.3 msec) ..... 15,000 Amperes
(10 msec) ..... 13,500 Amperes
Maximum Rate-of-Rise of Anode Current Turn-On Interval (Switching From 1200 Volts) ..... 800 A/μsec
Repetitive di/dt Rating[2] ..... 200 A/μsec
I^2t (for fusing) (at 8.3 milliseconds) ..... 933,750 Ampere² Seconds
Peak Gate Power Dissipation, P_{GM} ..... 100 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 5 Watts
Peak Reverse Gate Voltage, V_{GRM} ..... 20 Volts
Storage and Operating Temperature, T_{STG} and T_J ..... -40°C to +125°C
Mounting Force Required ..... 5000 Lb. + 1000 – 0 Lb.
22.2 KN + 4.4 – 0 KN

NOTES:

[1] 10 msec voltage sinewave.

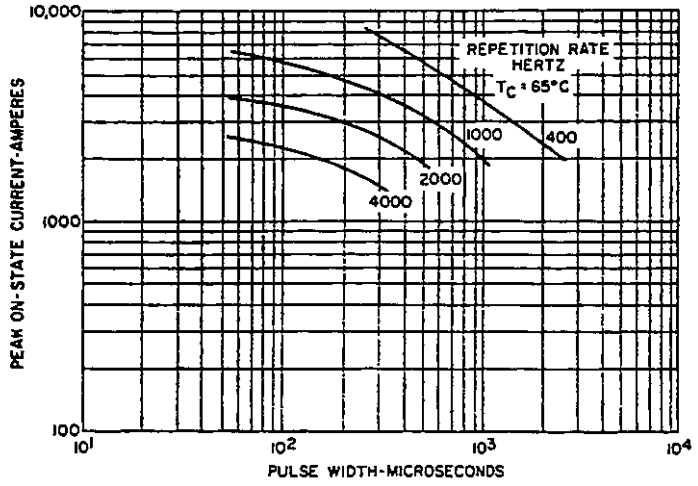
[2] di/dt rating established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2. This di/dt is in addition to the discharge of a 0.25 μf, 20 ohm snubber circuit in parallel with the DUT.

175 Great Valley Pkwy., Malvern, PA 19355, USA

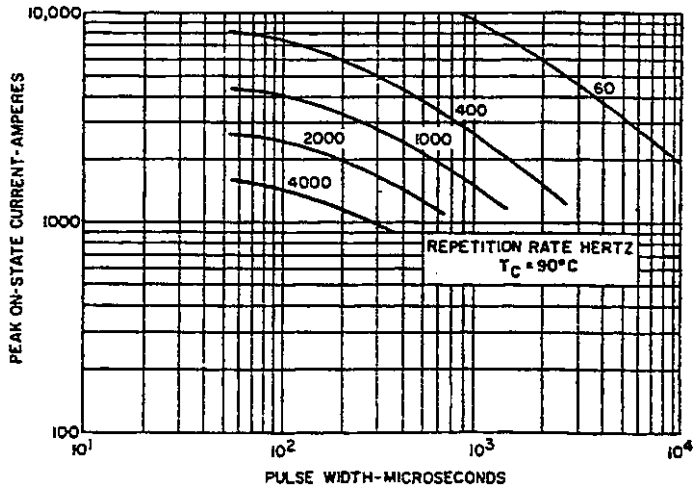
CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and On-State Blocking Current	I_{DRM} and I_{RRM}	–	20	60	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance, Junction-to-Case	$R\theta_{JC}$	–	–	.023	°C/Watt	Double-Side Cooled (DC)
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	500	–	–	V/μsec	T_J = +125°C, V_{DRM} = .80 Rated V_{RRM} Gate Open.
Delay Time	t_d	–	1.5	–	μsec	Switching from 1000 Volts, 20 Volt, 10 Ohm Gate 0.5 μsec Rise Time, T_J = 25°C
Gate Pulse Width Necessary To Trigger		10	–	–	μsec	T_J = 25°C
Gate Trigger Current	I_{GT}	–	120	200	mAdc	T_C = 25°C, V_D = 10 Vdc, R_L = 3 Ohms
		5.0	30	–		T_C = +125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Gate Trigger Voltage	V_{GT}	–	3.0	5.0	Vdc	T_C = 0°C to +125°C, V_D = 10 Vdc, R_L = 3 Ohms
Peak On-State Voltage	V_{TM}	–	–	1.7	Volts	T_C = +125°C, I_T = 1000 Amps. Peak Duty Cycle ≤ 0.01%
Conventional Circuit Commutated Turn-Off Time(1) (With Reverse Voltage)	t_q	–	45	50	μsec	(1) Tc = + 125 °C (2) It = 1000 amps (3) Vr ≥ 50 volts (4) Rate of Rise of Forward Blocking Voltage = 200V/usec to 80% Vdrm or 400V/usec to 70% of Vdrm (5) Gate Bias = Open During Turn-Off Interval 0 Volts, 100 ohms. (6) Duty Cycle ≤ 0.01%
Conventional Circuit Commutated Turn-Off Time(1) (With Feedback Diode)	t_q	–	50	55	μsec	(1) Tc = +125 °C (2) It = 1000 amps (3) Vr = 2 Volts Min. (4) Rate of Rise of Forward Blocking Voltage = 400 V/usec to 80% Vdrm (5) Gate Bias = Open During Turn-Off Interval (6) Duty Cycle ≤ 0.01%

(1) Turn-off times are measured on a go/no-go basis using LEM test equipment. Experimental determination of critical turn-off times may lead to device degradation.



1. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT T_C = 65°C FOR SINUSOIDAL CURRENT WAVEFORMS



2. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT T_C = 90°C FOR SINUSOIDAL CURRENT WAVEFORMS

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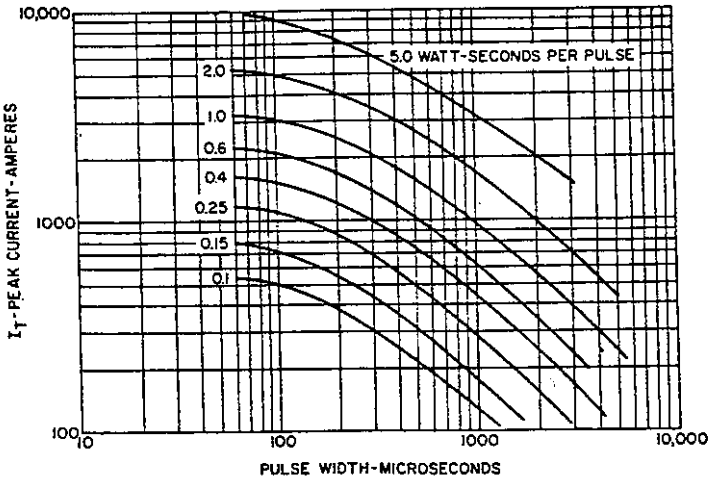
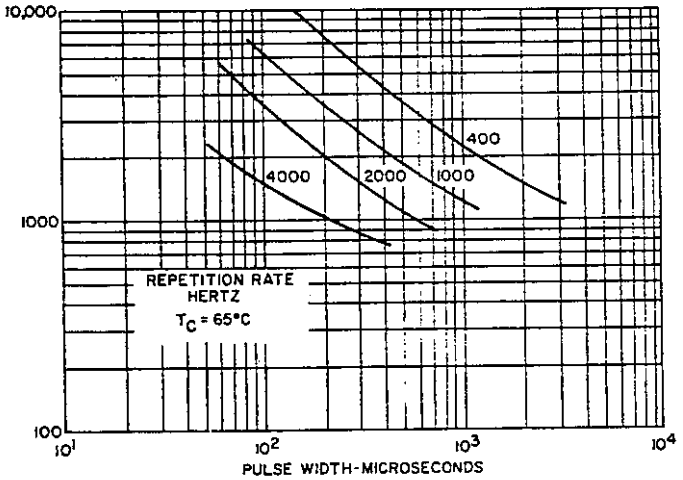


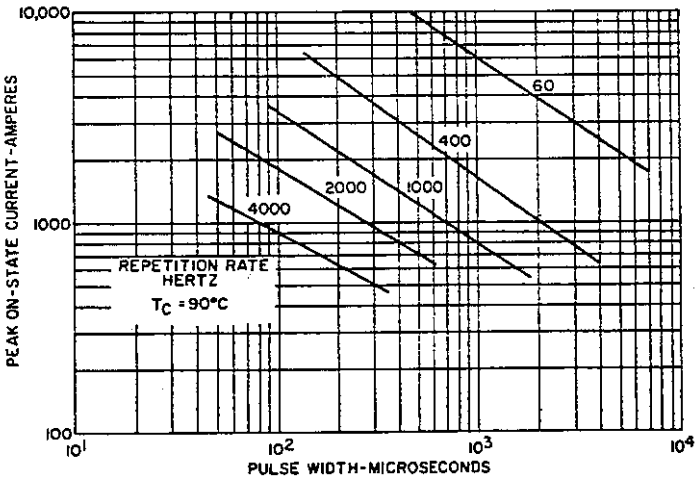
NOTES:

1. —— Switching capability and losses with bypass diode.
2. Switching voltage from 15 Volts to 0.8 V_{DRM}.
3. Snubber discharge < 50 Amps. RC time constant < 10 μsec.
4. High gate drive, 20V/10 Ohms, 0.5 μsec rise time.

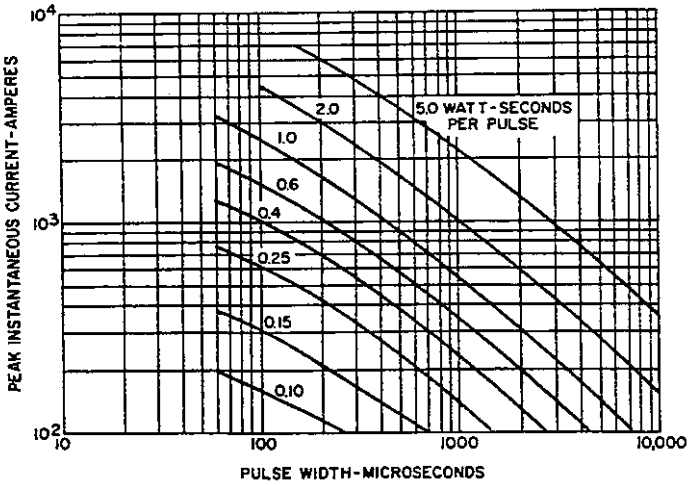
3. ENERGY PER PULSE FOR SINUSOIDAL PULSES



4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR T_C = 65°C



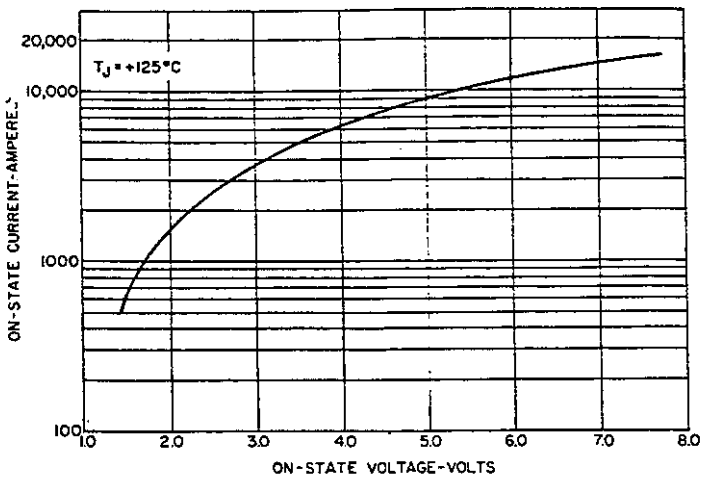
5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR T_C = 90°C



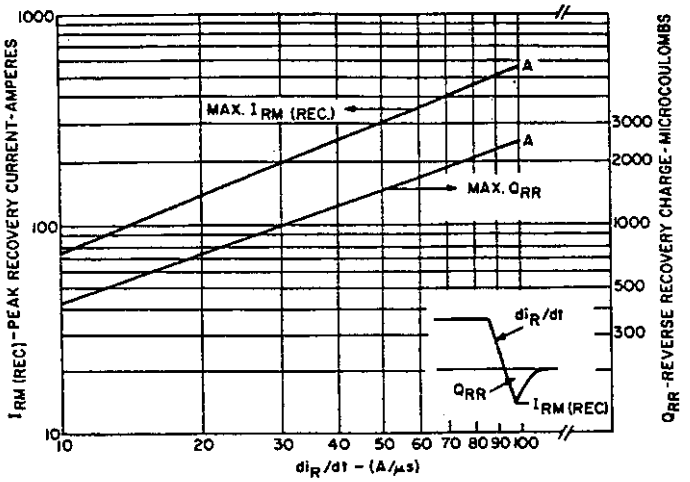
NOTES:

1. Switching voltage from 15 Volts to 0.8 V_{DRM}.
2. DI/DT during turn-on: 100A/μsec.
3. Reverse voltage < 50 Volts. If no bypass diode is used, recovery switching losses must be added.
4. RC snubber time constant < 10 μsec.
5. High gate drive: 20V/10 Ohms, 0.5 μsec rise time.

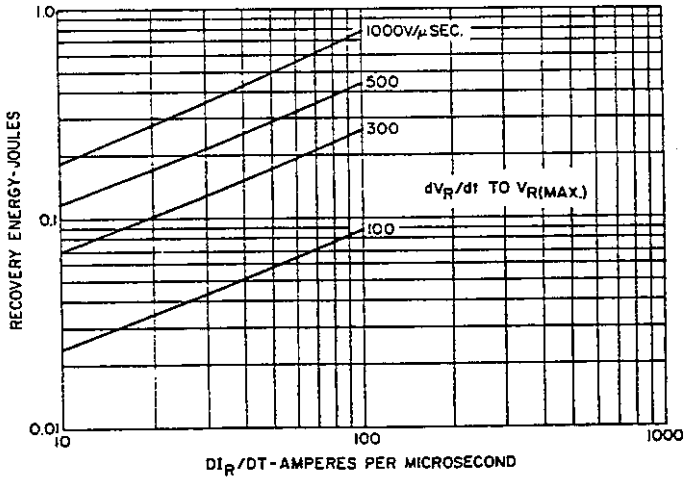
6. ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS



7. FORWARD CONDUCTION CHARACTERISTIC ON-STATE



8. RECOVERED CHARGE (125°C)



NOTES:

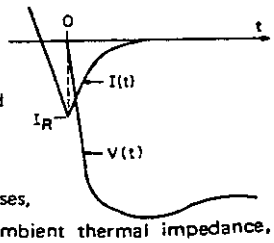
If no bypass diode is used with this thyristor, the switching losses during recovery can be significant. The actual magnitude of these losses will vary widely depending on circuit conditions and snubber design. The switching losses in a given circuit may be calculated with the following equation: $SLR = \int_0^{\infty} I(t) \cdot V(t)\ dt$

Where SLR is the recovery switching losses; I (t) is the recovery current decay; V(t) is the recovery voltage; and t = o occurs at the peak of the recovery current. I (t) may be expressed as an exponential decay:

$$I(t) = I_{Re} - (t/T)$$

Where I_R is the peak recovery current and T = 2.5μsec. The junction temperature rise due to the recovery losses may be computed as follows:

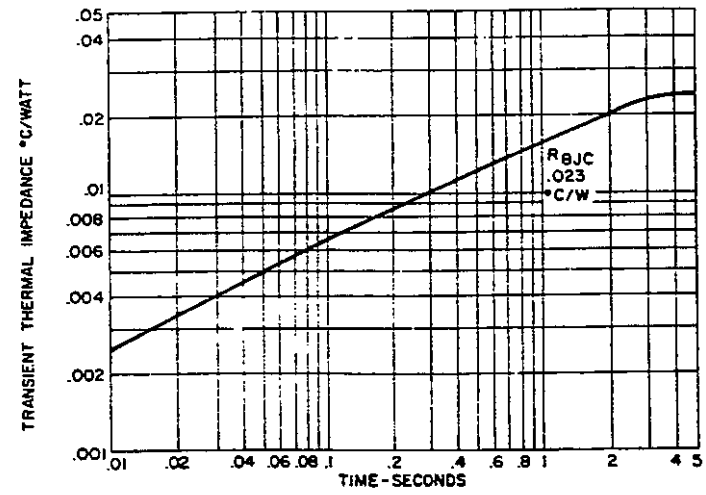
$$\Delta T_j = F * \sigma_{\mathcal{A}} * R\theta_{JA} + \alpha_{\mathcal{A}} * 3.5$$



Where $\sigma_{\mathcal{A}}$ is the recovery losses, $R\theta_{JA}$ is the DC junction to ambient thermal impedance, and F is the operating frequency.

This curve represents the maximum recovery loss as a function of circuit di/dt, and different assumed linear dv/dts.

9. RECOVERY CURRENT SWITCHING LOSSES



NOTES:

1. Add .006°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R\theta_{JS}$ = .029° C/W. See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature.

10. TRANSIENT THERMAL RESISTANCE – JUNCTION-TO-CASE

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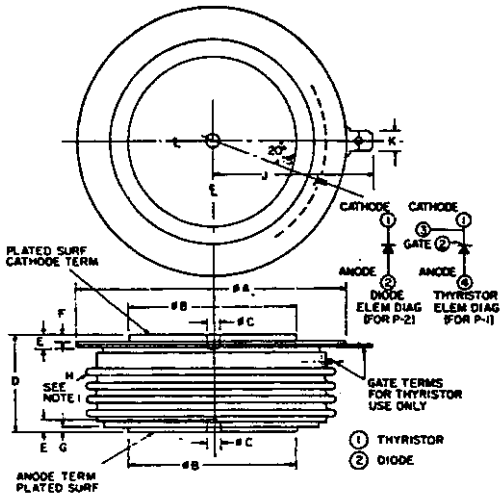
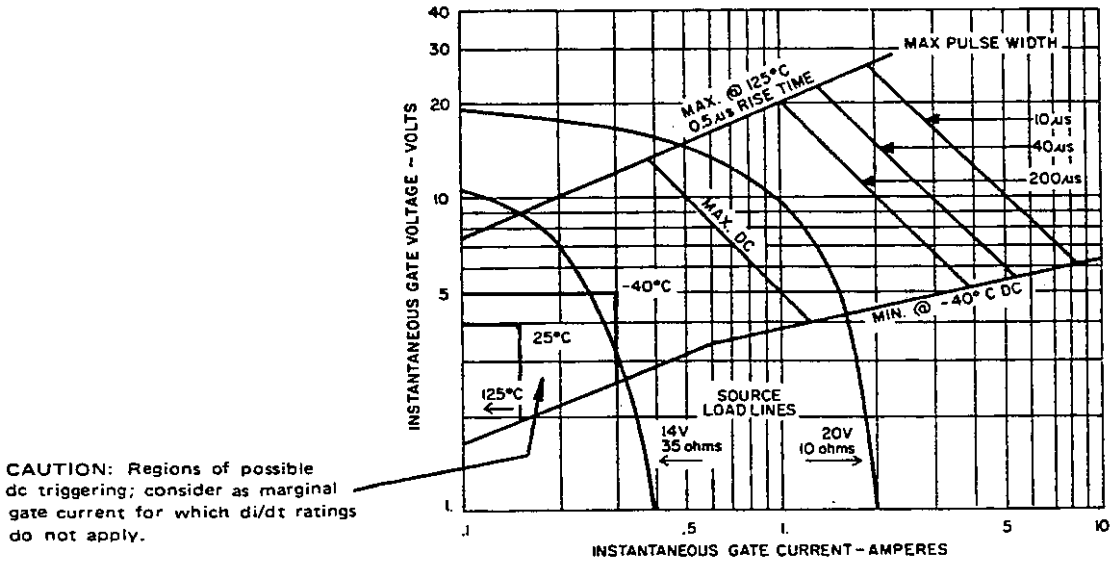
OUTLINE DRAWING



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
ϕA	–	2.960	–	75.18	
ϕB	1.800	1.900	45.72	48.26	
ϕC	0.136	0.146	3.45	3.71	
D	1.000	1.070	25.40	27.18	
E	.070	1.00	1.78	2.54	
F	.030	–	0.76	–	
G	.005	.067	0.13	1.70	
H	–	–	–	–	1
J	1.680	1.710	42.67	43.43	
K	.186	.189	4.72	4.80	

NOTES:

1. Glazed ceramic insulator with 1.00-inch (25.40mm) surface creepage, min.
2. Lead lengths are 12" (30.5cm.) with eyelet terminals to accomodate no.6 or M3 screws.



11. GATE TRIGGER CHARACTERISTICS AND POWER RATINGS

SUGGESTED MOUNTING METHODS FOR PRESS-PAKS TO HEAT DISSIPATORS

When the Press-Pak is assembled to a heat sink in accordance with the following general instructions, a reliable and low thermal resistance interface will result.

1. Check each mating surface for nicks, scratches, flatness and surface finish. The heat dissipator mating surfaces should be flat within .0005 inches and have a surface finish of 63 micro-inches.

2. It is recommended that the heat dissipator be plated with nickel or tin. Bare aluminum or copper surfaces will oxidize in time resulting in excessively high thermal resistance.

3. Sand each surface *lightly* with 600 grit paper just prior to assembly. Clean off and apply silicone oil (GE SF1154 200 centistoke viscosity) or silicone grease (GE G623 or Dow Corning DC3, 4, 340 or 640). Clean off and apply again as a *thin* film. (A thick film will adversely affect the electrical and thermal resistances.)

4. Assemble with the specified mounting force applied through a self-leveling, swivel connection. The force has to be evenly distributed over the full area. Center holes on both top and bottom of the Press-Pak are for locating purposes only.