SILICON POWER

C601
40mm Thyristor
1800V / 750A

The C601 is specifically designed for phase control applications and processed by multidiffusion, utilizing 40mm diameter silicon and a unique pilot gate. It is supplied in a disk package ready to mount using commercially available heat dissipators and mechanical clamping hardware.

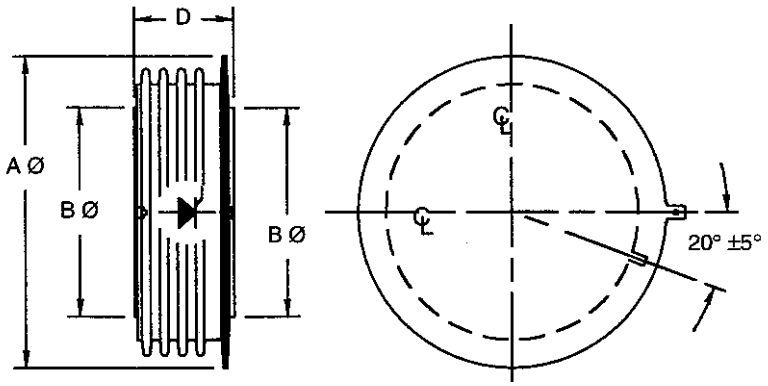
MAXIMUM ALLOWABLE RATINGS

TYPE	V_{DRM}/V_{RRM} Repetitive T_J=-40°C to 125°C	V_{DRM}/V_{RRM} Repetitive T_J=0°C + 125°C	Transient Peak Reverse Voltage (Non-Recurrent <5 Millisec.), V_{RSM}, T_J= -40°C to + 125°C
C601PA	1100Volts	1200Volts	1200Volts
C601PB	1200	1300	1300
C601PC	1300	1400	1400
C601PD	1400	1500	1500
C601PE	1500	1600	1600
C601PM	1600	1700	1700
C601PS	1700	1800	1800

Average Forward Current, On-State ..... Depends on conduction angle
Peak One-Cycle Surge ON-State Current, I_{TSM} .....11,000 Amperes
Maximum Rate of Rise ofAnode Current Turn-on Interval (see chart 11) (Switching Rates ≦ 400 H_z)
Switch From ≤ 600 V 150A/µsec
Switch From < 1000V 100A/µsec
Switch From ≥ 1300V 80A/µsec

I^2t (for fusing) (at 8.3 milliseconds) .....500,000 ampere^{2}seconds
Peak Gate Power Dissipation, P_{GM} .....40 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ ..... 5 Watts
Peak Reverse Gate Voltage, V_{GRM} ..... 5 Volts
Storage and Operating Temperature T_{STG} & T_J ..... Refer Above
Mounting Force Required ..... 4000 lbs, ± 10%

A Ø = 2.30 in (58.0 mm)
B Ø = 1.35 in (34.3 mm)
D = 1.04 in (26.4 mm)



175 Great Valley Pkwy., Malvern, PA 19355, USA

CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and Forward Blocking Current	I_{DRM} and I_{RRM}	——	10	15	mA	T_J=+25°C, V = V_{DRM} = V_{RRM}
Peak Reverse and ON-state Blocking Current	I_{DRM} and I_{RRM}	—	15	35	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance (DC), $R_{\Theta JS}$ (See Note)	DC	—	—	.041	°C/watt	Junction to Sink Double Side Cooled
	1Ø			.045		
	3Ø	—	—	.048		
	6Ø	—	—	.056		
Critical Exponential Rate of Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	500	—	—	V/usec	T_J = +125°C, V_{DRM} = .67 Rated Gate open.
Holding Current	I_H	—	100	250	mAdc	T_C = +25°C, Anode supply = 20Vdc. Initial forward current=500 amps.
Latching Current	I_L	—	—	1	Adc	T_C = +25°C, Anode voltage=24Vdc. Load resistance 12 ohms max.
Delay Time	t_d	—	4.0		usec	Switching From 140 Volts 14 Volt, 40∿Gate 2 usec Rise Time
Gate Pulse Width Necessary to Trigger		—	—	10	usec	See Figure 11
Gate Trigger Current See Fig # II	I_{GT}	—	— 80	— 150	mAdc	T_C = 25°C, V_D = 10 VDC, R_L = 3 Ohms
		5.0	15	75		T_C = +125°C, V_D = .5 x Rated R_L = 1000 Ohms
Gate Trigger Voltage See Fig #II	V_{GT}	—	2.6	4.5	Vdc	T_C = 0°C, to +125°C, V_D = 10 VDC, R_L = 3 Ohms
		.2	—	—		T_C = 125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Peak On-Voltage	V_{FM}	—	—	1.65	Volts	T_C = + 125°C, I_T = 1500 Amp Peak Duty Cycle ≦ 0.01%
Circuit Commutated Turn-Off Time	t_q	—	300	350	usec	T_C = +125°C, I_T = 450A, V_R = 75 volts min., V_{DRM} (reapplied) = ½ Rated, Rate of rise of reapplied forward blocking voltage = .25V/usec linear, Gate bias = open during turn-off interval, Duty cycle ≦ 0.01%

NOTE: T_C = Sink Temperature (measured ⅛ inch from base of SCR.)

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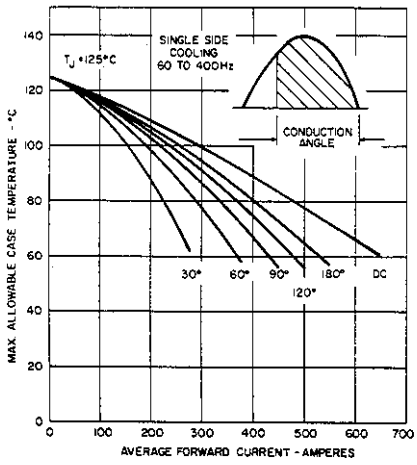
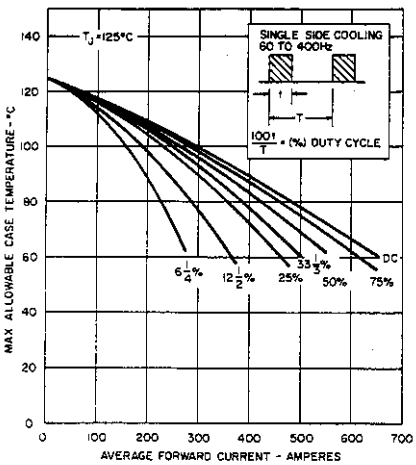
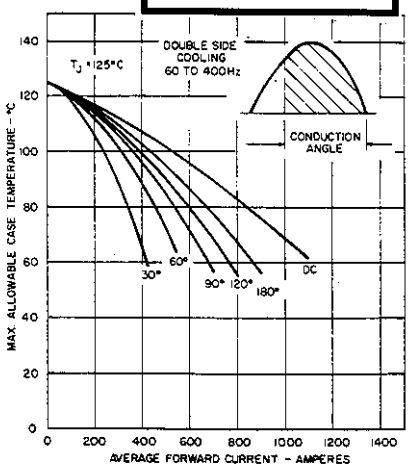


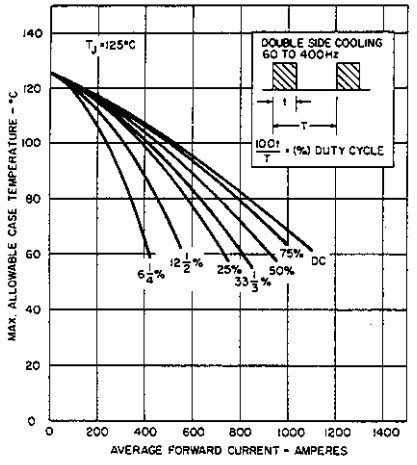
1. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM —SINGLE-SIDE COOLED



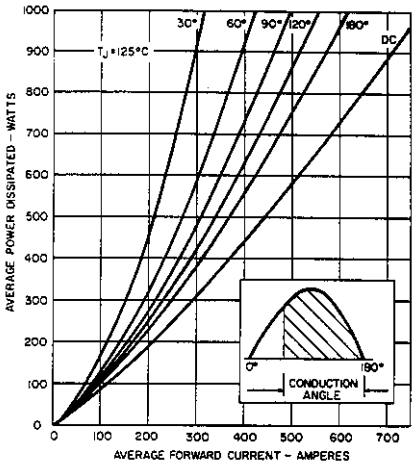
2. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM —SINGLE-SIDE COOLED



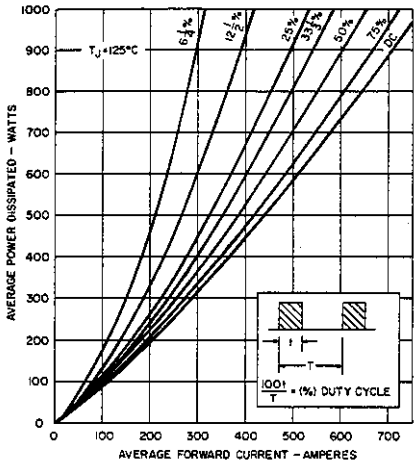
3. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM —DOUBLE-SIDE COOLED



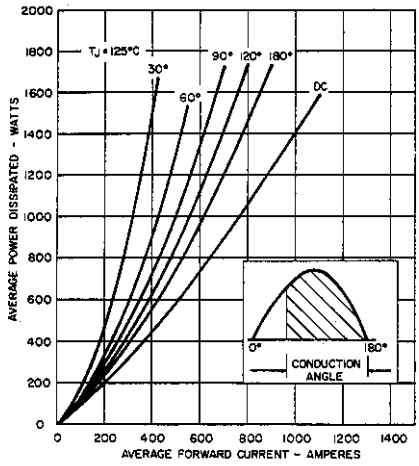
4. MAXIMUM ALLOWABLE SINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM —DOUBLE-SIDE COOLED



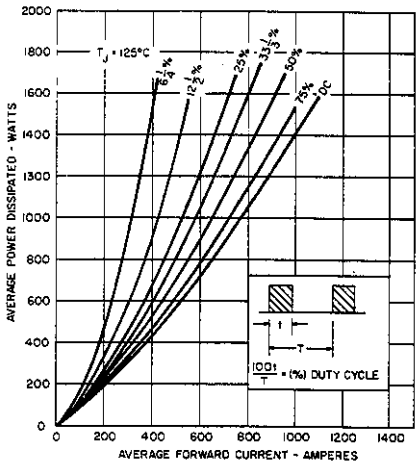
5. AVERAGE FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



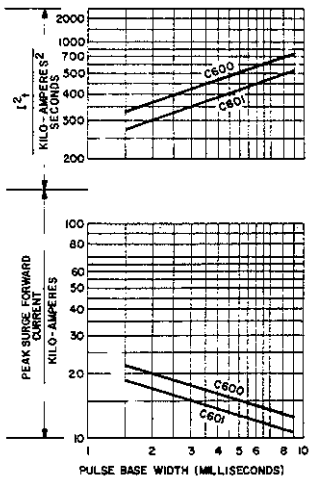
6. AVERAGE FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



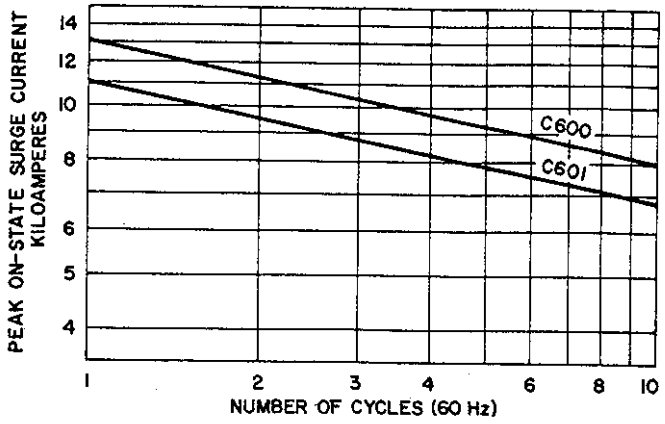
7. EXTENDED FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



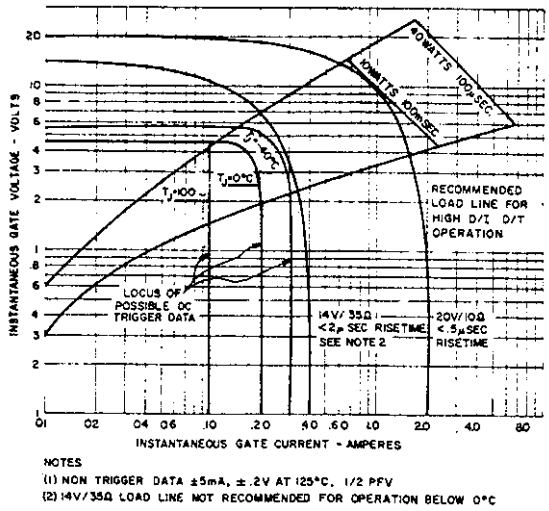
8. EXTENDED FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



9. SUB-CYCLE SURGE AND I^2t RATING FOLLOWING RATED LOAD CONDITIONS

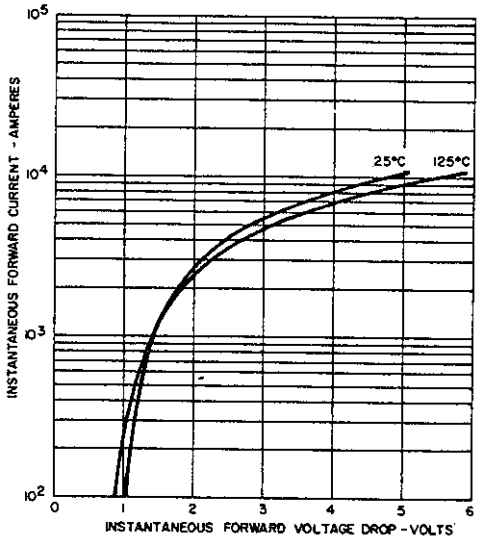


10. MAXIMUM ALLOWABLE SURGE CURRENT FOLLOWING RATED LOAD CONDITIONS



NOTES
(1) NON TRIGGER DATA ±5mA, ±.2V AT 125°C, 1/2 PFV
(2) 14V/35Ω LOAD LINE NOT RECOMMENDED FOR OPERATION BELOW 0°C

11. GATE TRIGGERING CHARACTERISTICS



12. FORWARD CONDUCTION CHARACTERISTIC, ON-STATE

THERMAL IMPEDANCE vs> POWER ON-TIME