C8750

Low EMI Clock Generator for ALi-M1541 Chipset with AGP Support.

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Product Features

- Supports K6-II, Pentium® and M2 CPU's.
- Supports Mobile **Pentium® II designs.**
- Designed to meet AliM1541 and Intel high speed chipset
- 3 CPU clocks with isolated power supply
- 6 PCI clocks
- 13 SDRAM clocks for 3 DIMM support with feedback.
- One 48 MHz USB clock
- < 175 pS Max. skew among CPU clocks.
- < 250 pS Max. skew among PCI clocks.
- I^2C control interface for programmability
- Allows Jumperless Frequency Selection
- Independent clock disable
- Spread Spectrum bandwidth selection
- 48-pin SSOP package
- Spread Spectrum for EMI reduction
- Supports power management function

Block Diagram

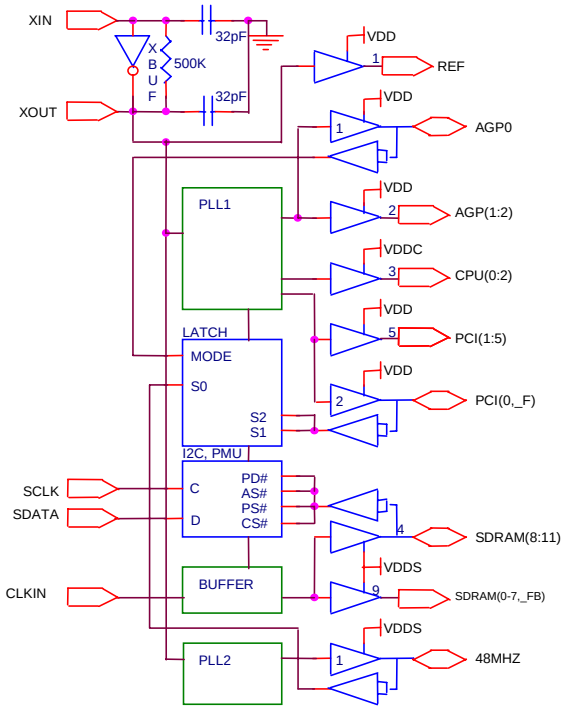


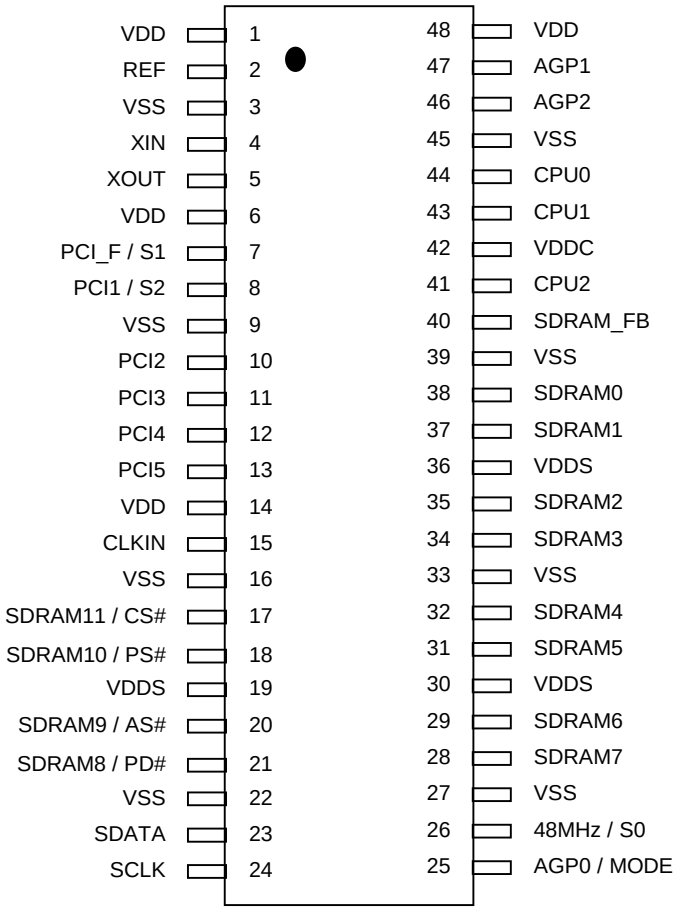
Fig.1

Frequency Table

S2	S1	S0	CPU	AGP	PCI
0	0	0	60	60	30
0	0	1	66.8	66.8	33.4
0	1	0	95.25	63.5	31.75
0	1	1	75	75	37.5
1	0	0	75	50	25
1	0	1	83.3	55.53	27.77
1	1	0	90	60	30
1	1	1	100.2	66.6	33.3

Table 1

Pin Configuration



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Pin Description

PIN No.	Pin Name	PWR	I/O	TYPE	Description
2	**REF**	VDD	O		A buffer output clock of the reference signal at Xin.
4	**Xin**	VDD	I	OSC1	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
5	**Xout**	VDD	O	OSC1	On-chip reference oscillator output pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected.
7	**S1**		I		This is a bidirectional pin (see app. note,p.4). At power up, it is an input select pin, S1 (table 1,p.1). When the power reaches the rail, the selection is latched into the control registers, and this pin becomes
	PCI_F		O		a PCI clock output. This clock does **not stop** when PS# is asserted low.
8	**S2**		I		This is a bidirectional pin (see app. note,p.4). At power up, it is an input select pin, S2 (table 1,p.1). When the power reaches the rail, the selection is latched into the control registers and this pin becomes
	PCI1		O		a PCI1 clock output.
10, 11,12, 13	**PCI(2:5)**	VDD	O		PCI clock outputs. They are Synchronous to the CPU clocks.
15	**CLKin**	VDD	I	-	Input buffer pin of SDRAM distribution clocks.
17,18,20,21	**CS#, PS#, AS#, PD#**	-	I		This is a bidirectional pin. The direction of these pins is controlled by Mode, pin25. When Mode =0, then these pins are input CS#,PS#,AS#, and PD# for power management (See power management function description, p.3)
	SDRAM(8:11)	VDD	O		When Mode = 1, these pins are SDRAM(8:11)buffered outputs of CLKin.
23	**SDATA**	VDD	I/O	PU	Serial data input pin. Conforms to the Philips I2C specification of a Slave Receiver device. This pin is an input when receiving data. It is an open drain output when acknowledging. See I2C function description,p.5.
24	**SCLK**	VDD	I	PU	Serial clock input pin. Conforms to the Philips I2C 100KHz Specification.
	Mode				This is a bidirectional pin (see app. note,p.4). At power up, it is an input select pin Mode. Mode sets the direction of pins 17,18,20, and 21. If Mode = 0, then pins 17,18,20,21 are power management inputs. If Mode = 1 (default), then pins 17,18,20,21 are SDRAM(8:11) outputs. When the power reaches the rail, the selection of is latched internally and this pin becomes
25	**AGP0**	VDD	O		an AGP0 clock output AGP clocks are synchronous to CPU clocks (see table1, p.1)
26	**S0**		I		This is a bidirectional pin (see app. note,p.4). At power up, it is an input select pin, S0 (table 1,p.1). When the power reaches the rail, the selection is latched into the control registers, and this pin becomes
	48M	VDD	O		a 48MHz USB clock output
28,29,31,32, 34, 35, 37, 38, 40	**SDRAM(0:7) SDRAM_FB**	VDD	O		These pins are SDRAM clock outputs. They are buffered outputs of the signal applied at CLKin (pin15).
41, 43, 44	**CPU(0:2)**	VDDC	O		Host (CPU) Clock outputs. See Table 1,p.1 for frequency selection.
47,48	**AGP(1:2)**	VDD	O		AGP clock outputs. They are synchronous to CPU clocks. (see table1,p.1)
1,6,14,48	**VDD**	-	P	-	3.3 Volt common power supply pins.
19,30,36	**VDDS**	-	P	-	3.3 Volt power supply pins for SDRAM(_FB,0:11) outputs.
42	**VDDC**	-	P	-	3.3 or 2.5 Volt power supply pins for the CPU(0:2) outputs.
3,9,16,22,27, 33, 39, 45	**VSS**	-	P	-	Common Ground pins.

Table 2

A bypass capacitor (0.1 uF) should be placed as close as possible to each Vdd, Vddc, and Vdds pins. If these bypass capacitors are not close to the pins, their high frequency filtering characteristic will be canceled by the lead inductance of the traces.

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Power Management Functions

When MODE = 0, the power management function is enabled and pins 17,18,20 and 21 are inputs CS# (CPU_STOP#) , PS# (PCI_STOP#), AS# (AGP_STOP#) and PD# (PWR_DWN#) respectively. (When MODE=1, these functions are not available, see Note 1 below).

A particular output is enabled only when both the serial interface (I2C) and these pins indicate that it should be enabled. The clocks may be disabled according to the following table in order to reduce power consumption. All clocks are stopped in the low state, see fig.2. All clocks maintain a valid high period on transitions from running to stopped. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge of their own clock.

CS#	PS#	AS#	PD#	CPU(0:2)	PCI(1:5)	AGP(0:2)	OTHER CLKs	XTAL & VCOs
x	x	x	0	LOW	LOW	LOW	LOW	OFF
0	0	0	1	LOW	LOW	LOW	RUNNING	RUNNING
0	0	1	1	LOW	LOW	RUNNING	RUNNING	RUNNING
0	1	0	1	LOW	RUNNING	LOW	RUNNING	RUNNING
0	1	1	1	LOW	RUNNING	RUNNING	RUNNING	RUNNING
1	0	0	1	RUNNING	LOW	LOW	RUNNING	RUNNING
1	0	1	1	RUNNING	LOW	RUNNING	RUNNING	RUNNING
1	1	0	1	RUNNING	RUNNING	LOW	RUNNING	RUNNING
1	1	1	1	RUNNING	RUNNING	RUNNING	RUNNING	RUNNING

Table 3

NOTE1: all clocks can be individually enabled / stopped via the I2C interface. In this case all clocks are stopped asynchronously in the low state.

Power Management Timing Table

Signal	Signal State	Latency
CS#	1 (disabled)	1 rising edge of CPU_F
	0 (enabled)	1 rising edge of CPU_F
PS#	1 (disabled)	1 rising edge of PCI_F
	0 (enabled)	1 rising edge of PCI_F
AS#	1 (disabled)	1 rising edge of AGP_F
	0 (enabled)	1 rising edge of AGP_F
PD#	1 (disabled)	2 mS
	0 (enabled)	1 rising edge of PCI_F

Table 4

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Power Management Timing

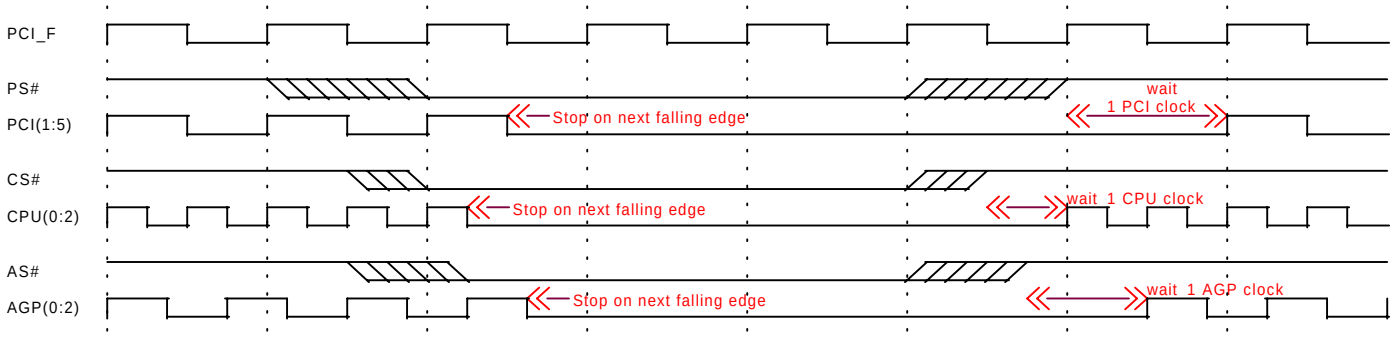

Fig. 2

Power on Bi-Directional Pins

Power Up Condition:

Pins 7, 8, 25, and 26 are Power up bi-directional pins and are used for selecting different functions in this device (see Pin description, Page 2). During power-up of the device, these pins are in input mode (see Fig 3, below), therefore, they are considered input select pins internal to the IC. After a settling time, the Selection data is latch into internal control registers and these pins become toggling clock outputs.

NOTE: This section does not apply to pins 17,18,20 and 21. The direction of these pins is controlled by Mode (pin25).

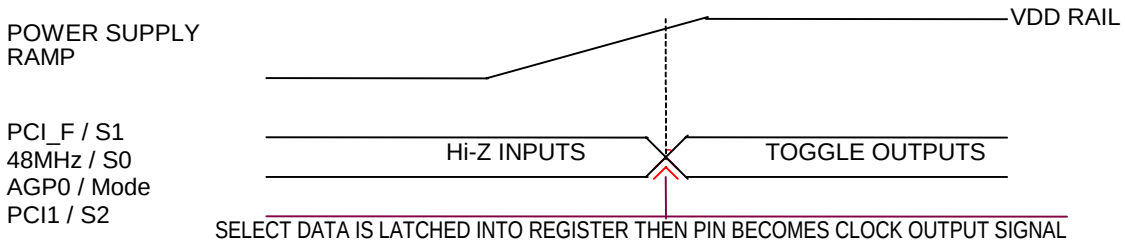

Fig.3

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Strapping Resistor Options

The power up bi-directional pins have a large value pull-up each (250KΩ), therefore, a selection "1" is the default. If the system uses a slow power supply (over 5mS settling time), then **it is recommended** to use an external Pullup (Rup) in order to insure a high selection. In this case, the designer may choose one of two configurations, see Fig.4A and Fig. 4B.

Fig4A represents an additional pull up resistor 50KΩ connected from the pin to the power line, which allows a faster pull to a high level.
If a selection "0" is desired, then a jumper is placed on JP1 to a 5KΩ resistor as implemented as shown in Fig.4A. Please note the selection resistors (Rup, and Rdn) are placed before the Damping resistor (Rd) close to the pin.

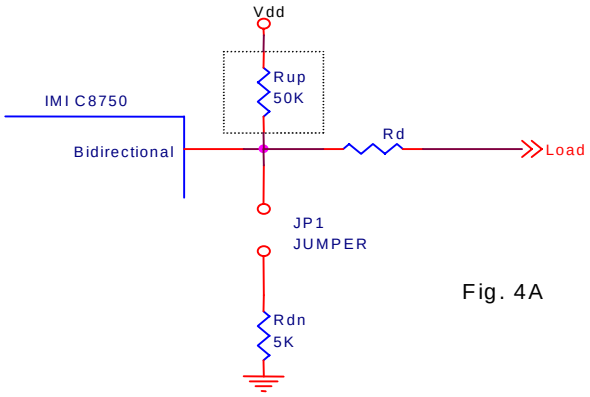

Fig. 4A

Fig4B represent a single resistor 10KΩ connected to a 3 way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

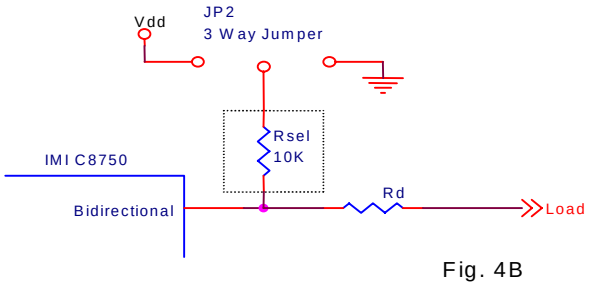

Fig. 4B

2-Wire I²C Control Interface

The 2-wire control interface implements a write slave only interface according to Philips I2C specification. (see fig5, page6) . The device can be read back by using standard I²C command bytes. Sub-addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 0 in write mode.

The device will respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions, and previously set control registers are retained.

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Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up.

Following the acknowledge of the Address Byte , two additional bytes must be sent:

1) "**Command Code** " byte, and
2) "**Byte Count**" byte.

Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the below described sequence (Byte 0, Byte 1, Byte2,) will be valid and acknowledged.

Byte 0: Frequency, Function Select Register

Bit	@Pup	Pin#	Description, See Page 7 for SSCG description.			
7	0	n/a	when MBS, Bit2 = **0**		when MBS, Bit2 = **1**	
			0 = +/-0.3% 1 = +/-0.15% For 60M – 83.3M	0 = +/-0. 25% 1 = +/-0.125% For 90M – 100.2M	0 = +/- 0.9 % 1 = +/-0.5% For 66.8M – 83.3M	0 = +/-0.5% 1 = +/-0.375% For 90M – 100.2M
6	0	n/a	S2 (for frequency table selection by software via I2C), selection valid if bit3 = 1			
5	0	n/a	S1 (for frequency table selection by software via I2C), selection valid if bit3 = 1			
4	0	n/a	S0 (for frequency table selection by software via I2C), selection valid if bit3 = 1			
3	0	n/a	0 = frequency selected by hardware, pins 25,26,46		1 = frequency selection via I^2C byte0.(bits4,5,6)	
2	0	n/a	MBS (Modulation Bandwidth Selector)			
1	0	n/a	0 = Spread Spectrum disabled		1 = Spread spectrum enabled	
0	0	n/a	0 = Running		1 = Test mode.	

Test Mode Table (enabled via I^2C Byte 0, Bit 0 = 1)

Signal	CPU(0:2)	PCI(_F,1:5)	AGP(0:2)	REF	48MHz
Operating mode					
Test mode, bit5=1	= XIN /2	= XIN /4	= XIN /3	= XIN	=XIN /4
Normal mode, bit5=0	see table 1	see table 1	see table 1	14.318M	48MHz

Table 5

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Serial Control Registers (Cont.)

Byte 1: CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	26	48 Mhz enable/Stopped
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	41	CPU2 enable/Stopped
1	1	43	CPU1 enable/Stopped
0	1	44	CPU0 enable/Stopped

Byte 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	7	PCI_F enable/Stopped
5	1	-	Reserved
4	1	13	PCI5 enable/Stopped
3	1	12	PCI4 enable/Stopped
2	1	11	PCI3 enable/Stopped
1	1	10	PCI2 enable/Stopped
0	1	8	PCI1 enable/Stopped

Byte 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	28	SDRAM7 enable/Stopped
6	1	29	SDRAM6 enable/Stopped
5	1	31	SDRAM5 enable/Stopped
4	1	32	SDRAM4 enable/Stopped
3	1	34	SDRAM3 enable/Stopped
2	1	35	SDRAM2 enable/Stopped
1	1	37	SDRAM1 enable/Stopped
0	1	38	SDRAM0 enable/Stopped

Byte 4: Additional SDRAM Clock Register (1=enable,0=Stopped)

Bit	@Pup	Pin#	Description
7	1	25	AGP0 enable/Stopped
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	17	SDRAM11 enable/Stopped
2	1	18	SDRAM10 enable/Stopped
1	1	20	SDRAM9 enable/Stopped
0	1	21	SDRAM8 enable/Stopped

Byte 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	47	AGP1 enable/Stopped
3	1	-	Reserved
2	1	-	Reserved
1	1	46	AGP2 enable/Stopped
0	1	2	REF enable/Stopped

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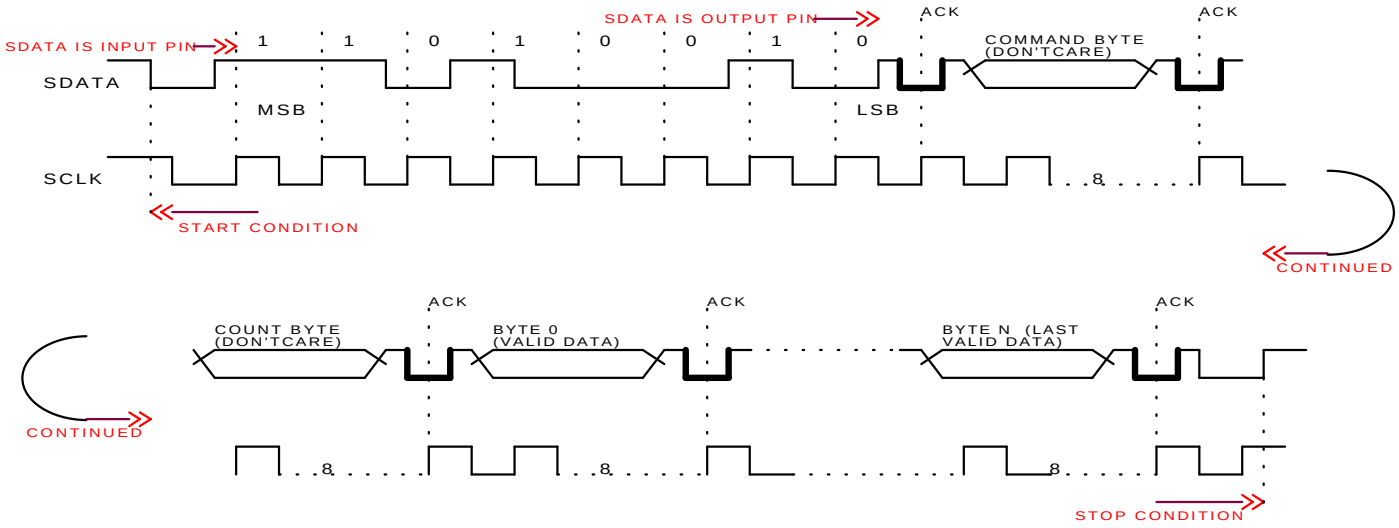

Fig.5

Spectrum Spread Clocking

Spread Spectrum is a modulation technique for reducing Electro Magnetic radiation (EMI) at the source, which in this case is the clock. The concept is based on redistributing the energy of a frequency over a finite bandwidth (also referred to as spread percentage), therefore reducing the measured emission. Fig5 represents an actual measurement on a spectrum analyzer showing the EMI reduction as a result of Spread Spectrum.

Center Spread is when the modulation does not effect the center frequency and the energy is redistributed equally on both sides of the center, which remains the same as the center frequency in the non-spread mode. Therefore, in Center spread, Fcs = Fcr.

For example; if the rested (non-spread) center frequency is 100.2 MHz, it will remain the same when spread spectrum is enabled but the modulation will vary from a max frequency to a min frequency depending of the Spread option selected by I2C byte0, bit7 and bit2 (MSB).

If a selection of +/-0.5% (bit7 = 0, bit2 (MSB) = 1),
then the max frequency would be Fmax = 100.2 + (100.2 x 0.5%) = 100.7MHz
and the min frequency would be Fmin = 100.2 - (100.2 x 0.5%) = 99.7MHz
But the center frequency will remain Fcs = (100.7 + 99.7) / 2 = 100.2MHz.

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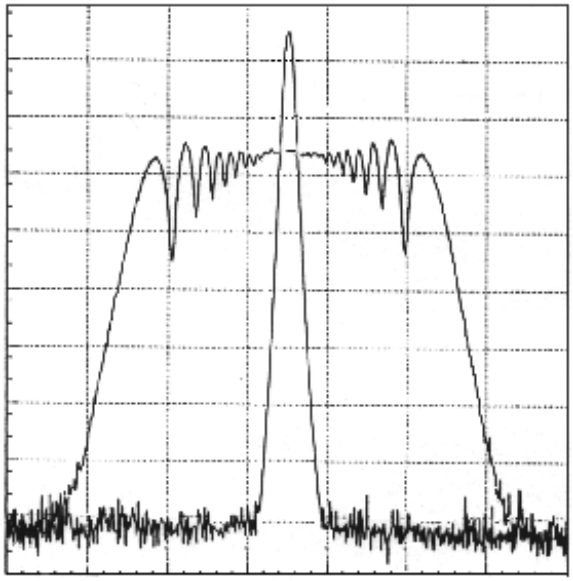

Fig.6

Spread Spectrum Selection Tables

Byte0, Bit2	Byte0, Bit7	Spread %
Applicable to 60, 66.8M, 75M, 83.3M		
0	0	+/- 0.3 %
0	1	+/-0.15 %
1	0	+/- 0.9 %
1	1	+/- 0.5 %
Byte0, Bit2	Byte0, Bit7	Spread %
Applicable to 90M, 95.25M, 100.2M		
0	0	+/- 0.25 %
0	1	+/- 0.125 %
1	0	+/- 0.5 %
1	1	+/- 0.375 %

Table 6.

Maximum Ratings

Input Voltage Relative to VSS:	VSS - 0.3V
Input Voltage Relative to VDD:	VDD + 0.3V
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to 70ºC
Maximum Power Supply:	7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	CLKin, PS#, CS#, AS#, PD#
Input High Voltage	VIH1	2.0	-	-	Vdc	CLKin, PS#, CS#, AS#, PD#
Input Low Voltage	VIL2	-	-	1.0	Vdc	SDATA, SCLK
Input High Voltage	VIH2	2.4	-	-	Vdc	SDATA, SCLK
Input Low Voltage	VIL3	-	-	1.1	Vdc	XIN
Input High Voltage	VIH3	2.0	-	-	Vdc	XIN
Input Low Current (@VIL = VSS)	IIL	-66	-	-5	µA	Pull up
Input High Current (@VIL = VDD)	IIH	-	-	5	µA	Pull up
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	IDD	-	-	250	mA	Note 1
Static Supply Current	Isdd	-	-	4	mA	PD# = 0. Crystal running at 14.318M
VDD = VDDS = VDDC = 3.3V ±5***%, TA = 0ºC to +70ºC***						

Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V for 3.3V signals
CLKin to SDRAM(0:11,_FB)	tPD	1	3	5	nS	see Note 3
Offset (CPU-PCI)	tOFF	1	-	4	nS	see Note 3
Skew (CPU-CPU), (SDRAM-SDRAM), (PCI-PCI), (AGP-AGP), (AGP-PCI))	tSKEW1	-	-	250	pS	see Note 3
Long Term Jitter	LTJ	-	-	500	pS	see Note 4
VDD = VDDS = VDDC = 3.3V ±5***%, TA = 0ºC to +70ºC***						

Note 1: Measures total current consumption through all vdd pins. All outputs loaded as per table7 below
Note 3: All outputs loaded as per table 7 below. Probes are placed on the pins and taken at 1.5V levels.
Note 4: This measurement is applicable with Spread Spectrum ON or OFF at the CPU clock outputs.

Output Name	Max Load (in pF)
CPU(0,2), AGP(02), REF, SDRAM_FB	20
PCI(_F,1:5), SDRAM(0:11)	30
48 MHz	15

Table 7.

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Buffer Characteristics

CPU(0:2)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-13	-	-	mA	Vout =VDDC - 0.5V
Pull-Up Current	IOH_2	-22	-	-	mA	Vout = 1. 25 V
Pull-Down Current	IOL_1	18	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	50	-	-	mA	Vout = 1.2 V
Rise/Fall Time, @ 0.4V-2.0V	Tr, Tf	0.4	-	2	nS	See table 7 page 8
VDD = VDDS = 3.3V ±5***% VDDC = 2.5V***±5%,***TA = 0ºC to +70ºC***						

REF, AGP(0:2) and PCI(1:5, _F)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-18	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-44	-	-	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	18	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	50	-	-	mA	Vout = 1.5 V
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	2	nS	See table 7 page 8
VDD = VDDS = 3.3V ±5***% VDDC = 2.5V***±5%,***TA = 0ºC to +70ºC***						

48 MHz

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-13	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-30	-	-	mA	Vout = 1.5 V
Pull-Down Current	IOL_1	13	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	32	-	-	mA	Vout = 1.5 V
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	3	nS	See table 7 page 8
VDD = VDDS = 3.3V ±5***% VDDC = 2.5V***±5%,***TA = 0ºC to +70ºC***						

SDRAM(0:13)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-22	-	-	mA	Vout =VDD - 0.5V
Pull-Up Current	IOH_2	-54	-	-	mA	Vout = 1.5 V
Pull-Down Current	IOL_1	20	-	-	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	54	-	-	mA	Vout = 1.5 V
Rise/Fall Time, @ 0.4V-2.4V	Tr, Tf	0.4	-	1.6	nS	See table 7 page 8
VDD = VDDS = 3.3V ±5***% VDDC = 2.5V***±5%,***TA = 0ºC to +70ºC***						

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Crystal and Reference Oscillator Parameters

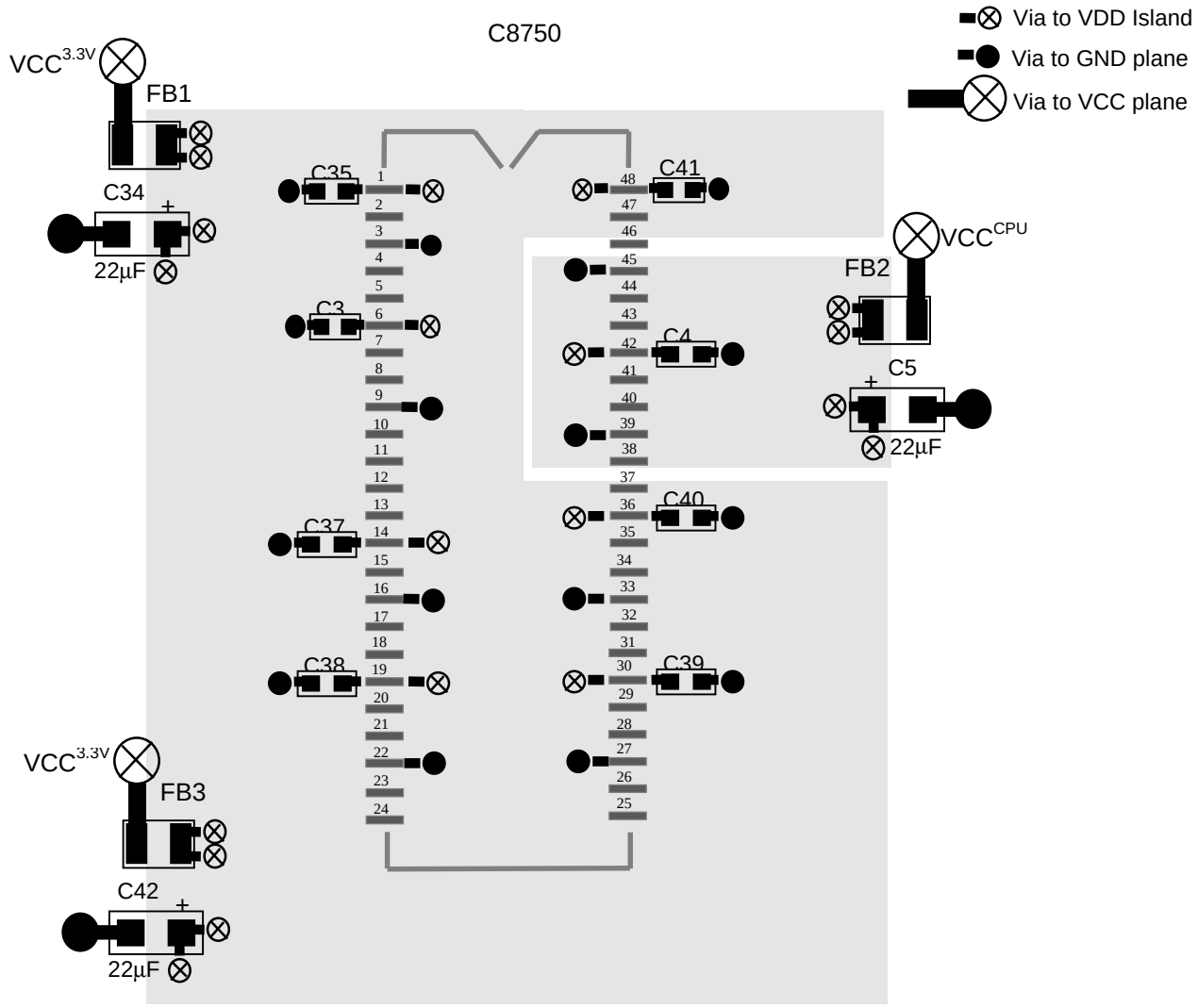
Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	TC	-	-	+/-100	PPM	Calibration note 1
	TS	-	-	+/- 100	PPM	Stability (Ta -10 to +60C) Note 1
	TA	-	-	5	PPM	Aging (first year @ 25C) Note 1
Mode	OM	-	-	-		Parallel Resonant
Pin Capacitance	CP		36		pF	Capacitance of XIN and Xout pins to ground (each)
DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Startup time	Ts	-	-	30	µS	
Load Capacitance	CL	-	20	-	pF	The crystal's rated load. Note 1
Effective Series resistance (ESR)	R1	-	-	40	Ohms	
Power Dissipation	DL	-	-	0.10	mW	note 1
Shunt Capacitance	CO	-	--	8	pF	Crystal's internal package capacitance (total)

For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors.
Budgeting Calculations
Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore = 2.0 pF
Clock generator internal pin capacitance of 32 pF, Load to the crystal is therefore = 18.0 pF
The total parasitic capacitance would therefore be = 20.0 pF.

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

Approved Product

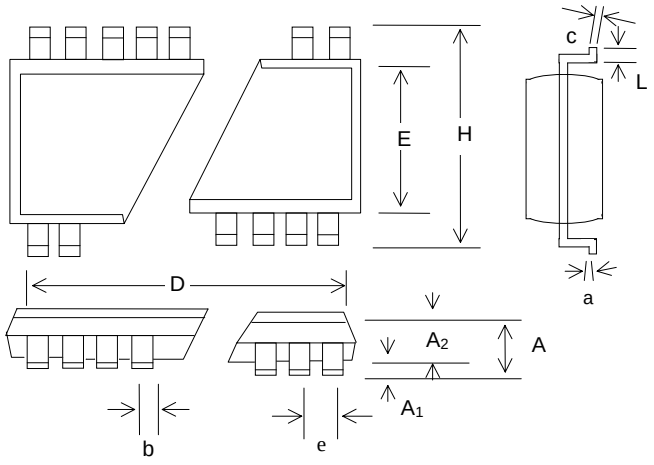
PCB Layout Suggestion



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C35, C36, C37, C38, C39, C40, C41, and C4 (all are 0.1µf) should **always** be used and placed as close as possible to their VDD pins.

Approved Product

Package Drawing and Dimensions



48 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.20	0.31	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.0135	0.203	0.254	0.343
c	0.005	.008	0.010	0.127	0.20	0.254
D	0.620	0.625	0.637	15.75	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.0256 BSC			0.640 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.024	0.030	0.040	0.61	0.76	1.02
a	0º	4º	8º	0º	4º	8º

Ordering Information

Part Number	Package Type	Production Flow
C8750AYB	48 PIN SSOP	Commercial, 0ºC to +70ºC

Marking: Example: IMI
C8750
Date Code, Lot #

IMIC8750AYB

- Flow: B = Commercial, 0ºC to + 70ºC
- Package: Y = SSOP
- Revision
- IMI Device Number