High Performance Pentium® 4 Clock Synthesizer

Product Features

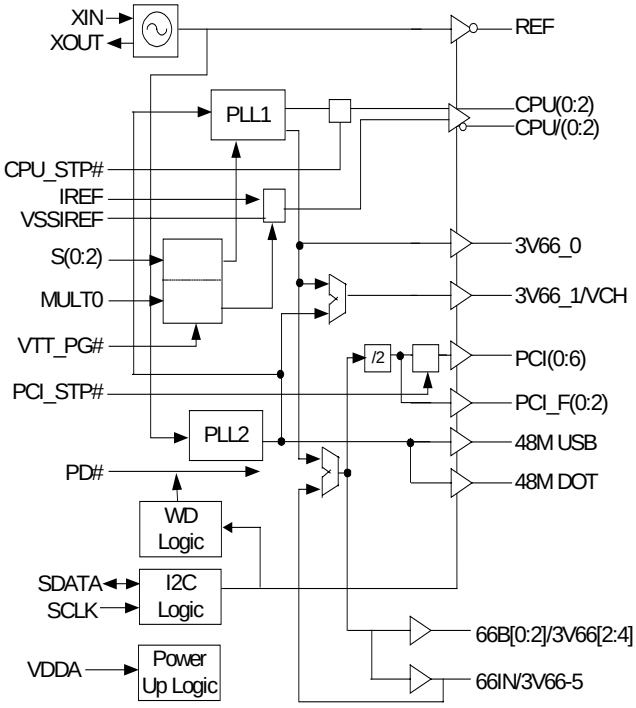
- Supports Pentium® 4 Type CPUs
- 3.3 Volt Power Supply
- 10 Copies of PCI Clocks
- 3 Differential CPU Clocks
- SMBus Support with Read-back Capabilities
- Spread Spectrum EMI Reduction
- Dial-a-Frequency™ Features
- Dial-a-dB™ Features
- 56 Pin SSOP and TSSOP Package

Frequency Table

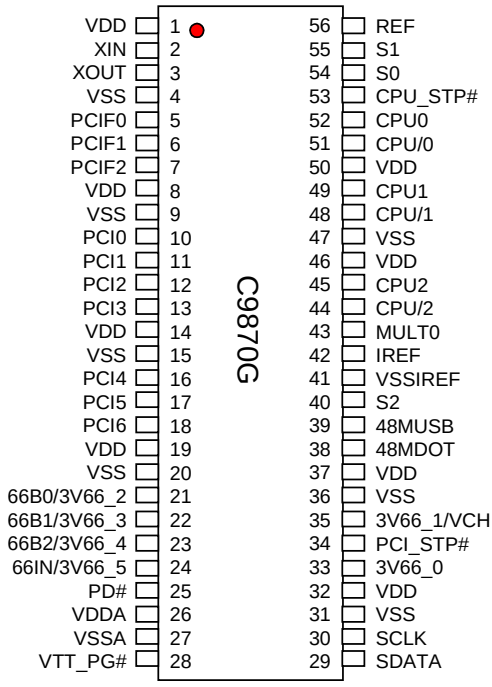
S2	S1	S0	CPU (0:2)	3V66	66BUFF(0:2)/ 3V66(0:4)	66IN/ 3V66-5	PCI_F PCI	REF	USB/ DOT
1	0	0	66M	66M	66IN	66MHz clock input	66IN/2	14.318M	48M
1	0	1	100M	66M	66IN	66MHz clock input	66IN/2	14.318M	48M
1	1	0	200M	66M	66IN	66MHz clock input	66IN/2	14.318M	48M
1	1	1	133M	66M	66IN	66MHZ clock input	66IN/2	14.318M	48M
0	0	0	66M	66M	66M	66M	33 M	14.318M	48M
0	0	1	100M	66M	66M	66M	33 M	14.318M	48M
0	1	0	200M	66M	66M	66M	33 M	14.318M	48M
0	1	1	133M	66M	66M	66M	33 M	14.318M	48M
M	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	0	1	TCLK/2	TCLK/4	TCLK/4	TCLK/4	TCLK/8	TCLK	TCLK/2
M	1	0	150M	50M	50M	50M	25M	14.318M	48M
M	1	1	166.6M	55.5M	55.5M	55.5M	27.7M	14.318M	48M

Note: TCLK is a test clock over driven on the XTAL_IN input during test mode. M= driven to a level between 1.0 and 1.8 Volts
If the S2 pin is at a M level during power up, a 0 state will be latched into the devices internal state register.

Block Diagram



Pin Configuration



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Pin Description

PIN	NAME	PWR	I/O	Description
2	**XIN**		I	Oscillator Buffer Input. Connect to a crystal or to an external clock.
3	**XOUT**	VDD	O	Oscillator Buffer Output. Connect to a crystal. Do not connect when an external clock is applied at XIN.
52, 51, 49, 48, 45, 44	**CPU, CPU/ (0:2)**	VDD	O	Differential host output clock pairs. See the frequency table on page one of this data sheet for frequencies and functionality.
10, 11, 12, 13, 16, 17, 18	**PCI(0:6)**	VDDP	O	PCI Clock Outputs. Are synchronous to 66IN or 3V66 clock. See Frequency Table on page one of this data sheet.
5, 6, 7	**PCIF (0:2)**	VDD	O	33Mhz PCI clocks, which are ÷2 copies of 66IN or 3V66 clocks, may be free running (not stopped when PCI_STP# is asserted low) or may be stoppable depending on the programming of SMBus register Byte3, Bits (3:5).
56	**REF**	VDD	O	Buffered Output copy of the device's XIN clock.
42	**IREF**	VDD	I	Current reference programming input for CPU buffers. A resistor is connected between this pin and VSSIREF. See CPU Clock current Select Table in page 18 of this data sheet.
28	**VTT_PG#**	VDD	I	Qualifying input that latches S (0:2) and MULT0. When this input is at a logic low, the S (0:2) and MULT0 are latched
39	**48MUSB**	VDD48	O	Fixed 48MHz USB Clock Outputs.
38	**48MDOT**	VDD48	O	Fixed 48MHZ DOT Clock Outputs.
33	**3V66_0**	VDD	O	3.3 Volt 66 MHz fixed frequency clock.
35	**3V66_1/VCH**	VDD	O	3.3 volt clock selectable with SMBus byte0, Bit5, when Byte5, Bit5. When Byte 0 Bit 5 is at a logic 1, then this pin is a 48M output clock. When byte0, Bit5 is a logic 0, then this is a 66M output clock (default).
25	**PD#**	VDD	I PU	This pin is a power down mode pin. A logic low level causes the device to enter a power down state. All internal logic is turned off except for the SMBus logic. All output buffers are stopped. See the Power Down section of this data sheet.
43	**MULT0**		I PU	Programming input selection for CPU clock current multiplier. See CPU Clock Current Select Function Table.
55, 54	**S(0,1)**	I	I	Frequency Select Inputs. See Frequency Table on page 1.
29	**SDATA**	I	I	Serial Data Input. Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See application note AN-0022
30	**SCLK**	I	I	Serial Clock Input. Conforms to the SMBus specification. See application note AN-0022.
40	**S2**	VDD	I T	Frequency Select input. See Frequency Table on page 1. This is a Tri level input that is driven high, low or driven to an intermediate level.
34	**PCI_STP#**	VDD	I PU	PCI Clock Disable Input. When asserted low, PCI (0:6) clocks are synchronously disabled in a low state. This pin does not effect PCIF (0:2) clocks' outputs if they are programmed to be PCIF clocks via the device's SMBus interface.

Pin Description (Cont.)

PIN	NAME	PWR	I/O	Description
53	**CPU_STP#**	VDD	I PU	CPU Clock Disable Input. When asserted low, CPU (0:2) clocks are synchronously disabled in a high state and CPU/(0:2) clocks are synchronously disabled in a low state.
24	**66IN/3V66_5**	VDD	I/O	Input connection for 66CLK(0:2) output clock buffers if S2 = 1, or output clock for fixed 66 MHz clock if S2=0. See table on page 1
21, 22, 23	**66B(0:2)/ 3V66(2:4)**	VDD	O	3.3 volt clock outputs. These clocks are buffered copies of the 66IN clock or fixed at 66 MHz. See table on page 1
1, 8, 14, 19, 32, 37, 46, 50	**VDD**		PWR	3.3V Power Supply
4, 9, 15, 20, 27, 31, 36, 47	**VSS**		PWR	Common Ground
41	**VSSIREF**		PWR	Current reference programming input for CPU buffers. A resistor is connected between this pin and IREF. See CPU Clock current Select Table in page 18 of this data sheet. This pin should also be returned to device VSS.
26	**VDDA**	-	PWR	Analog power input. Used for PLL and internal analog circuits. Is also specifically used to detect and determine when power is at an acceptable level to enable the device to operate.

PU = Internal Pull-Up. PD = Internal Pull-Down. T = Tri level logic input with valid logic voltages of LOW=<0.8V, T=1.0-1.8V and HIGH=>2.0V

2-Wire SMBus Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification. (See Application Note AN-0022).

The device will accept data written to the D2 address and data may read back from address D3. It will not respond to any other addresses, and previously set control registers are retained as long as power in maintained on the device.

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.

Although the data (bits) in the command is considered "don't care"; it must be sent and will be acknowledged.

After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

Note: The Pin# column lists the relevant pin number where applicable. The @Pup column gives the default state at power up.

Serial Control Registers (Cont.)

Byte 0: CPU Clock Register

Bit	@Pup	Pin#	Description
7	0	-	Spread Spectrum Enable 0 = Spread Off, 1 = Spread On This is a Read and Write control bit.
6	0	-	Reserved
5	0	35	3V66_1/VCH frequency Select 0 = 66M selected, 1 = 48M selected This is a Read and Write control bit.
4	Pin 53	44,45,48,49, 51,52	CPU_STP#. Reflects the current value of the external CPU_STP# (pin 53) This bit is Read Only.
3	Pin 34	10,11,12,13, 16,17,18	Reflects the current value of the internal PCI_STP# function when read. Internally PCI_STP# is a logical AND function of the internal SMBus register bit and the external PCI_STP# pin.
2	Pin 40	-	Frequency Select Bit 2. Reflects the value of SEL2 (pin 40). This bit is Read Only.
1	Pin 55	-	Frequency Select Bit 1. Reflects the value of SEL1 (pin 55). This bit is Read Only.
0	Pin 54	-	Frequency Select Bit 0. Reflects the value of SEL0 (pin 54). This bit is Read Only.

Byte 1: CPU Clock Register

Bit	@Pup	Pin#	Description
7	Pin 43	-	MULT0 (Pin 43) Value. This bit is Read Only.
6	0	-	Reserved
5	0	44,45	Controls CPU2 functionality when CPU_STP# is asserted LOW 1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW This is a Read and Write control bit.
4	0	48,49	Controls CPU1 functionality when CPU_STP# is asserted LOW 1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW This is a Read and Write control bit.
3	0	51,52	Controls CPU0 functionality when CPU_STP# is asserted LOW 1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW This is a Read and Write control bit.
2	1	44,45	CPU2 Output Control, 1 = enabled, 0 = disable HIGH and CPU/2 disables LOW This is a Read and Write control bit.
1	1	48,49	CPU1 Output Control, 1 = enabled, 0 = disable HIGH and CPU/1 disables LOW This is a Read and Write control bit.
0	1	51,52	CPU0 Output Control, 1 = enabled, 0 = disable HIGH and CPU/0 disables LOW This is a Read and Write control bit.

Byte 2: PCI Clock Control Register
(all bits are read and write functional)

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	1	18	PCI6 Output Control 1 = enabled, 0 = forced LOW
5	1	17	PCI5 Output Control 1 = enabled, 0 = forced LOW
4	1	16	PCI4 Output Control 1 = enabled, 0 = forced LOW
3	1	13	PCI3 Output Control 1 = enabled, 0 = forced LOW
2	1	12	PCI2 Output Control 1 = enabled, 0 = forced LOW
1	1	11	PCI1 Output Control 1 = enabled, 0 = forced LOW
0	1	10	PCI0 Output Control 1 = enabled, 0 = forced LOW

Byte 3: PCI_F Clock and 48M Control Register
(all bits are read and write functional)

Bit	@Pup	Pin#	Description
7	1	38	48MDOT Output Control 1 = enabled, 0 = forced LOW
6	1	39	48MUSB Output Control 1 = enabled, 0 = forced LOW
5	0	7	PCI_STP#, control of PCI_F2. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW
4	0	6	PCI_STP#, control of PCI_F1. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW
3	0	5	PCI_STP#, control of PCI_F0. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW
2	1	7	PCI_F2 Output Control 1=running, 0=forced LOW
1	1	6	PCI_F1 Output Control 1= running, 0=forced LOW
0	1	5	PCI_F0 Output Control 1= running, 0=forced LOW

Byte 4: DRCG Control Register
(all bits are read and write functional)

Bit	@Pup	Pin#	Description
7	0	-	SS2 Spread Spectrum control bit (0=down spread, 1=Center spread)
6	0	-	Reserved
5	1	33	3V66_0 Output Enabled 1 = enabled, 0 = disabled
4	1	35	3V66_1/VCH Output Enable 1 = enabled, 0 = disabled
3	1	24	3V66_5 Output Enable 1 = enabled, 0 = disabled
2	1	23	66B2/3V66_4 Output Enabled 1 = enabled, 0 = disabled
1	1	22	66B1/3V66_3 Output Enabled 1 = enabled, 0 = disabled
0	1	21	66B0/3V66_2 Output Enabled 1 = enabled, 0 = disabled

Byte 6: Silicon Signature Register
(all bits are read only)

Bit	@Pup	Pin#	Description
7	0	-	Vendor Code 011 = IMI
6	0	-	
5	0	-	
4	0	-	
3	0	-	
2	0	-	
1	1	-	
0	1	-	

Note: When writing to this register the device will acknowledge the write operation, but the data itself will be ignored.

Byte 8: Dial-a-Frequency™ Control Register N
(all bits are read and write functional)

Bit	@Pup	Pin#	Description
7	0	0	N7, MSB
6	0	0	N6
5	0	0	N5
4	0	0	N4
3	0	0	N3
2	0	0	N2
1	0	0	N3
0	0	0	N0, LSB

66IN to 66M Delay Control Table

Byte5		Delay (ns)
Bit5	Bit4	
0	**0**	**4.29**
0	**1**	**4.43**
1	**0**	**3.95 (default)**
1	**1**	**3.95**

Byte 5: Clock control register
(all bits are read and write functional)

Bit	@Pup	Pin#	Description
7	0	-	SS1 Spread Spectrum control bit
6	1	-	SS0 Spread Spectrum control bit
5	0	-	66IN to 66M delay Control MSB, See table
4	0	-	66IN to 66M delay Control LSB, See table
3	0	-	Reserved
2	0	-	48MDOT edge rate control. When set to 1, the edge is slowed by 15%.
1	0	-	Reserved
0	0	-	USB edge rate control. When set to 1, the edge is slowed by 15%

Byte 7: Watch Dog Time Stamp Register

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	**0**	-	Reserved
2	**0**	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

Byte 9: Dial-a-Frequency™ Control Register R
(all bits are read and write functional)

Bit	@Pup	Pin#	Description
7	0	-	R6 MSB
6	0	-	R5
5	0	-	R4
4	0	-	R3
3	**0**	-	R2
2	**0**	-	R1
1	0	-	R0, LSB
0	0	-	R and N register load gate 0=gate closed (data is latched), 1=gate open (data is loading from SMBus registers into R and N)

Dial-a-Frequency™ Feature

SMBus Dial-a-frequency feature is available in this device via Byte8 and Byte9. See our App Note AN-0025 for details on our Dial-a-Frequency™ feature.

P is a large value PLL constant that depends on the frequency selection achieved through the hardware selectors (S1, S0). P value may be determined from the following table:

S(1:0)	P
0 0	32005333
0 1	48008000
1 0	96016000
1 1	64010667

Table 1

Dial-a-dB™ Features

SMBus Dial-a-dB™ feature is available in this device via Byte8 and Byte9. See our App Note AN-0026 for details on the Dial-a-dB™.

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing Electro-Magnetic Interference (EMI) radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control Bytes. See applications note AN-0024 for a more in depth description of Spread spectrum modulation and see the SMBus register section of this data sheet for the exact bit and byte functionally. The following table is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

SS2	SS1	SS0	Spread Mode	Spread %
0	0	0	Down	0, -1.00
0	0	1	Down	0, -1.20
0	1	0	Down	0, -0.50
0	1	1	Down	0, -1.50
1	0	0	Center	+0.50, -0.50
1	0	1	Center	+0.60, -0.60
1	1	0	Center	+0.25, -0.25
1	1	1	Center	+0.75, -0.75

AC Parameters

Symbol	Parameter	66 MHz		100 MHz		133 MHz		200 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
TDC	Xin Duty Cycle	47.5	52.5	47.5	52.5	47.5	52.5	47.5	52.5	%	1, 11, 14
TPeriod	Xin period	69.841	71.0	69.841	71.0	69.841	71.0	69.841	71.0	nS	1, 2, 4, 11
VHIGH	Xin High Voltage	.7Vdd	Vdd	.7Vdd	Vdd	.7Vdd	Vdd	.7Vdd	Vdd	Volts	
VLOW	Xin Low Voltage	0	.3Vdd	0	.3Vdd	0	.3Vdd	0	.3Vdd	Volts	
Tr / Tf	Xin rise and fall times	-	10.0	-	10.0	-	10.0	-	10.0	nS	13
TCCJ	Xin Cycle to Cycle Jitter	-	500	-	500	-	500	-	500	pS	2, 5, 11
CPU at 0.7 Volts Timing											
TSKEW	Any CPU to CPU clock Skew	-	100	-	100	-	100	-	100	pS	2, 5, 17
TCCJ	CPU Cycle to Cycle Jitter	-	150	-	150	-	150		150	pS	2, 17, 22
TDC	CPU and CPU# Duty Cycle	45	55	45	55	45	55	45	55	%	5, 17, 22
TPeriod	CPU and CPU# period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	nS	5, 17, 22
Tr / Tf	CPU and CPU# rise and fall times	175	700	175	700	175	700	175	700	ps	5, 6, 25
	Rise.Fall Matching	-	20%	-	20%		20%	-	20%	-	6, 21, 22
DeltaTr	Rise Time Variation	-	125	-	125	-	125		125	ps	6, 22
DeltaTf	Fall Time Variation	-	125	-	125	-	125	-	125	ps	6, 22
Vcross	crossing point voltage at 0.7 V swing	280	430	280	430	280	430	280	430	mV	5, 22
CPU at 1.0 Volts Timing											
TSKEW	Any CPU to any CPU clock Skew	-	100	-	100	-	100	-	100	pS	2, 5, 17
TCCJ	CPU Cycle to Cycle Jitter	-	150	-	150	-	150		150	pS	2, 17
TDC	CPU and CPU# Duty Cycle	45	55	45	55	45	55	45	55	%	5, 17
TPeriod	CPU and CPU# period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	nS	5, 17
Differential Tr / Tf	CPU and CPU# rise and fall times	175	467	175	467	175	467	175	467	ps	5, 25
SE-DeltaSlew	Absolute Single-ended rise/fall waveform symmetry		325		325		325		325	ps	7, 26
Vcross	Cross point at 1.0 Volt swing	510	760	510	760	510	760	510	760	mV	26
TDC	3V66 Duty Cycle	45	55	45	55	45	55	45	55	%	2, 4
TPeriod	3V66 period	15.0	15.3	15.0	15.3	15.0	15.3	15.0	15.3	nS	1, 2, 4
THIGH	3V66 high time	4.95	-	4.95	-	4.95	-	4.95	-	nS	19
TLOW	3V66 low time	4.55	-	4.55	-	4.55	-	4.55	-	nS	20
Tr / Tf	3V66 rise and fall times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	nS	3
Tskew Unbuffered	3V66 to 3V66 clock skew	-	500	-	500	-	500	-	500	pS	2, 4
Tskew Buffered	3V66 to 3V66 clock skew	-	250	-	250	-	250	-	250	pS	2, 4
TCCJ	DRCG Cycle to Cycle Jitter	-	250	-	250	-	250	-	250	pS	2, 4

AC Parameters (Cont.)

Symbol	Parameter	66 MHz		100 MHz		133 MHz		200 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
TDC	66B(0:2) Duty Cycle	45	55	45	55	45	55	45	55	%	2, 4
Tr / Tf	66B(0:2) rise and fall times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	nS	2, 3
TSKEW	Any 66B to any 66B Skew	-	175	-	175	-	175		175	pS	2, 4
Tpd	66IN to 66B(0:2) propagation delay	2.5	4.5	2.5	4.5	2.5	4.5	2.5	4.5	nS	2, 4
TCCJ	66B(0:2) Cycle to Cycle Jitter	-	100	-	100	-	100	-	100	pS	2, 4, 18
TDC	PCI_F(0:2) PCI (0:6) Duty Cycle	45	55	45	55	45	55	45	55	%	2, 4
TPeriod	PCI_F(0:2) PCI (0:6) period	30.0	-	30.0	-	30.0	-	30	-	nS	1, 2, 4
THIGH	PCI_F(0:2) PCI (0:6) high time	12.0	-	12.0	-	12.0	-	12.0	-	nS	19
TLOW	PCI_F(0:2) PCI (0:6) low time	12.0	-	12.0	-	12.0	-	12.0	-	nS	20
Tr / Tf	PCI_F(0:2) PCI (0:6) rise and fall times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	nS	3
TSKEW	Any PCI clock to Any PCI clock Skew	-	500	-	500	-	500	-	500	pS	2, 4
TCCJ	PCI_F(0:2) PCI (0:6) Cycle to Cycle Jitter	-	250	-	250	-	250	-	250	pS	2, 4
TDC	USB48M Duty Cycle	45	55	45	55	45	55	45	55	%	2, 4
TPeriod	USB48M period	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	nS	2, 4
Tr / Tf	USB48M rise and fall times	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.10	nS	2, 3
TCCJ	USB48M Cycle to Cycle Jitter	-	350	-	350	-	350	-	350	pS	1, 2, 4
TDC	DOT48 Duty Cycle	45	55	45	55	45	55	45	55	%	2, 4
TPeriod	DOT48 period	20.837		20.837		20.837		20.837		nS	2, 4
Tr / Tf	DOT48 rise and fall times	0.5	1.0	0.5	1.0	0.5	1.0	0.5	1.0	nS	2, 4
TCCJ	DOT48Cycle to Cycle Jitter	-	350	-	350	-	350	-	350	pS	2, 4

AC Parameters (Cont.)

Symbol	Parameter	66 MHz		100 MHz		133 MHz		200 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
TDC	REF Duty Cycle	45	55	45	55	45	55	45	55	%	2, 4
TPeriod	REF period	69.8413	71.0	69.8413	71.0	69.8413	71.0	69.8413	71.0	nS	2, 4
Tr / Tf	REF rise and fall times	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	nS	2, 3
TCCJ	REF Cycle to Cycle Jitter	-	1000	-	1000	-	1000	-	1000	pS	2, 4
tpZL, tpZH	Output enable delay (all outputs)	1.0	10.0	1.0	10.0	1.0	10.0	1.0	10.0	nS	11
tpLZ, tpZH	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	1.0	10.0	1.0	10.0	nS	11
tstable	All clock Stabilization from power-up	-	3	-	3	-	3	-	3	mS	11
tss	Stopclock Set Up Time	10.0	-	10.0	-	10.0	-	10.0	-	nS	10
tsh	Stopclock Hold Time	0	-	0	-	0	-	0	-	nS	10
tsu	Oscillator startup time	-	X	-	X	-	X	-	X	mS	12

(VDD = VDDA = 3.3V ±5%, TA = 0°C to +70°C)

Note 1: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 2: All outputs loaded as per table 5 below.
Note 3: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals (see test and measurement setup section of this data sheet)
Note 4: Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals (see test and measurement setup section of this data sheet).
Note 5: This measurement is applicable with Spread ON or Spread OFF.
Note 6: Measured from Vol = 0.175V to Voh = 0.525V.
Note 7: Measurements taken from common mode waveforms, measure rise/fall time from 0.41 to 0.86V. Rise/fall time matching is defined as "the instantaneous difference between maximum clk rise (fall) and minimum clk# fall (rise) time, or minimum clk rise (fall) and maximum clk# fall (rise) time". This parameter is designed form waveform symmetry.
Note 8: The time specified is measured from when all VDD's reach their supply rail (3.3V) till the frequency output is stable and operating within the specifications.
Note 9: Measured from when both SEL1 and SEL0 are low
Note 10: CPU_STP# and PCI_STP# setup time with respect to any PCI_F clock to guarantee that the effected clock will stop or start at the next PCI_F clock's rising edge.
Note 11: When Xin is driven from an external clock source.
Note 12: When Crystal meets minimum 40 ohm device series resistance specification.
Note 13: Measured between 0.2Vdd and .7Vdd
Note 14: This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
Note 15: Vpullup(external)=1.5V, Min=(Vpullup(external)/2)-150mV, Max=(Vpullup(external)/2)+150mV
Note 16: Vp = V pull-up (external), Vdif specifies the minimum input differential voltage (Vtr-Vcp) required for switching, where Vtr is the true input level and Vcp is the compliment input level.
Note 17: Measured at crossing point (Vx) or where subtraction of CLK-CLK# crosses 0 volts.
Note 18: This figure is additive to any jitter already present when the 66IN pin is being used as an input. Otherwise a 500 ps jitter figure is specified.
Note 19: THIGH is measured at 2.4V for non host outputs.
Note 20: TLOW is measured at 0.4V for all outputs.
Note 21: Determined as a fraction of 2*(Trise-Tfall)/ (Trise+Tfall).
Note 22: Test load is Rta=33.2 ohms, Rd=49.9 ohms.
Note 23: These crossing points refer to only crossing points containing a rising edge of a Host output.
Note 24: This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
Note 25: Measurement taken from differential waveform, from –0.35V to +0.35V.
Note 26: Measured in absolute voltage, i.e. single-ended measurement.

Maximum Lumped Capacitive Output Loads

Clock	Max Load	Units
PCI Clocks	30	pF
3V66 (0,1)	30	pF
66B(0:2)	30	pF
48MUSB Clock	20	pF
48MDOT	10	pF
REF Clock	30	pF

Table 5

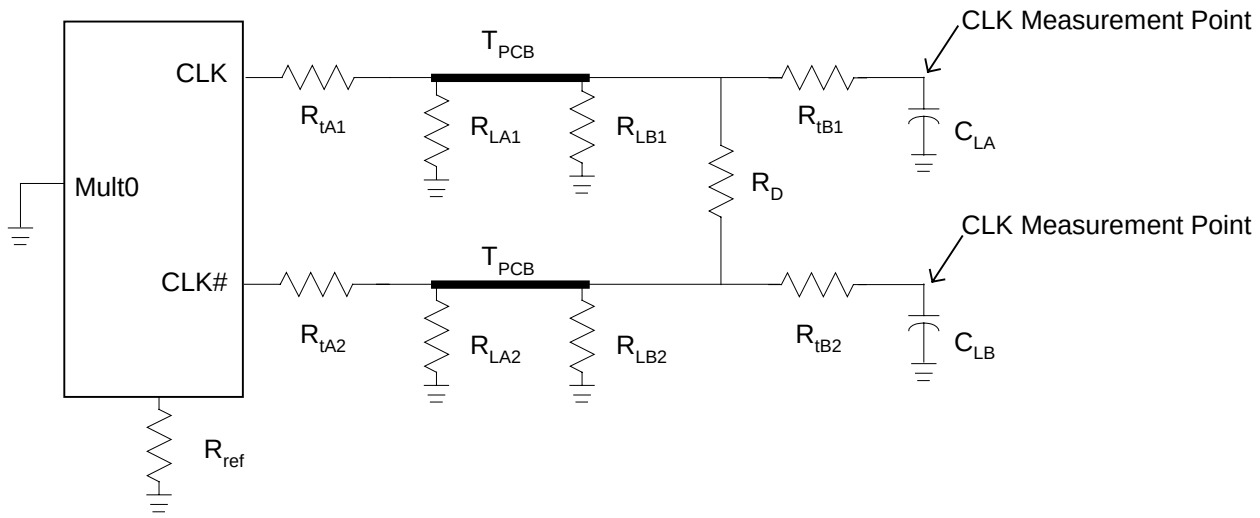
Maximum Ratings

Input Voltage Relative to VSS:	VSS-0.3V
Input Voltage Relative to VDDQ or AVDD:	VDD+0.3V
Storage Temperature:	-65°C to + 150°C
Operating Temperature:	0°C to +85°C
Maximum Power Supply:	3.5V

Test and Measurement Setup

For Differential CPU Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

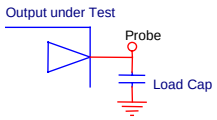


Lumped Test Load Configuration

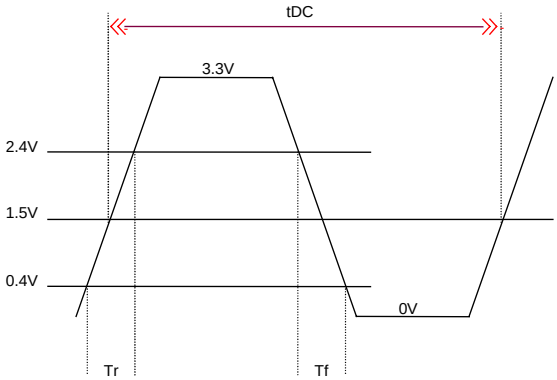
Component	0.7 Volt Amplitude Value	1.0 Volt Amplitude Value
R_{tA1}, R_{tA2}	33 Ω	0 Ω
R_{LA1}, R_{LA2}	49.9 Ω	∞
T_{PCB}	3” 50 ΩZ	3” 50 ΩZ
R_{LB1}, R_{LB2}	∞	63 Ω
R_D	∞	470 Ω
R_{tB1}, R_{tB2}	0 Ω	33 Ω
C_{LA}, C_{LB}	2pF	2 pF
R_{ref}	475 Ω w/mult0=1	221 Ω w/mult0=0

Test and Measurement Setup (Cont.)

For single Ended Output Signals



3.3V signals

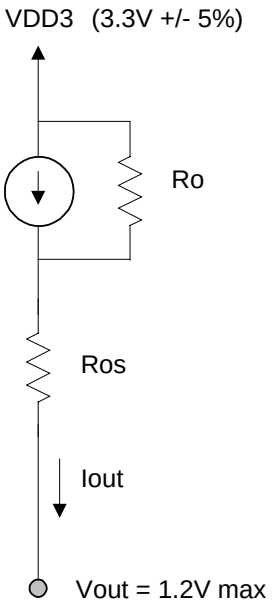


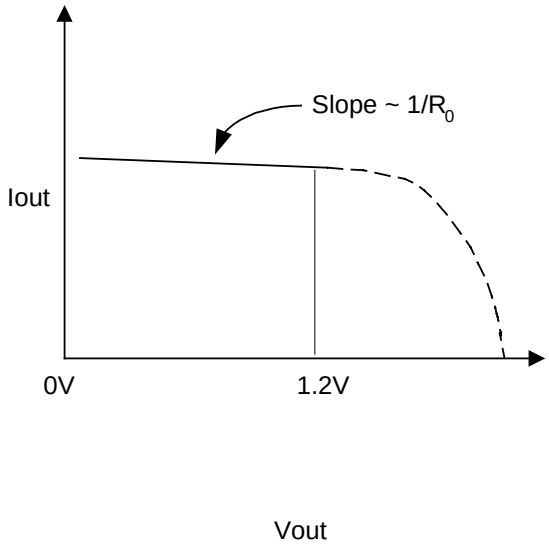
Buffer Characteristics

Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained in the previous table of this data sheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit - Ro (see figure below).
2. Minimum and maximum required voltage operation range of the circuit – Vop (see figure below).
3. Series resistance in the buffer circuit – Ros (see figure below).
4. Current accuracy at given configuration into nominal test load for given configuration.





Host Clock (HCSL) Buffer Characteristics

Characteristic	Minimum	Maximum
Ro	3000 Ohms (recommended)	N/A
Ros		
Vout	N/A	1.2V

Iout is selectable depending on implementation. The parameters above apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is +/- 7% as shown in the current accuracy table.

CPU Clock Current Select Function

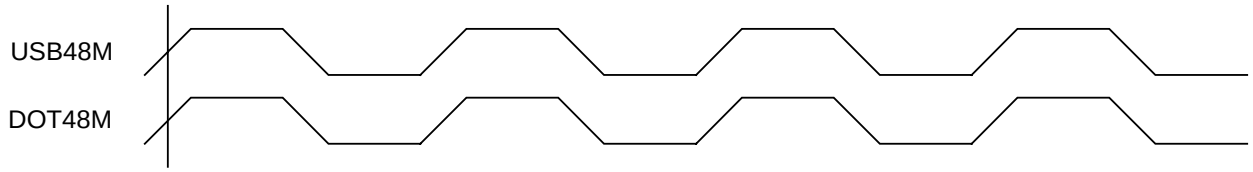
Mult0	Board Target Trace/Term Z	Reference R, Iref – Vdd (3*Rr)	Output Current	Voh @ Z
0	50 Ohms	Rr = 221 1%, Iref = 5.00mA	Ioh = 4*Iref	1.0V @ 50
1	50 Ohms	Rr = 475 1%, Iref = 2.32mA	Ioh = 6*Iref	0.7V @ 50

Group Timing Relationship and Tolerances

	Offset	Tolerance	Conditions
3V66 to PCI	2.5 nS	±1.0 nS	3V66 Leads PCI (un-buffered mode)
USB to DOT 48M Skew	0.0 nS	±1.0 nS	0 degrees phase shift
66B(0:2) to PCI offset	2.5 nS	±1.0 nS	66B leads PCI (buffered mode)

USB and DOT 48M Phase Relationship

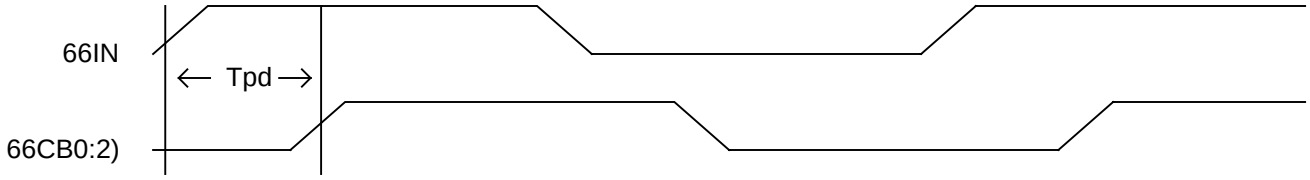
The 48MUSB and 48MDOT clocks are in phase. It is understood that the difference in edge rate will introduce some inherent offset. When 3V66_1/VCH clock is configured for VCH (48MHz) operation it is also in phase with the USB and DOT outputs.



48MUSB and 48MDOT Phase Relationship Figure

66IN to 66B(0:2) Buffered Prop Delay

The 66IN to 66B(0:2) output delay is shown below.

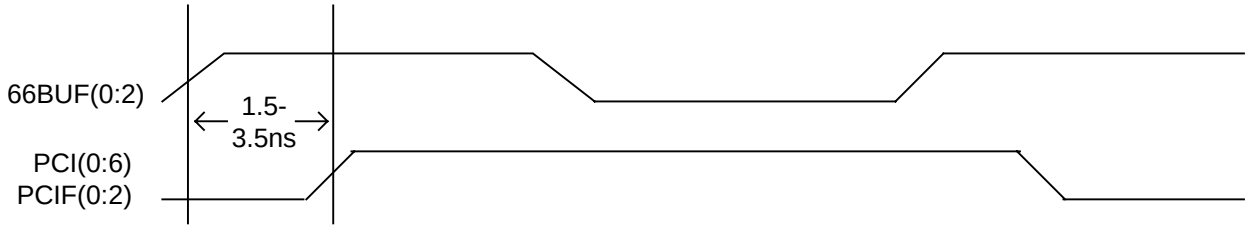


66IN to 66B(0:2) Output Delay Figure

The Tpd is the prop delay from the input pin (66IN) to the output pins (66B[0:2]). The outputs' variation of Tpd is described in the AC parameters section of this data sheet. The measurement taken at 1.5 volts.

66BUF to PCI Buffered Clock Skew

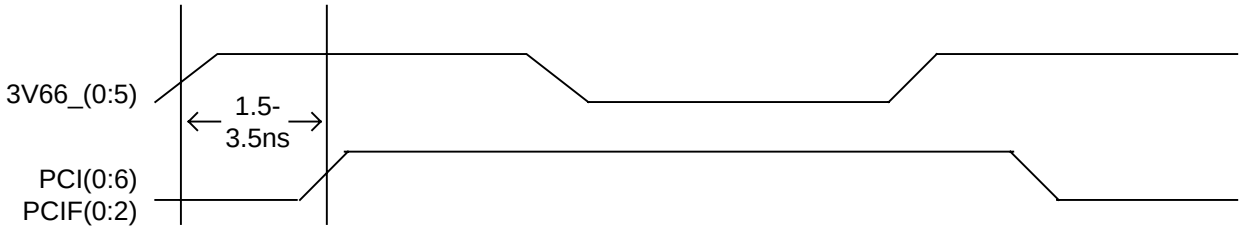
The following figure shows the difference (skew) between the 3V33(0:5) outputs when the 66M clocks are connected to 66IN. This offset is described in the Group Timing Relationship and Tolerances section of this data sheet. The measurements were taken at 1.5 volts.



Buffer Mode – 33V66(0:1); 66BUF(0:2) Phase Relationship

3V66 to PCI Un-Buffered Clock Skew

The following figure show the timing relationship between 3V66_(0:5) and PCI(0:6) and PCIF(0:2) when configured to run in the un-buffered mode.



Un-buffered Mode - 3V66_(0:5) to PCI (0:6) and PCIF(0:2) Phase Relationship

Special Functions

PCI_F and IOAPIC Clock Outputs

The PCIF clock outputs are intended to be used, if required, for systems IOAPIC clock functionality. ANY 2 of the PCI_F clock outputs can be used as IOAPIC 33Mhz clock outputs. They are 3.3V outputs will be divided down via a simple resistive voltage divider to meet specific system IOAPIC clock voltage requirements. In the event these clocks are not required, then these clocks can be used as general PCI clocks or disabled via the assertion of the PCI_STP# pin.

3V66_1/VCH Clock Output

The 3V66_1/VCH pin has a dual functionality, which is selectable via SMBus.

Configured as DRCG (66M), SMBus Byte0, Bit 5 = '0'

The default condition for this pin is to power up in a 66M operation. In 66M operation this output is SSCG capable and when spreading is turned on, this clock will be modulated.

Configured as VCH (48M), SMBus Byte0, Bit 5 = '1'

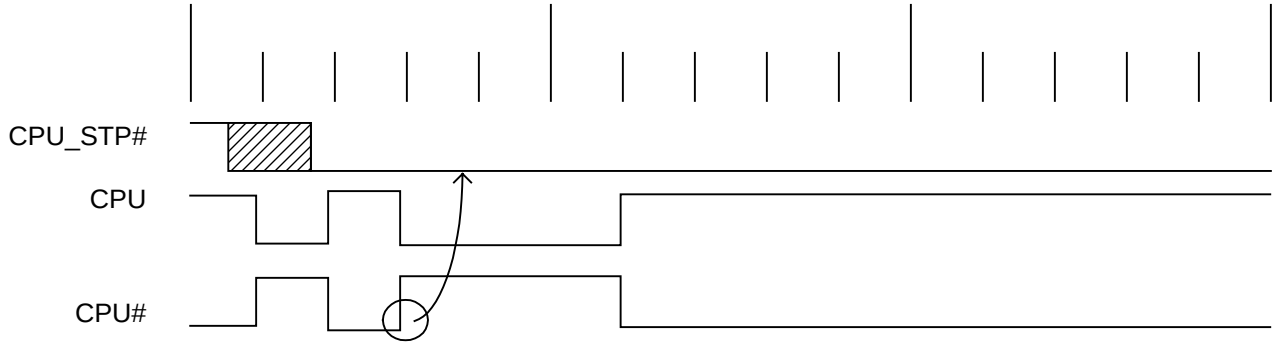
In this mode, the output is configured as a 48Mhz non-spread spectrum output. This output is phase aligned with the other 48M outputs (USB and DOT), to within 1ns pin to pin skew. The switching of 3V66_1/VCH into VCH mode occurs at system power on. When the SMBus Bit 5 of Byte 0 is programmed from a '0' to a '1', the 3V66_1/VCH output may glitch while transitioning to 48M output mode.

CPU_STP# Clarification

The CPU_STP# signal is an active low input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function.

CPU_STP# - Assertion (transition from logic '1' to logic '0')

When CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped after being sampled by 2 falling CPU clock edges. The final state of the stopped CPU signals is CPU = high and CPU0# = Low. There is no change to the output drive current values during the stopped state. The CPU is driven high with a current value equal to (Mult 0 'select') x (Iref), and the CPU# signal will not be driven. Due to external pulldown circuitry CPU# will be low during this stopped state.



Assertion CPU_STP# Waveform Figure

CPU_STP# Functionality Table

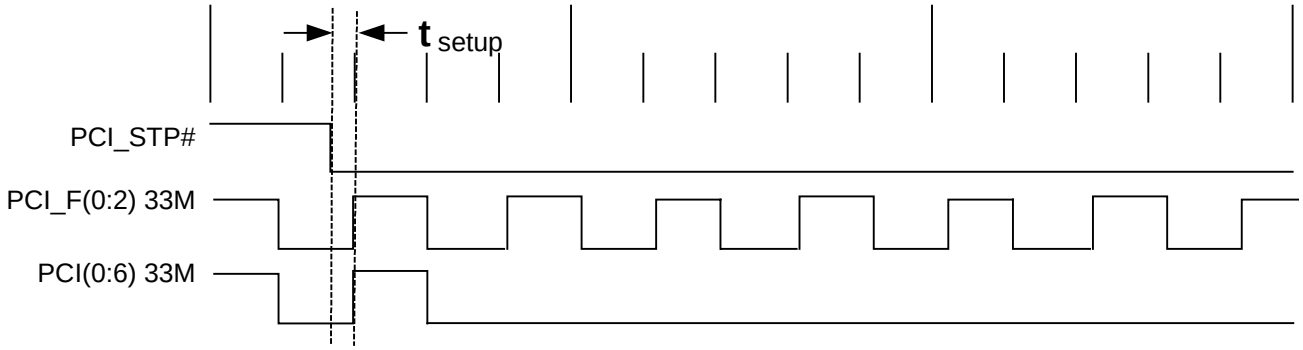
CPU_STP#	CPU#4	CPU	DRCG	66CLK(0:2)	PCI_F/PCI	PCI	USB/DOT
1	Normal	Normal	66M	66Input	66Input/2	66Input/2	48M
0	Iref*Mult	Float	66M	66Input	66Input/2	66Input/2	48M

CPU_STP# De-assertion (transition from logic '0' to logic '1')

The de-assertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produces when the clock resumes. The maximum latency from the de-assertion to active outputs is no more than 2 CPU clock cycles.

PCI_STP# Clarification

The PCI_STP# signal is an active low input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The setup time for capturing PCI_STP# going low is 10 nsec (t_{setup}). The PCI_F (0:2) clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free running.



PCI_STP# Waveform Figure

PCI_STP# - De-assertion (transition from logic '0' to logic '1')

The de-assertion of the PCI_STP# signal will cause all PCI(0:6) and stoppable PCI_F(0:2) clocks to resume running in a synchronous manner within 2 PCI clock periods after PCI_STP# transitions to a high level.

Note that the PCI STOP function is controlled by 2 inputs. One is the device PCI_STP# pin number 34 and the other is SMBus byte 0 bit 3. These 2 inputs to the function are logically ANDed. If either the external pin or the internal SMBus register bit is set low then the stoppable PCI clocks will be stopped in a logic low state. Reading SMBus Byte 0 Bit 3 will return a 0 value if either of these control bits are set low thereby indicating the devices stoppable PCI clocks are not running.

PD# (Power Down) Clarification

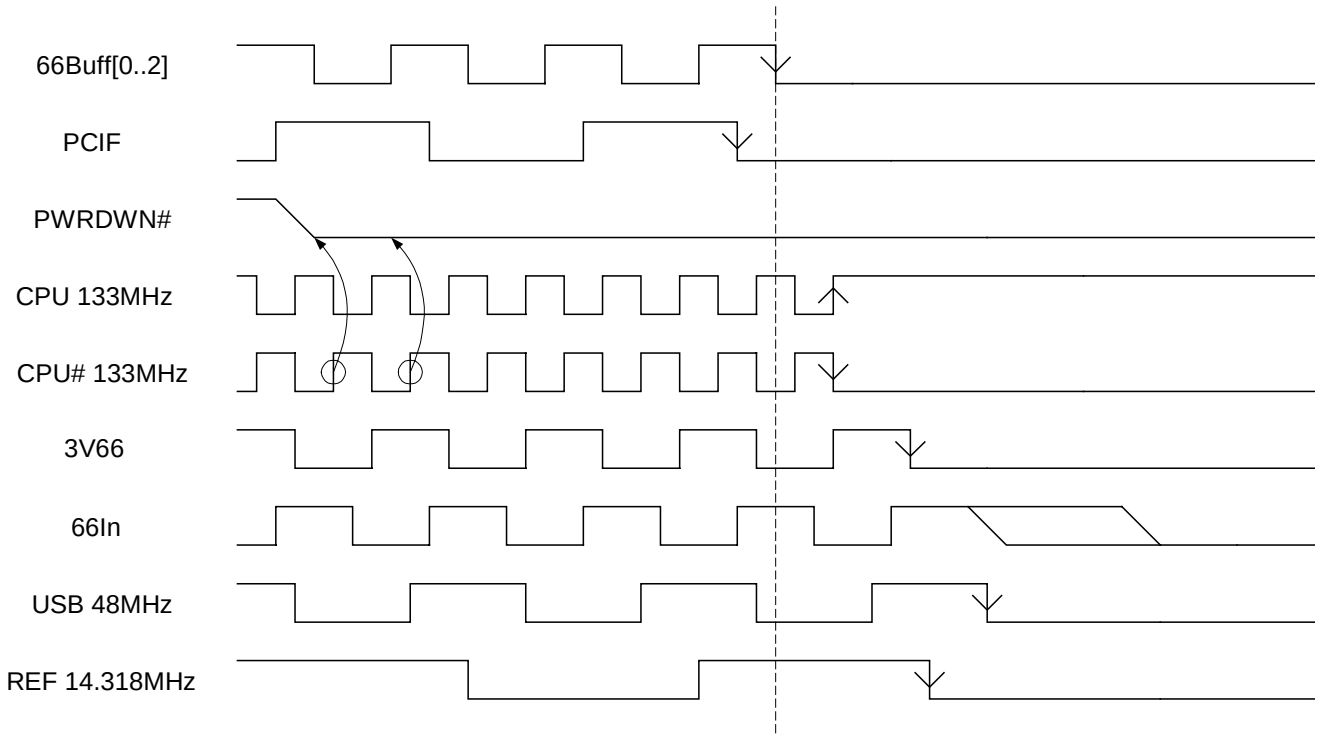
The PD# (Power Down) pin is used to shut off ALL clocks prior to shutting off power to the device. PD# is an asynchronous active low input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is low, all clocks are driven to a low value and held there and the VCO and PLL's are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the low 'stopped' state.

PD# Functionality

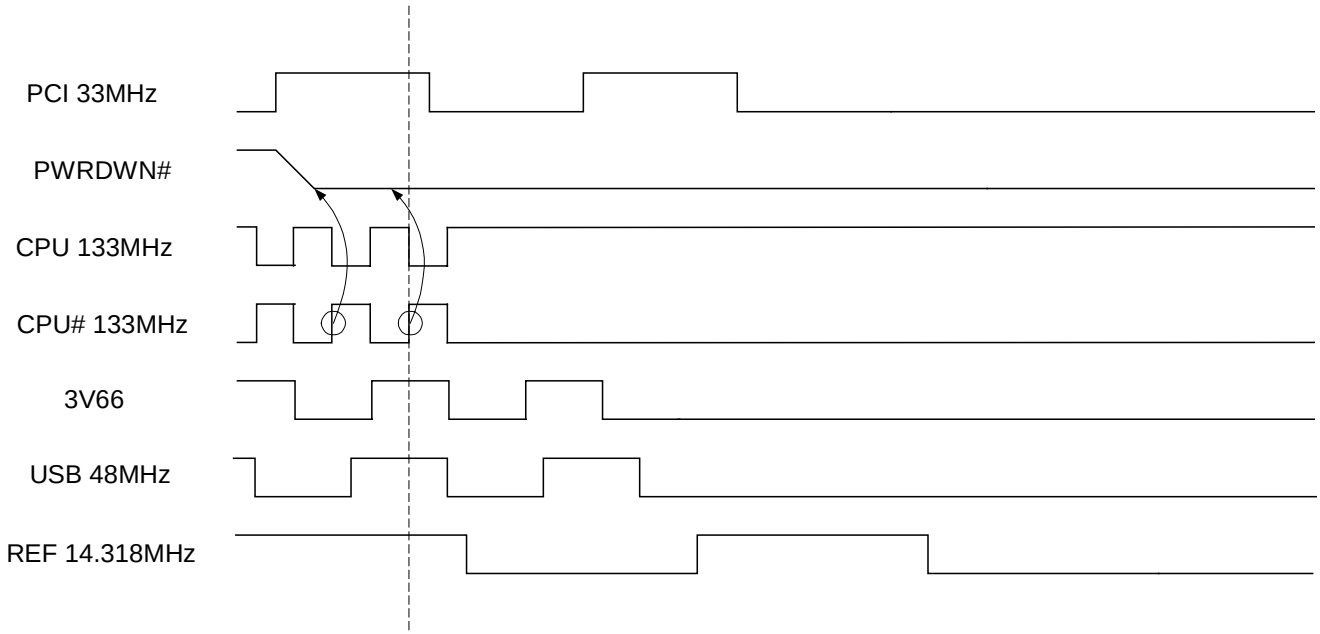
PD#	CPU	CPU#	DRCG	66CLK (0:2)	PCI_F/PCI	PCI	USB/DOT
1	Normal	Normal	66M	66Input	66Input/2	66Input/2	48M
0	Iref*2	Float Low	Low	Low	Low	Low	Low

PD# - Assertion (transition from logic 'l' to logic '0')- Buffered Mode

When PD# is sampled low by two consecutive rising edges of the CPU# clock, then on the next high to low transition of PCIF, the PCIF clock is stopped low. On the next high to low transition of 66Buff, the 66Buff clock is stopped low. From this time, each clock will stop low on it's next high to low transition, except the CPU clock. The CPU clocks are held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# un-driven. After the last clock has stopped, the rest of the generator will be shut down.



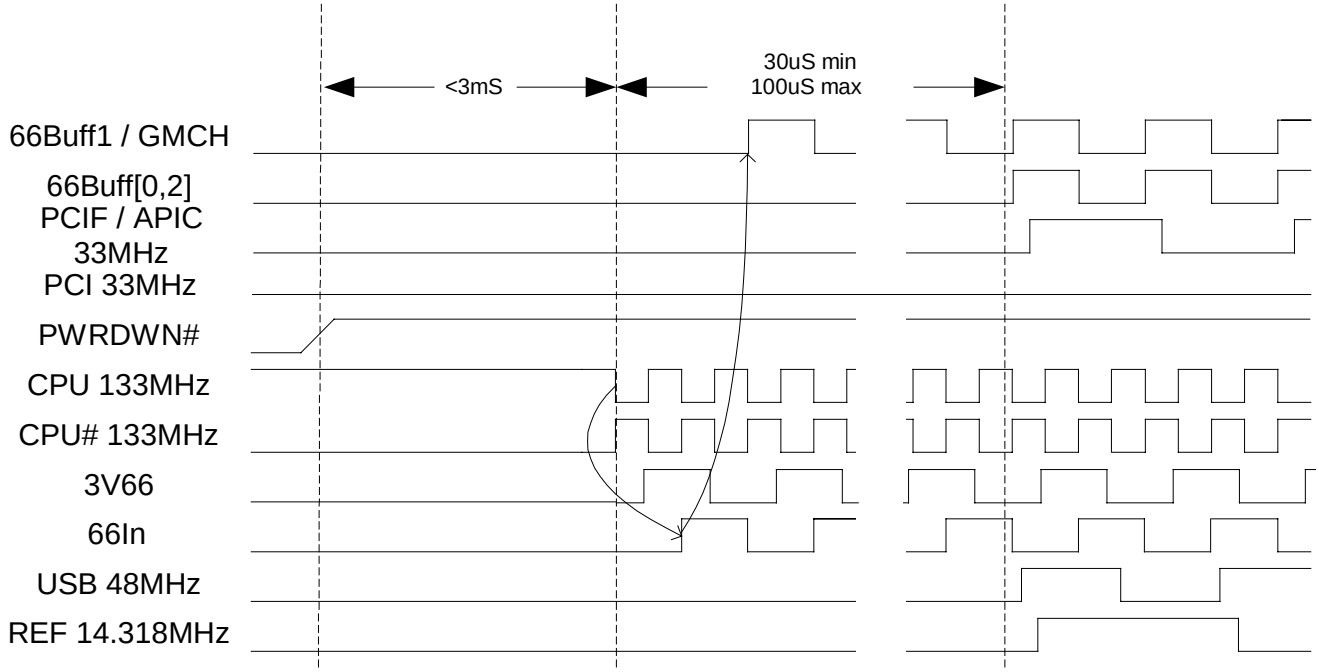
Power Down Assertion Timing Waveforms Figure – Buffered Mode



Power Down Assertion Timing Waveforms Figure – Non-Buffered Mode

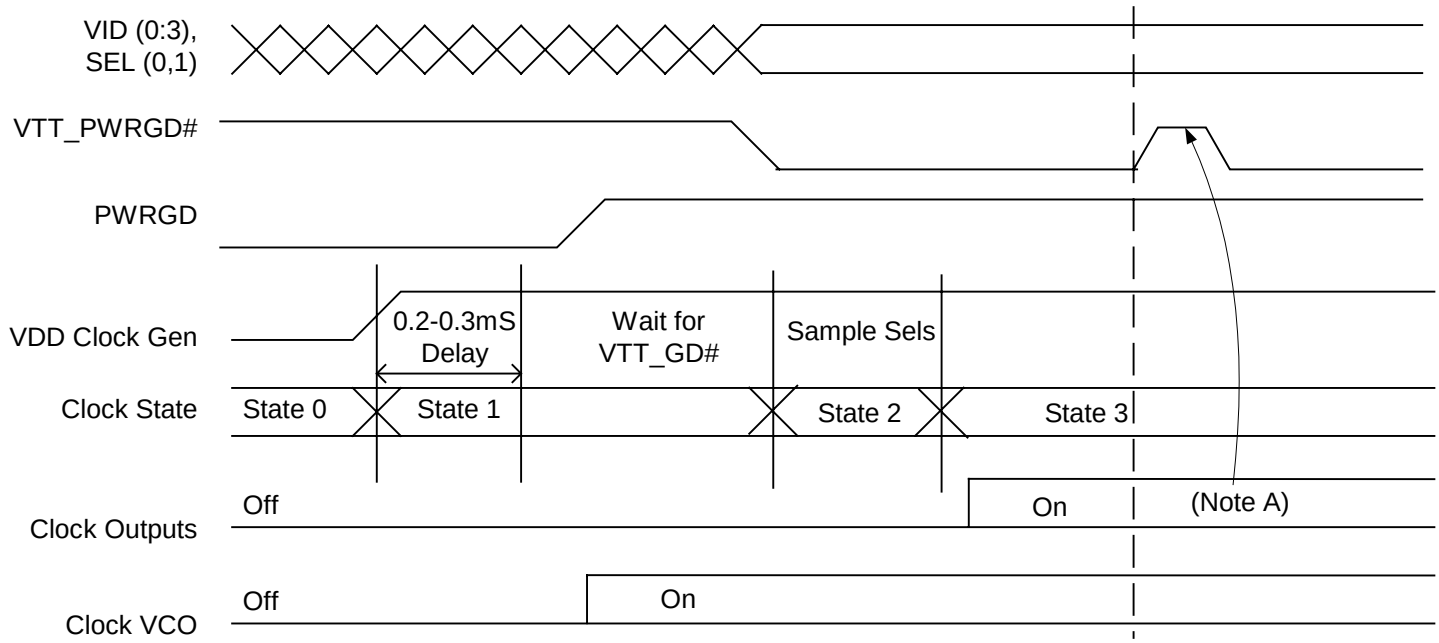
PD# - De-assertion (transition from logic ‘0’ to logic ‘1’)

The power-up latency between PD# rising to a valid logic ‘1’ level and the starting of all clocks is less than 3.0 mS.



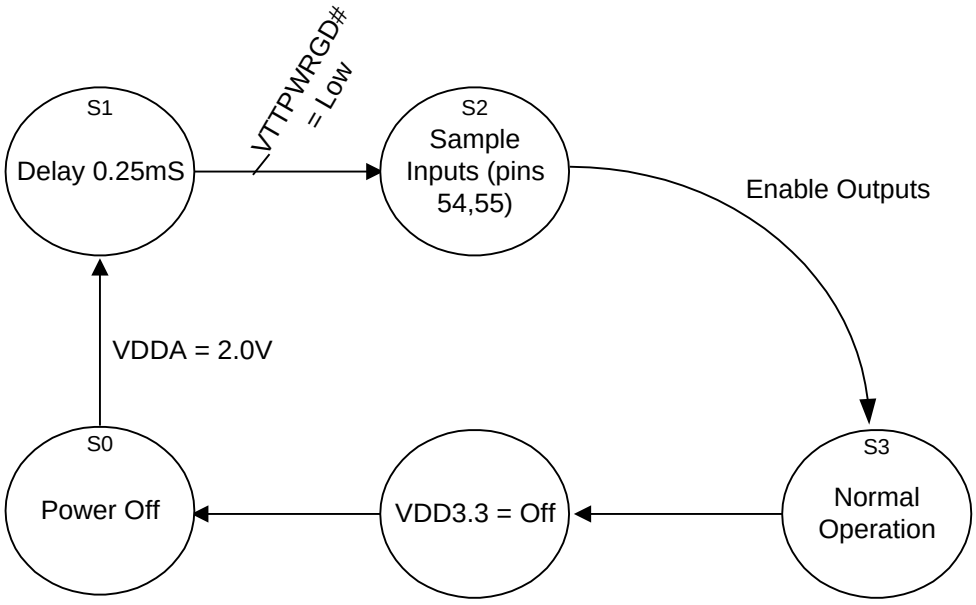
Power Down De-Assertion Timing Waveforms Figure

VTT_PWRGD# Timing Diagram



Note A: Device is not effected, VTT_PWRGD# is ignored.

Clock Generator PowerUp/Run State Diagram



DC Characteristics

Current Accuracy

	Conditions	Configuration	Load	Min	Max
Iout	VDD = nominal (3.30V)	M0 = 0 or 1 and Rr shown in Table	Nominal test load for given configuration	-7% Inom	+ 7% Inom
Iout	VDD = 3.30 +/- 5%	All combinations of M0 or 1 and Rr shown in Table	Nominal test load for given configuration	-12% Inom	+ 12% Inom

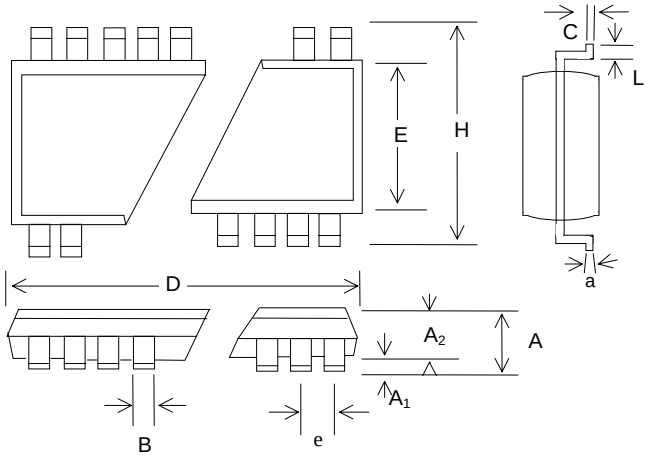
Note: Inom refers to the expected current based on the configuration of the device.

DC Component Parameters (VDD = 3.3V ±5%, TA = 0°C to +70°C)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Dynamic Supply Current	Idd3.3V	-	-	280	mA	All frequencies at maximum values, Note 1
Power Down Supply current	Ipd3.3V	-	-	See Note 2	mA	PD# Asserted
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin Inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	30	36	42	pF	Measured from the Xin or Xout Pin to Ground.

Note1: All outputs loaded as per maximum capacitive load table.
Note2: Absolute value = ((Programmed CPU Iref) (7)) + 10 ma

Package Drawing and Dimensions



56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.720	0.725	0.730	18.29	18.42	18.54
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

56 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Product Flow
C9870GY	56 Pin SSOP	Commercial, 0° to 85°C
C9870GT	56 Pin TSSOP	Commercial, 0° to 85°C

Marking: Example: IMI
C9870
Date Code, Lot #

C9870GY

- Package
  Y = SSOP
  T = TSSOP
- Revision
- Device Number

Notice

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Document Title: C9870G High Performance Pentium® 4 Clock Synthesizer **Document Number:** 38-07108				
Rev	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107512	06/14/01	NDP	Convert from IMI to Cypress