C9815

Low EMI Clock Generator for Intel® 133MHz/2DIMM Chipset Systems

Product Features

- Meets Intel's 133MHz/SDRAM chipset specification
- 3 copies of CPU Clock (CPU[0:1] and CPU2_ITP)
- 9 copies of SDRAM Clock (SDRAM[0:7] and DCLK)
- 7 copies of PCI Clock
- 3 copies of 3V66 Clock
- 2 copies of IOAPIC Clock
- 1 REF Clock
- 1 USB Clock (Non SSC)
- 1 DOT Clock (Non SSC)
- Cypress Spread Spectrum for best EMI reduction
- SMBUS Support with read back
- 56 Pin SSOP package

Block Diagram

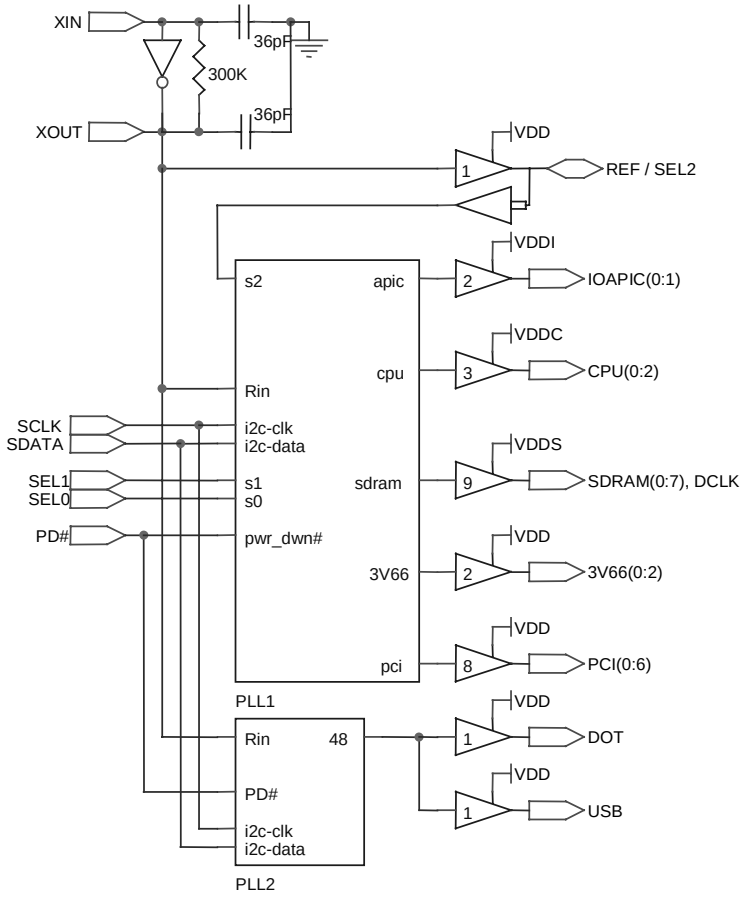


Fig.1

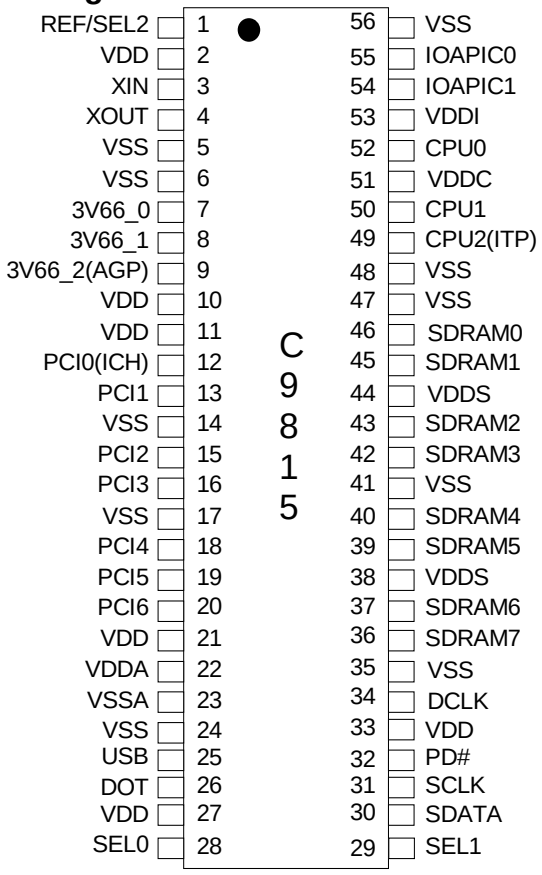
Frequency Table (MHz)

SEL2	SEL1	SEL0	CPU	SDRAM	PCI
X	0	0	Tri-state		
X	0	1	Test Mode		
0	1	0	66.6 MHz	100 MHz*	33.3
0	1	1	100 MHz	100 MHz*	33.3
1	1	0	133.3 MHz	133.3 MHz	33.3
1	1	1	133.3 MHz	100 MHz*	33.3

Table 1

Note: The following clocks remain fixed frequencies except in Test Mode: 3V66=66.6MHz, USB/DOT=48MHz, REF=14.318MHz and IOAPIC=33.3MHz.
*SMBUS programmable to 133 MHz, Byte 3, Bit 0

Pin Configuration



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Pin Description

PIN No.	Pin Name	PWR	I/O	Description
1	**SEL2/REF**	VDD	I/O	This is a bi-directional pin (see app. note, p.5). At power up, it is an input pin Sel2 for selecting the CPU/SDRAM frequencies (see table 1 p.1). When the power reaches the rail, the state of Sel2 is latched, and this pin becomes REF, a buffer output of the signal applied at Xin, typically 14.318MHz. This pin has an Internal Pull-Down. Typical 50KΩ (range 20KΩ to 70KΩ)
3	**XIN**	VDD	I	On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal
4	**XOUT**	VDD	O	On-chip reference oscillator pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin remains unconnected.
12,13,15, 16,18,19, 20	**PCI0_ICH PCI(1..6)**	VDD	O	3.3V PCI clock outputs. They are Synchronous to CPU clocks. See fig.3, page4.
7, 8, 9	**3V66(0:2)**	VDD	O	3.3V Fixed 66.6 MHz clock outputs. See fig.3 page 4.
25	**USB**	VDD	O	3.3V Fixed 48 MHz clock outputs
26	**DOT**	VDD	O	3.3V Fixed 48 MHz clock outputs
28, 29	**SEL(0,1)**	VDD	I	3.3V LVTTL inputs for logic selection. This pin has an Internal Pull-Up. Typical 250KΩ (range 200KΩ to 500KΩ)
30	**SDATA**	VDD	I/O	Serial data input pin. Conforms to the SMBUS specification of a Slave Receive/Transmit device. This pin is an input when receiving data. It is an open drain output when acknowledging or transmitting data. See SMBUS function description, pp.6,7,8.
31	**SCLK**	VDD	I	Serial clock input pin. Conforms to the SMBUS specification.
32	**PD#**	VDD	I	3.3V LVTTL compatible input. When held LOW, the device enters a power down mode. See description page 3. This pin has an Internal Pull-Up. Typical 250KΩ (range 200KΩ to 500KΩ)
34	**DCLK**	VDD	O	3.3V SDRAM feedback clock. See table1, p.1 for frequency selection. See fig.3, page 4 for timing relationship.
36,37,39,40, 42,43,45, 46	**SDRAM(7..0)**	VDDS	O	3.3V SDRAM DIMM clocks. See table1, p.1 for frequency selection. See fig.3, page 4 for timing relationship.
49, 50, 52	**CPU(2)_ITP,CPU(1,0)**	VDDC	O	2.5V Host clock outputs. See table 1 p. 1 for frequency selection.
54, 55	**IOAPIC(1,0)**	VDDI	O	2.5V IOAPIC clock outputs. See fig.3 p.4 for timing relationship.
2,10, 11, 21, 27, 33	**VDD**	-		3.3V Common Power Supply
22	**VDDA**	-		Analog circuitry 3.3V Power Supply
23	**VSSA**	-		Analog circuitry power supply Ground pins.
51, 53	**VDDC, VDDI**	-		2.5V Power Supply's
5, 6,14, 17, 24, 35, 41, 47, 48, 56	**VSS**	-		Common Ground pins.
38, 44	**VDDS**	-		3.3V power support for SDRAM clock output drivers.

A bypass capacitor (0.1μF) should be placed as close as possible to each positive power pin. If these bypass capacitors are not close to the pins their high frequency filtering characteristic will be cancelled by the lead inductance of the traces.

Test Mode Function

Test Mode Functionality

SEL2	SEL1	SEL0	CPU	SDRAM	3V66	PCI	USB/DOT	REF	IOAPIC
x	0	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6

Table 2

Note: TCLK is a test clock over driven on the XIN input during test mode.

Power Management Functions

Power Management on this device is controlled by a single pin, PD# (pin32). When PD# is high (default) the device is in normal running mode and all signals are active.

When PD# is asserted (forced) low, the device is in shutdown (or in power down) mode and all power supplies (3.3V and 2.5V except for VDDA/pin 27) may be removed. When in power down, all outputs are synchronously stopped in a low state (see Fig.2 below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I²C function is also disabled.

Power Management Timing

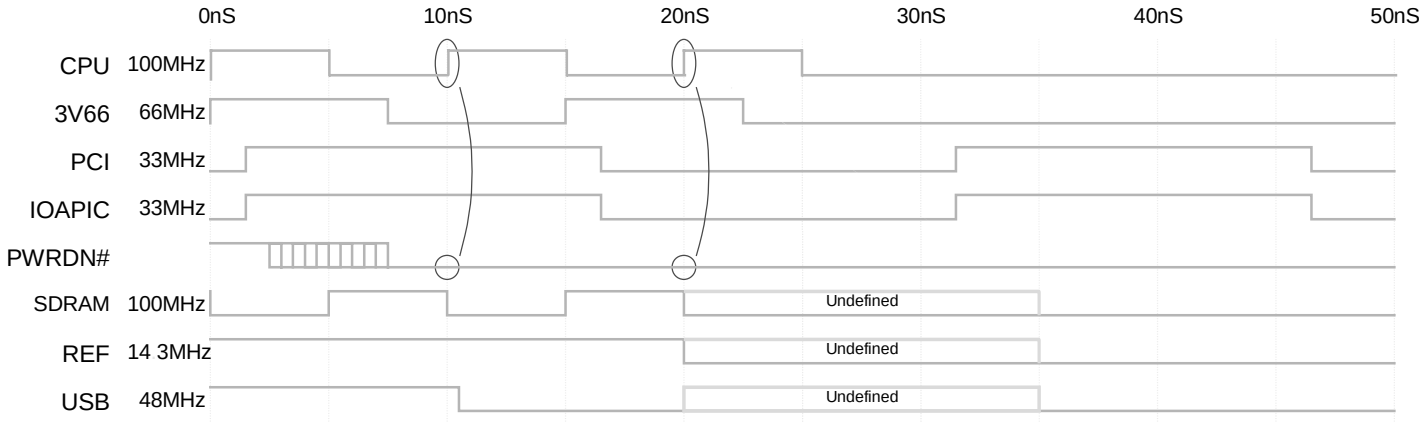


Fig.2

Power Management Current

PD#, SEL2, SEL1, SEL0	Maximum 2.5 Volt Current Consumption (VDDC = VDDI =2.625)	Maximum 3.3 Volt Current Consumption (VDD = VDDA = VDDS = 3.465 V)
0XXX (Power down)	10mA	10mA
1010 (66MHz)	70 mA	280 mA
1011 (100MHz)	100 mA	280 mA
1101 (133MHz)	133 mA	365 mA

Table 3

When exiting the power down mode, the designer must supply power to the VDD pins first, a minimum of 200mS before releasing the PD# pin high.

IOAPIC Clock Synchronization and Phase Alignment

This device incorporates IOAPIC clock synchronization. With this feature, the IOAPIC clocks are derived from the CPU clock. The IOAPIC clock lags the CPU clock by the specified 1.5 to 3.5 nSec. Figure 3 shows the relationship between the CPU and IOAPIC clocks.

Clock Phase Relationships

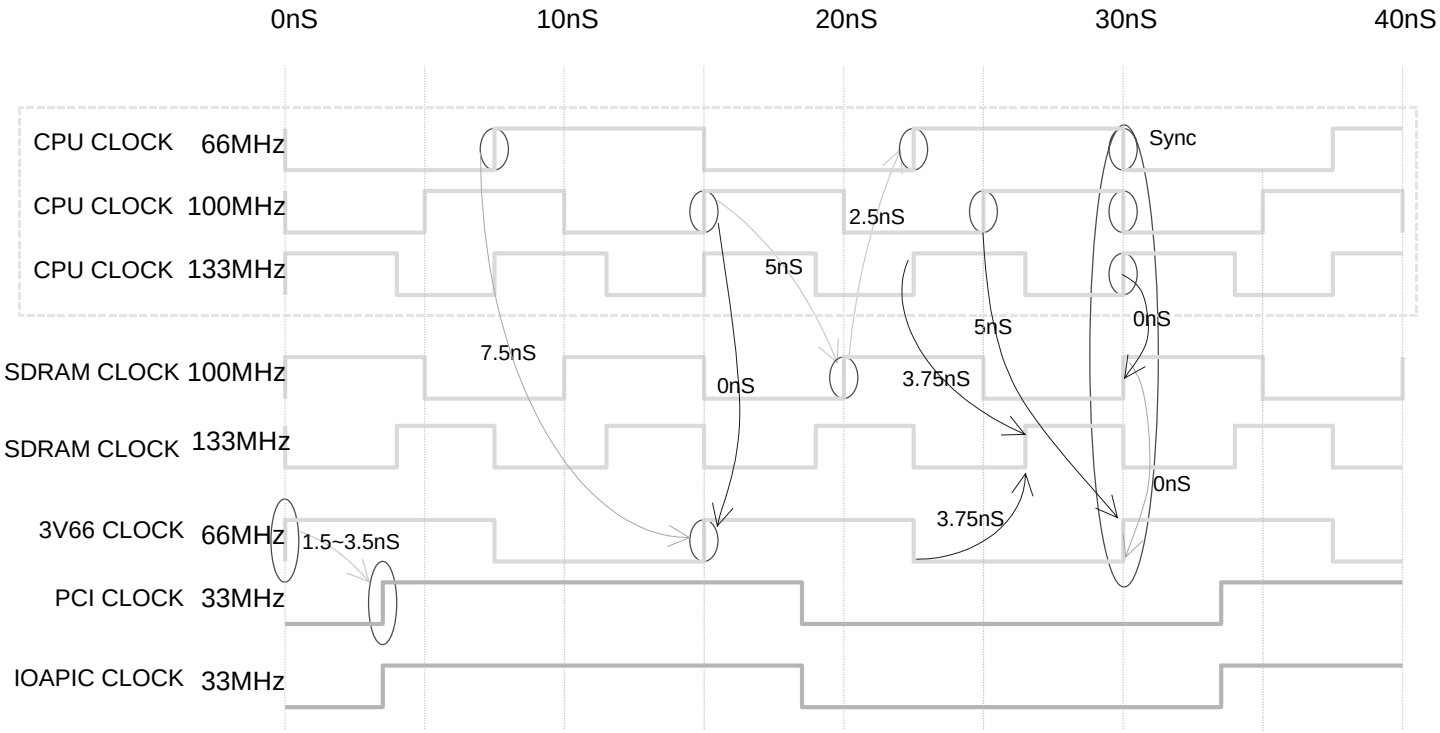


Fig.3

Group Timing Relationships and Tolerances

	CPU = 66.6 MHz, SDRAM = 100 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	2.5	500	SDRAM Leads
CPU to 3V66	7.5	500	180 degrees phase shift
SDRAM to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
	CPU = 100 MHz, SDRAM = 100 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	5	500	180 degrees phase shift
CPU to 3V66	5	500	CPU leads
SDRAM to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
	CPU = 133.3 MHz, SDRAM = 100 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	0	500	When rising edges line-up
CPU to 3V66	0	500	
SDRAM to 3V66	0	500	When rising edges line-up
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	
	CPU = 133.3 MHz, SDRAM = 133.3 MHz		
	Offset (nS)	**Tolerance (pS)**	**Conditions**
CPU to SDRAM	3.75	500	180 degrees phase shift
CPU to 3V66	0	500	
SDRAM to 3V66	3.75	500	
3V66 to PCI	1.5-3.5	500	3V66 leads
PCI to IOAPIC	0	1000	

Power on Bi-Directional Pins

Power Up Condition:

Pin1 is a Power up bi-directional pin and is used for selecting the host frequency in page 1, table 1. During power-up of the device, this pin is in input mode (see Fig 4, below), therefore; it is considered input select pin, Sel2 internal to the IC. After a settling time, the selection data is latch into the internal control register and this pin becomes a clock output.

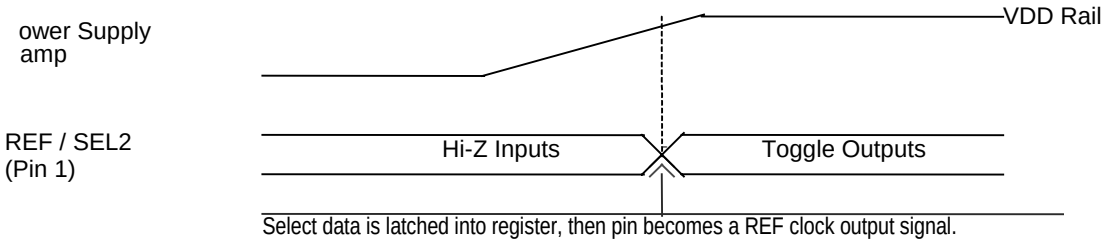


Fig.4

Strapping Resistor Options:

The power up bi-directional pin has a large value pull-down (50KΩ+/–20KΩ), therefore, a selection "0" is the default. If the system uses a slow power supply (over 10mS settling time), then **it is recommended** to use an external Pull-down (Rdn) in order to insure a low selection. In this case, the designer may choose one of two configurations, see Fig.5A and 5B.

Fig. 5A represents an additional pull down resistor 5KΩ connected from the pin to the power line, which allows a faster down to a high level.
If a selection "1" is desired, then a jumper is placed on JP1 to a 1 KΩ resistor as shown in Fig.5A. Please note the selection resistors (Rup and Rdn) are placed before the Damping resistor (Rd) close to the pin.

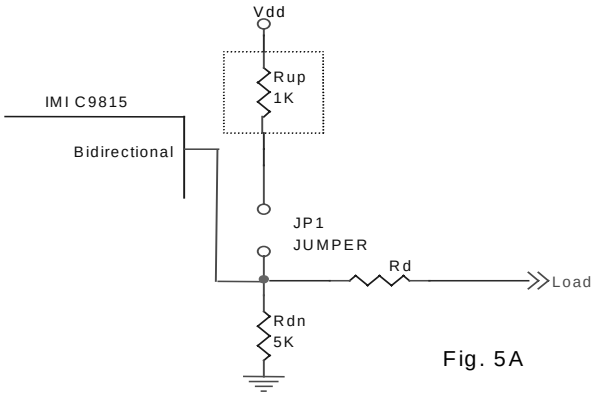


Fig. 5A

Fig. 5B represent a single resistor 5KΩ connected to a 3-way jumper, JP2. When a "1" selection is desired, a jumper is placed between leads1 and 3. When a "0" selection is desired, a jumper is placed between leads 1 and 2.

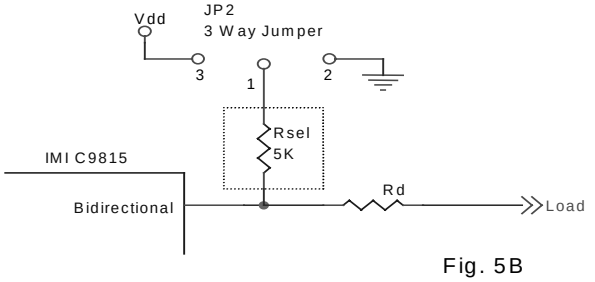


Fig. 5B

2-Wire SMBUS Control Interface

The 2-wire control interface implements a read/write slave only interface according to SMBus specification. (See Fig. 6 below). The device can be read back by using standard SMBUS command bytes. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is an 8-bit address. The LSB address Byte = 0 in write mode.

The device will respond to transfers of 10 bytes (max) of data. The device will generate an acknowledge (low) signal on the SDATA wire following reception of each byte. Data is transferred MSB first at a max rate of 100kbits/S. This device will also respond to a D3 address which sets it in a read mode. It will not respond to any other control interface conditions, and previously set control registers are retained.

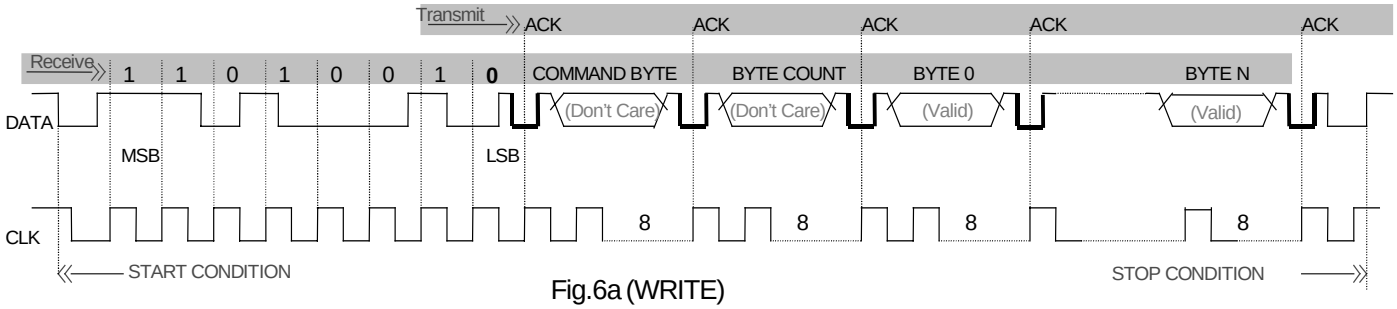


Fig.6a (WRITE)

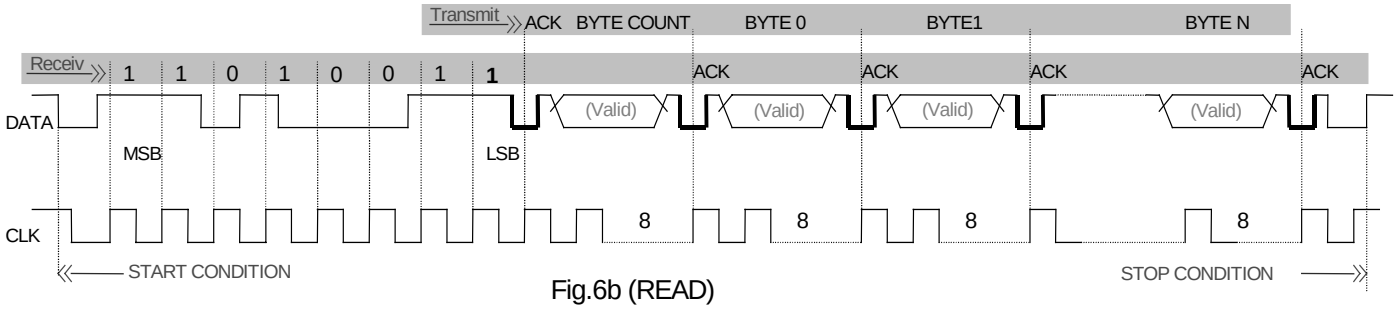


Fig.6b (READ)

Figure 6
SMBUS Communications Waveforms

Serial Control Registers

NOTE: The Pin# column lists the relevant pin number where applicable. The @Pup column gives the default state at power up.

Following the acknowledge of the Address Byte, two additional bytes must be sent:
1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

After the Command Code and the Count bytes have been acknowledged, the sequence described below (Byte 0, Byte 1, and Byte 2) will be valid and acknowledged.

Byte 0: CPU Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	0	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	0	-	Reserved
3	0	-	Spread spectrum mode
2	1	26	DOT
1	1	25	USB
0	1	49	CPU2_ITP

Byte 1: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	36	SDRAM7
6	1	37	SDRAM6
5	1	39	SDRAM5
4	1	40	SDRAM4
3	1	42	SDRAM3
2	1	43	SDRAM2
1	1	45	SDRAM1
0	1	46	SDRAM0

Byte 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	@Pup	Pin#	Description
7	1	9	3V66-2 (AGP)
6	1	20	PCI6
5	1	19	PCI5
4	1	18	PCI4
3	1	16	PCI3
2	1	15	PCI2
1	1	13	PCI1
0	0	-	Reserved

Byte 3: Reserved Register

Bit	@Pup	Pin#	Description
7	0	-	RESERVED
6	0	-	RESERVED
5	0	-	RESERVED
4	0	-	RESERVED
3	0	-	RESERVED
2	0	-	RESERVED
1	0	-	RESERVED
0	0	-	0 = SDRAM runs at 100MHz 1= SDRAM runs at 133.3MHz

Byte 4: Reserved Register

Byte 5: SSCG Control Register

Bit	@Pup	Pin#	Description
7	0	-	Spread Mode (0=down, 1=center)
6	0	-	Selects spread bandwidth. Ref. Table 4
5	0	-	Selects spread bandwidth. Ref. Table 4
4	0	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	0	-	Reserved
0	0	-	Reserved

SMBUS Test Circuitry

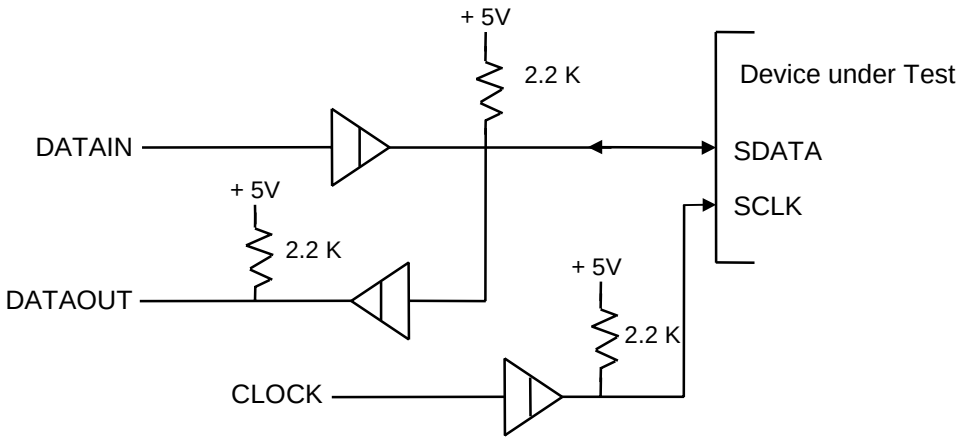


Fig.7

Note: Buffer is 7407 with VCC @ 5.0 V

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique applied here for maximum efficiency in minimizing Electro-Magnetic Interference radiation generated from repetitive digital signals mainly clocks. A clock accumulates EM energy at the center frequency it is generating. Spread Spectrum distributes this energy over a small frequency bandwidth therefore distributing an even amount of energy over a wider spectrum. This technique is achieved by modulating the clock either down (Fig.8A) or around the center (Fig.8B) of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth). In this device, Spread Spectrum is enabled by setting SMBUS byte0, bit3 = 1. The default of the device at power up keeps the Spread Spectrum disabled, it is therefore, important to have SMBUS accessibility to turn-on the Spread Spectrum function. Once the Spread Spectrum is enabled, the spread bandwidth option is selected by SST(0:2) in SMBUS byte 5, bits 5, 6 & 7 following tables 4A, and 4B below.

In Down Spread mode the center frequency is shifted down from its rested (non-spread) value by ½ of the total spread %. (eg.: assuming the center frequency is 100MHz in non-spread mode; when down spread of –0.5% is enabled, the center frequency shifts to 99.75MHz.).

In Center Spread mode, the Center frequency remains the same as in the non-spread mode.

Down Spread

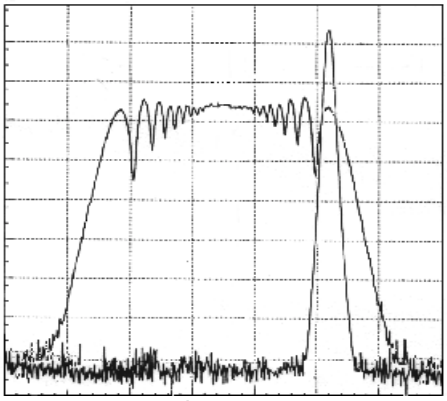


Figure 8A

Center Spread

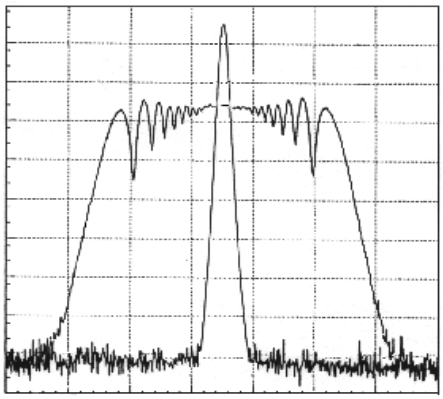


Figure 8B

Spread Spectrum Selection Tables

I²C BYTE5 Bit[7:5]	Spread %
000	- 0.5
001	- 0.7
010	- 1.0
011	- 0.25

Table 4A

I²C BYTE5 Bit[7:5]	Spread %
100	± 0.25
101	± 0.35
110	± 0.5
111	+/- 0.125

Table 4B

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65ºC to + 150ºC
Operating Temperature: 0ºC to +85ºC
Maximum ESD protection 2KV
Maximum Power Supply: 5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters (All outputs loaded per table 5 below) (VDD=VDDS = 3.3V ±5%, VDDC = VDDI = 2.5 ± 5%, TA = 0º to +85ºC)

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	Note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	Note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL1	-66		-5	µA	For internal Pull up resistors, Note 6
Input High Current (@VIL =VDD)	IIH1			5	µA	
Input Low Current (@VIL = VSS)	IIL2				µA	For internal Pull Down resistors, Note 6
Input High Current (@VIL = VDD)	IIH2				µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	280	mA	Sel2 = 0, Sel1 = Sel0 = 1
Dynamic Supply Current	Idd2.5V	-	-	100	mA	Sel2 = 0, Sel1 = Sel0 = 1
Static Supply Current	Isdd	-	-	10	mA	Sel1 = Sel0 = x, PD# = 0
Input pin capacitance	Cin	-	-	5	pF	
Output pin capacitance	Cout	-	-	6	pF	
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	32	34	38	pF	Measured from Pin to Ground. Note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.

Note1: Applicable to input signals: Sel(0:1), PD# (pull up), SEL2 (pull down)
Note2: Applicable to Sdata, and Sclk.
Note3: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note5: Although the device will reliably interface with crystals of a 17pF – 20pF C_L range, it is optimized to interface with a typical C_L = 18pF crystal specifications.
Note6: Internal Pull up and Pull down resistors have a typical value of 50k (it may vary between 30K and 70K).

Clock Name	Max Load (in pF)
CPU(0:2), IOAPIC(0:1), REF, USB	20
PCI(0:6), SDRAM(0:7), DCLK, 3V66(0:2)	30
DOT	15

Table 5.

AC Parameters

Symbol	Parameter	133 MHz Host		100 MHz Host		66 MHz Host		Units
		Min	Max	Min	Max	Min	Max	
TPeriod	CPU(0:2) period[5,8]	7.5	8.0	10.0	10.5	14.75	15.25	nS
THIGH	CPU(0:2) high time[10]	1.87	-	3.0	-	5.2	-	nS
TLOW	CPU(0:2) low time[11]	1.67	-	2.8	-	5.0	-	nS
Tr / Tf	CPU(0:2) rise and fall times[7]	0.4	1.6	0.4	1.6	0.4	1.6	nS
TSKEW	CPU0 to CPU Skew[6,9]	-	175	-	175	-	175	pS
TCCJ	CPU(0:2) Cycle to Cycle Jitter[6,9]	-	250	-	250	-	250	pS
TPeriod	SDRAM(0:7) and DCLK period[5,6]	7.5	8.0	10.0	10.5	10.0	10.5	nS
THIGH	SDRAM(0:7) and DCLK high time[10]	1.87	-	3.0	-	3.0	-	nS
TLOW	SDRAM(0:7) and DCLK low time[11]	1.67	-	2.8	-	2.8	-	nS
Tr / Tf	SDRAM(0:7) and DCLK rise and fall times[7]	0.4	1.6	0.4	1.6	0.4	1.6	nS
TSKEW	SDRAM(0:7) and DCLK Skew[6,9]	-	250	-	250	-	250	pS
TCCJ	SDRAM(0:7), DCLK Cycle to Cycle Jitter[6,9]	-	250	-	250	-	250	pS
TPeriod	IOAPIC(0:1) period[5,6]	30.0	-	30.0	-	30.0	-	nS
THIGH	IOAPIC(0:1) high time[10]	12.0	-	12.0	-	12.0	-	nS
TLOW	IOAPIC(0:1) low time[11]	12.0	-	12.0	N/S	12.0	-	nS
Tr / Tf	IOAPIC(0:1) rise and fall times[7]	0.4	1.6	0.4	1.6	0.4	1.6	nS
TCCJ	IOAPIC(0:1) Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	pS
TPeriod	3V66-(0:2) period[5,6]	15.0	16.0	15.0	16.0	15.0	16.0	nS
THIGH	3V66-(0:2) high time[10]	5.25	-	5.25	-	5.25	-	nS
TLOW	3V66-(0:2) low time[11]	5.05	-	5.05	-	5.05	-	nS
Tr / Tf	3V66-(0:2) rise and fall times[7]	0.5	2.0	0.5	2.0	0.5	2.0	nS
TSKEW	(Any 3V66) to (any 3V66) Skew[6,9]	-	175	-	175	-	175	pS
TCCJ	3V66-(0:2) Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	pS
TPeriod	PCI(0:6) period[5,6]	30.0	-	30.0	-	30.0	-	nS
THIGH	PCI(0:6) period[10]	12.0	-	12.0	-	12.0	-	nS
TLOW	PCI(0:6) low time[11]	12.0	-	12.0	-	12.0	-	nS
Tr / Tf	PCI(0:6) rise and fall times[7]	0.5	2.0	0.5	2.0	0.5	2.0	nS
TSKEW	(Any PCI) to (Any PCI) Skew[6,9]	-	500	-	500	-	500	pS
TCCJ	PCI(0:6) Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	pS
TPeriod	DOT & USB period (conforms to +167ppm max) [5,6]	20.8299	20.8333	20.8299	20.8333	20.829	20.833	nS
Tr / Tf	DOT & USB rise and fall times[7]	1.0	4.0	1.0	4.0	1.0	4.0	nS
TCCJ	DOT & USB Cycle to Cycle Jitter[6,9]	-	500	-	500	-	500	pS

Symbol	Parameter	133 MHz Host		100 MHz Host		66 MHz Host		Units
		Min	Max	Min	Max	Min	Max	
TPeriod	REF period[5,6]	69.8413	71.0	69.8413	71.0	69.8413	71.0	nS
Tr / Tf	REF rise and fall times[7]	1.0	4.0	1.0	4.0	1.0	4.0	nS
TCCJ	REF Cycle to Cycle Jitter[6]	-	1000	-	1000	-	1000	pS
tpZL, tpZH	Output enable delay (all outputs)[8]	1.0	10.0	1.0	10.0	1.0	10.0	nS
tpLZ, tpHZ	Output disable delay (all outputs)[13]	1.0	10.0	1.0	10.0	1.0	10.0	nS
tstable	All clock Stabilization from power-up[12]		3		3		3	mS
Tduty	Duty Cycle for All outputs[14]	45	55	45	55	45	55	%

Note 5: This parameter is measured as an average over 1uS duration, with a crystal center frequency of 14.31818MHz
Note 6: All outputs loaded as per table 5, page 11. Probes are placed on the pins and taken at 1.5V levels for 3.3V signals and at 1.25V for 2.5V signals (figs. 9A and 9B).
Note 7: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals and between 0.4V and 2.0V for 2.5V signals (see Fig.9A and Fig.9B)
Note 8: Measured from when both SEL1 and SEL0 are switched to high (enable).
Note 9: This measurement is applicable with Spread ON or Spread OFF.
Note 10: Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals, (see Figs. 9A & 9B)
Note 11: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 12: The time specified is measured from when all VDD's reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications
Note 13: Measured from when both SEL1 and SEL0 are switched to low (disable).
Note 14: Device designed for Typical Duty Cycle of 50%.

Output Buffer Characteristics (VDD=VDDS=3.3V ±5%, VDDC=VDDI=2.5±5%, TA=0 to 85ºC)

CPU and IOAPIC

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-15	-31	-51	mA	Vout =VDDC - 0.5V (or VDDI –0.5V)
Pull-Up Current	IOH_2	-26	-58	-101	mA	Vout = 1.2 V
Pull-Down Current	IOL_1	12	24	40	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	27	56	93	mA	Vout = 1.2 V

PCI, 3V66 and DOT

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-20	-25	-33	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-30	-54	-184	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9.4	18	38	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	28	55	148	mA	Vout = 1.5 V

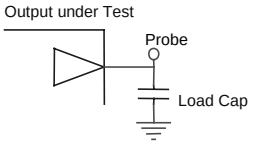
USB and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-12	-20	-30	mA	Vout =VDD - 1.0 V
Pull-Up Current	IOH_2	-27	-43	-92	mA	Vout = 1. 5 V
Pull-Down Current	IOL_1	9	13	27	mA	Vout = 0.4 V
Pull-Down Current	IOL_2	26	39	79	mA	Vout = 1.5 V

Buffer Characteristics for SDRAM

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-30	-40	-60	mA	Vout =VDD - 1. 0 V
Pull-Up Current	IOH_2	-68	-110	-188	mA	Vout = 1. 4 V
Pull-Down Current	IOL_1	23	34	53	mA	Vout = 0.4 V
Pull-Down Current	IOL_1	64	98	159	mA	Vout = 1.5 V

Test and Measurement Condition



3.3V signals

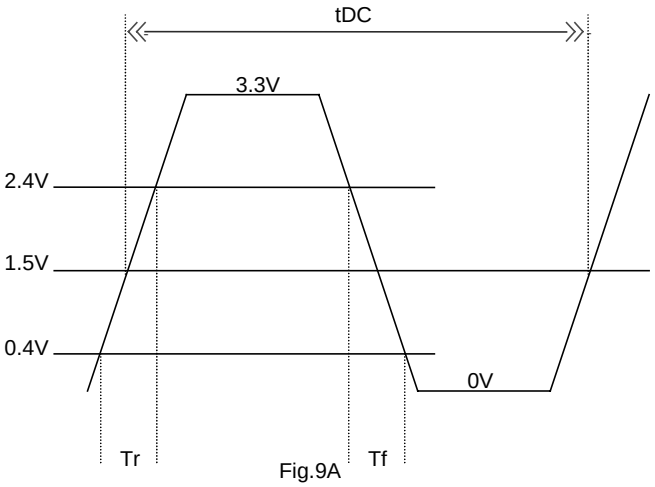


Fig.9A

2.5V signals

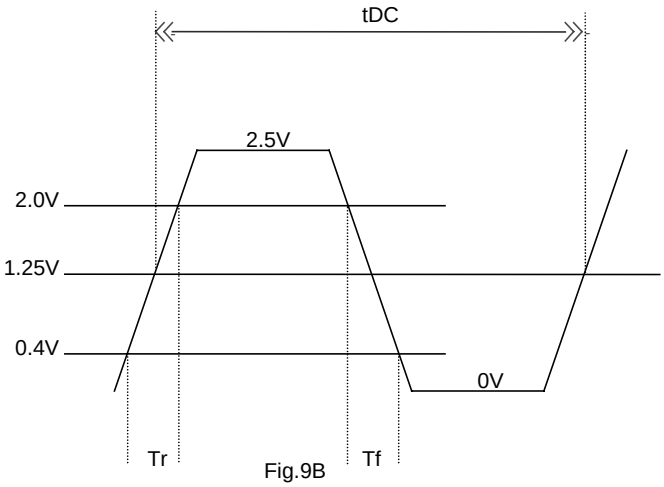


Fig.9B

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	12.00	14.31818	16.00	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
	T_A	-	-	5	PPM	Aging (first year @ 25C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

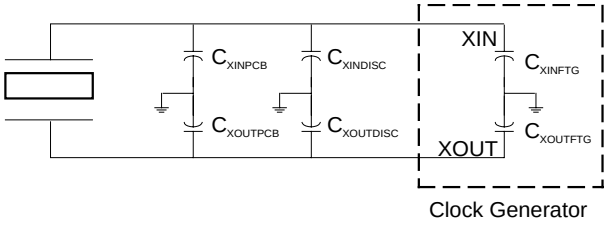
To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit traces (C_{PCB}), and any onboard discrete load capacitors (C_{DISC}).

The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground



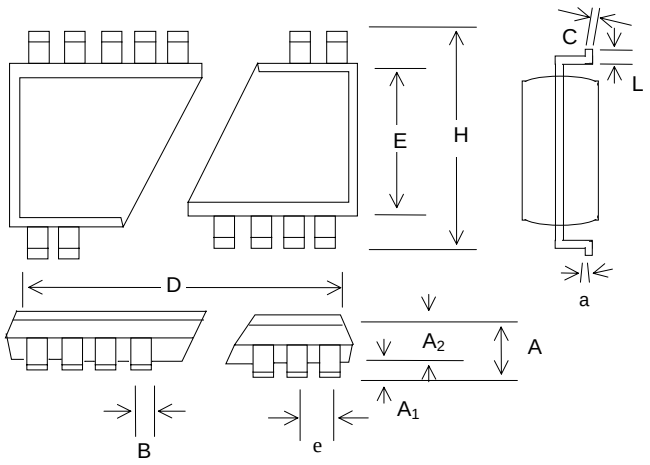
Suggested Oscillator Crystal Parameters (Cont.)

As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF.

Package Drawing and Dimensions



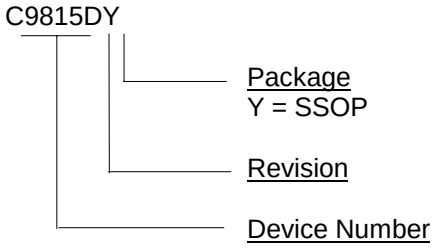
56 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.720	0.725	0.730	18.29	18.42	18.54
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9815DY	56 PIN SSOP	Commercial, 0 to 85ºC

Marking: Example: Cypress
C9815DY
Date Code, Lot #



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Document Title: C9815 Low EMI Clock Generator for Intel® 133 MHz/2DIMM Chipset Systems
Document Number: 38-07054

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	107062	06/11/01	IKA	Convert from IMI to Cypress